BUSBAR GEOMETRY AND DESIGN TECHNIQUES FOR CORELESS ACS37610 DIFFERENTIAL CURRENT SENSOR

By Yannick Vuillermet
Allegro MicroSystems

INTRODUCTION

The purpose of this application note is to offer guidelines for selecting the optimum combination of ACS37610 and busbar geometry for a given current sensor application and its specific requirements.

The ACS37610 is a Hall-plate-based differential current sensor designed to measure current flowing in a busbar or a PCB without using a ferromagnetic concentrator core. It is a contactless current sensor and features differential sensing to reject common-mode stray magnetic fields. It is recommended for typical current measurement ranging from 200 A to more than 1000 A. Because of its low-noise Hall plates, a reasonably good resolution can be achieved without using a ferromagnetic concentrator core. When higher accuracy or resolution is required, Allegro recommends using a ferromagnetic concentrator core in conjunction with, for example, A1365, A1367, or ACS70310 linear ICs.

Figure 1 illustrates how the ACS37610 senses the magnetic field induced by the current, I, flowing in the busbar. The ACS37610 has two Hall plates, sensitive along the Z axis and 2.58 mm away from each other. B_L is the magnetic field measured by the left Hall plate, and B_R is the magnetic field measured by the right Hall plate. The output voltage, V_{OUT}, of the sensor is proportional to the differential magnetic field, ΔB (equation 1 and equation 2). α is the ACS37610 output sensitivity to magnetic field; this is a programmable value to best match the application requirements. The relationship between the applied current and the differential field is given by the coupling factor, C_F (equation 3). A high coupling factor is usually recommended for high accuracy and for fine output resolution. This can be understood from equation 4, which gives the definition of the resolution δ, where ε is the input referred noise density and BW is the required bandwidth.

$$\Delta B = B_R - B_L \quad (1)$$

$$V_{OUT} = \alpha \times \Delta B \quad (2)$$

$$\Delta B = CF \times I \quad (3)$$

$$\delta = \frac{\varepsilon \times \sqrt{BW \times \pi/2}}{CF} \quad (4)$$

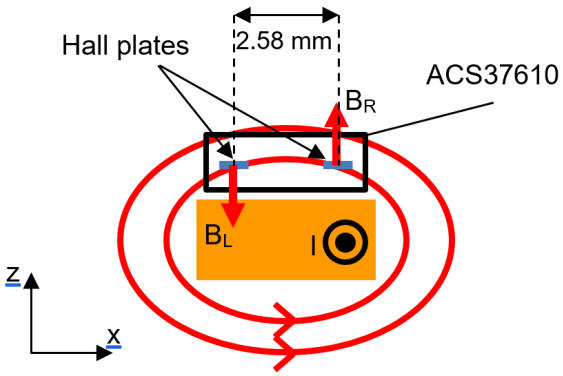


Figure 1. ACS37610 measurement principle

While the ACS37610 would function using any busbar design, to achieve best performance (accuracy, high signal-to-noise ratio, high bandwidth, low sensitivity to mechanical tolerances, etc.), the busbar must include certain features. In addition, placement of the IC relative to the busbar must be considered. Depending on the application requirements, the optimum busbar geometry can vary. In this document, alternative designs to bare busbars are proposed. Recommended busbar designs and expected performances are given for four different current ranges: ±300 A, ±600 A, ±900 A and ±1200 A.

Note that all results in this document come from 3D magnetic field simulations.

Busbar Design

The various geometries and corresponding parameters are shown in Figure 2 (bare), Figure 3 (notch), Figure 4 (slit), Figure 5 (rift), Figure 6 (single vertical slit), and Figure 7 (double vertical slit).

Bare busbar, notch, and rift designs allow easiest mechanical assembly, as the IC is mounted on top or below the busbar. Observe that the PCB is placed between the IC and the busbar in the figures. However, the IC could be placed between the busbar and the PCB to minimize the air gap and maximize the coupling factor. In this case, the limiting factor is the voltage isolation.

Slit and vertical slit designs are more mechanically challenging since the IC must be inserted in the busbar. Voltage isolation should also be considered for the vertical slit.

The air gap is defined by the distance between the Hall plates and the top of the busbar for the bare, notch, slit, and rift designs (Figure 8). For the vertical slit, the air gap is defined from the top of the busbar to the middle of the package (Figure 9).

Note that for the slit and vertical slit designs, the air gap can be negative. Figure 8 represents a positive air gap, while Figure 9 shows a negative air gap.

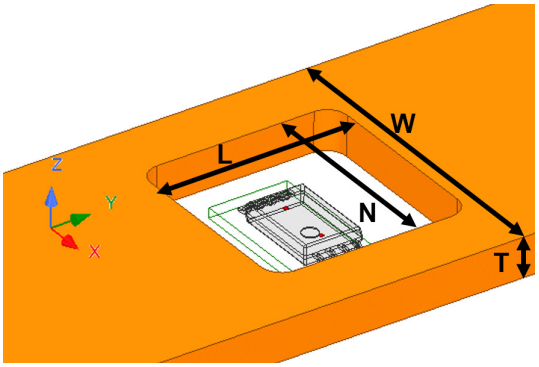


Figure 4. Slit

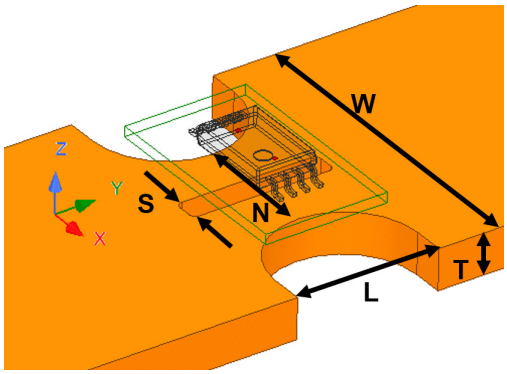


Figure 5. Rift

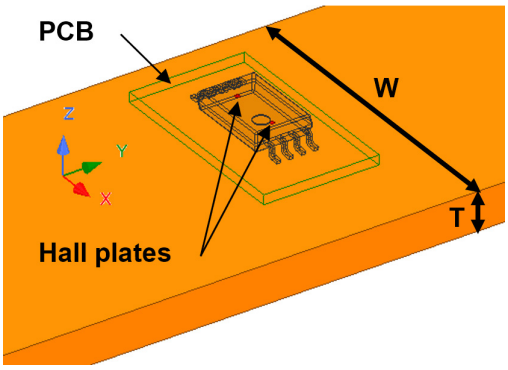


Figure 2. Bare busbar

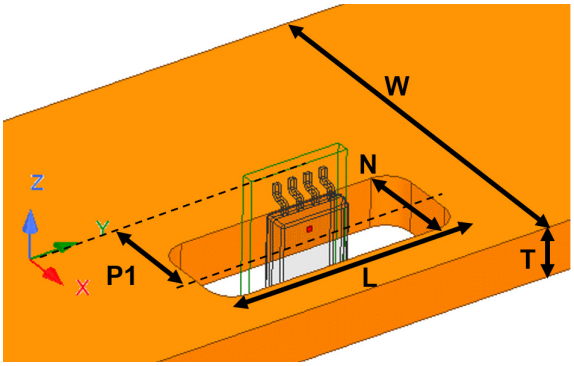


Figure 6. Single vertical slit

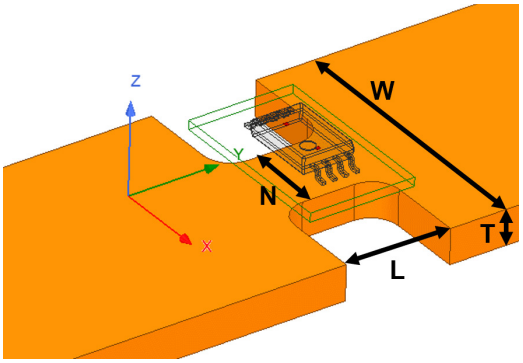


Figure 3. Notch

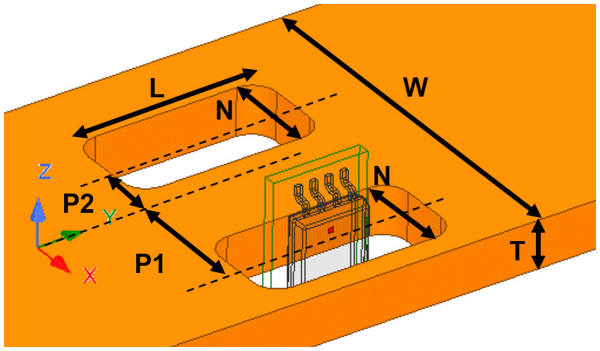


Figure 7. Double vertical slit

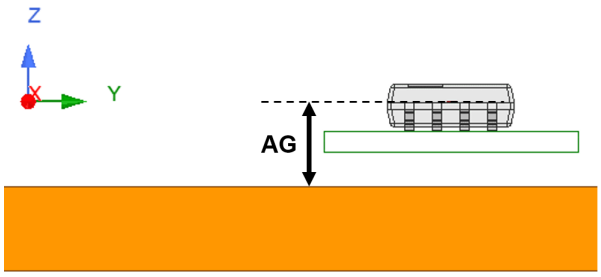


Figure 8. Air gap definition for bare, notch, slit, and rift designs

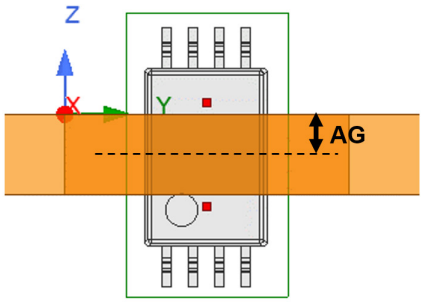


Figure 9. Air gap definition for single and double vertical slit

Optimum Designs

The bare busbars are designed to drive ~20 A/mm² at peak current. Table 1 through Table 4 contain the optimum designs for ±300 A, ±600 A, ±900 A, and ±1200 A applications.

The best performing designs have been selected based on specific conditions for each configuration.

For the notch, a maximum current density of 75 A/mm² in the neckdown is considered. This value is based on Allegro's experiences with high current applications. However, the current density can be higher or lower depending on thermal conditions (i.e. cooling) in the application. The length L is a compromise between overheating and AC performance: a long length L tends to improve the AC performance but may increase the busbar resistance significantly. L = 6 mm is usually the optimum length. For L > 8 mm, the AC performance reaches a plateau and does not improve further.

The slit is constrained by the busbar dimensions and IC package dimensions (6.4 mm × 3.0 mm × 1.1 mm). For example, the ±300 A application considered here has an 8 mm width busbar; a slit for the ACS37610 would not be possible. The proposed slit is also designed to optimize AC performances and tolerance to mechanical placement.

The rift is designed to be mostly insensitive to IC placement tolerance along air gap direction while still having a sufficient coupling factor.

The vertical slit dimensions are fixed by the IC package and electrical isolation requirements. The slit position along the X direction is optimized to have a flat sensor output over frequency, up to a few kHz. The behavior over frequency can be further improved by adding a second slit (if the busbar width is large enough), which must be placed appropriately along the X direction. For simplicity, the width of the second slit here is fixed to the same value as the first slit, but this not mandatory. For further AC behavior improvements, more slits could be added.

Table 1 through Table 4 are given at nominal air gap and 2 kHz AC current. This frequency is considered because it is a typical automotive inverter switching frequency. For the bare, notch, and rift configurations, and for typical applications, the nominal air gap is 2 mm. For the slit configurations, the nominal air gap is $AG = -T / 2$, corresponding to where the Hall plates are centered relative to the busbar thickness, T. For vertical slit configurations, the nominal air gap is also $AG = -T / 2$, corresponding to where the IC is centered relative to the busbar thickness, T.

More detailed information is available in Table 6 through Table 9 at the end of this document; they contain frequencies from 1 to 10 kHz and a few air gaps per configuration.

The following performances were evaluated:

- **Nominal coupling factor (CF):** Corresponds to the DC coupling factor where the IC is perfectly placed relatively to the busbar. For example, for the notch design, it corresponds to the center of the Hall plate spacing exactly at the center of the notch. Expressed in mG/A.
- **Sensitivity to IC misplacement along X, Y, and Z axis (CFΔX):** Once the IC is mounted and calibrated in the application, any motion or misplacements due to thermal expansion, vibration, etc., of the sensor relative to the busbar is not going to be covered by calibration. Expressed in percentage of the nominal coupling factor per 100 µm of misplacement.
- **Sensitivity to IC tilt around X, Y and Z axis (CF@X):** Expressed in percentage of the nominal coupling factor per degree of tilt.
- **Coupling factor variation with current frequency (CFAC):** When an AC current flows in the busbar, eddy currents are generated. These eddy currents alter the current density and, thus, the magnetic field distribution sensed by the IC. Expressed in percentage of the nominal coupling factor in DC.
- **Phase delay (PD):** Eddy currents introduce a delay in

the measured magnetic field. Expressed in degrees out of phase (electrical degree).

• **Crosstalk (CT):** For multiple phases systems, crosstalk measures the impact of the adjacent phase on the measured phase. Expressed in percentage of the nominal coupling factor. Calculated assuming 30 mm center-to-center distance, C, between two adjacent busbars and assuming parallel busbars (Figure 10).

• **Resistance increase (ΔR):** Indicates the increase of busbar resistance due to the geometry modification. Expressed in μΩ and assumes copper busbars.

• **IC sensitivity (ICsens):** Required IC sensitivity to measure the full current range with a 4000 mV output sweep. Expressed in mV/G.

Crosstalk is highly dependent on the busbar's layout and IC positioning. The results reported in the tables below are given for a worst case where the busbars are parallel. If necessary, the crosstalk can be reduced with smart IC placement and optimized busbar layout. For example, crosstalk can be improved by rotating the IC 90° around the Z axis and using busbars having elbows (Figure 11).

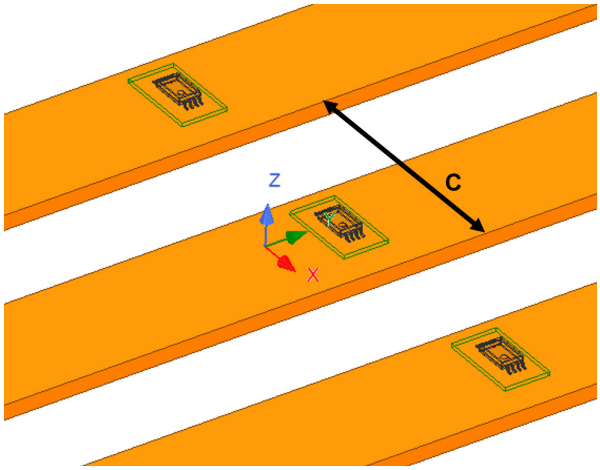


Figure 10. Crosstalk

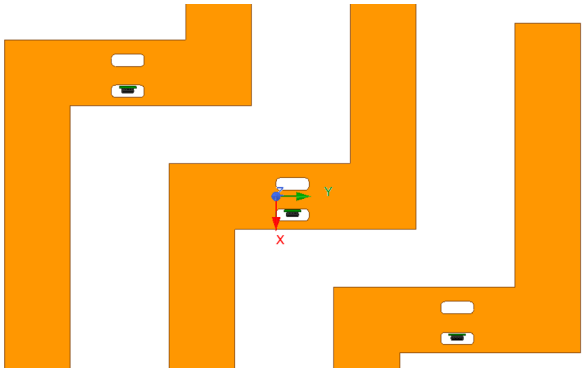


Figure 11. Example of crosstalk optimization

Table 1: Performance summary for ±300 A application

Symbol (Characteristic)	Bare	Notch	Single Vertical Slit	Unit
W (Width)		8		mm
T (Thickness)		2		mm
L (Length)	n/a	6.0	10	mm
N (Notch width)	n/a	4.0	3	mm
S (Slit width)	n/a	n/a	n/a	mm
P1	n/a	n/a	0.5	mm
P2	n/a	n/a	n/a	mm
ΔR (Resistance increase)	0.0	6.5	6.5	μΩ
AG (Air Gap)	2	2	–1	mm
CF (Nominal coupling factor)	206	376	580	mG/A
ICsens (Required IC sensitivity)	32	18	11	mV/G
CFΔZ (Sensitivity to Z misplacement)	2.4	4.8	1.3	%/100 μm
CFAC (Coupling factor variation @ 2 kHz)	**–12.5**	–1.2	**–0.3**	%
PD (Phase Delay @ 2 kHz)	**–15.5**	–2.5	–1.5	°elec
CT (Crosstalk @ 30 mm)	2.8	1.5	**1**	%
Mechanical Mounting	**Above busbar**	**Above busbar**	**Through busbar**	–

Table 2: Performance summary for ±600 A application

Symbol (Characteristic)	Bare	Notch	Slit	Rift	Single Vertical Slit	Unit
W (Width)			16			mm
T (Thickness)			2			mm
L (Length)	n/a	6.0	10	6	10	mm
N (Notch width)	n/a	4.5	10	10	5	mm
S (Slit width)	n/a	n/a	n/a	1.25	n/a	mm
P1	n/a	n/a	n/a	n/a	2	mm
P2	n/a	n/a	n/a	n/a	n/a	mm
ΔR (Resistance increase)	0.0	8.3	9.0	2.7	2.4	µΩ
AG (Air Gap)	2	2	–1	2	–1	mm
CF (Nominal coupling factor)	71	351	142	87	223	mG/A
ICsens (Required IC sensitivity)	47	9	23	39	15	mV/G
CFΔZ (Sensitivity to Z misplacement)	**0.8**	**4.6**	**0.2**	1.2	**0.7**	%/100 µm
CFAC (Coupling factor variation @ 2 kHz)	**–53.8**	–1.4	–1.7	**–23.1**	–1.9	%
PD (Phase Delay @ 2 kHz)	**–41**	**–3.5**	**–0.5**	**–23**	–2.0	°elec
CT (Crosstalk @ 30 mm)	**8.6**	1.6	**5.1**	**5.5**	**3.2**	%
Mechanical Mounting	**Above busbar**	**Above busbar**	**Inside busbar**	**Above busbar**	**Through busbar**	–

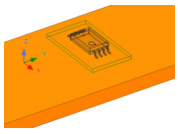
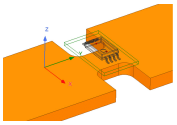
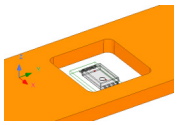
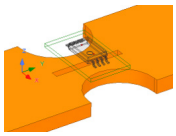
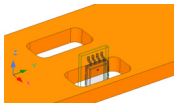
Table 3: Performance summary for ±900 A application

Symbol (Characteristic)	Bare	Notch	Slit	Rift	Single Vertical Slit	Unit
W (Width)			16			mm
T (Thickness)			3			mm
L (Length)	n/a	6	10	6	10	mm
N (Notch width)	n/a	4.5	10	10	5	mm
S (Slit width)	n/a	n/a	n/a	1.25	n/a	mm
P1	n/a	n/a	n/a	n/a	2	mm
P2	n/a	n/a	n/a	n/a	n/a	mm
ΔR (Resistance increase)	0.0	5.5	6.0	1.8	1.6	µΩ
AG (Air Gap)	2	2	–1.5	2	–1.5	mm
CF (Nominal coupling factor)	68	296	137	85	210	mG/A
ICsens (Required IC sensitivity)	33	8	16	26	11	mV/G
CFΔZ (Sensitivity to Z misplacement)	**0.9**	**4.4**	**0.2**	**0.4**	**0.6**	%/100 µm
CFAC (Coupling factor variation @ 2 kHz)	**–62.2**	–2.3	–2.5	**–30**	**–3.9**	%
PD (Phase Delay @ 2 kHz)	**–38**	**–4.0**	–1.5	**–25.5**	–2.5	°elec
CT (Crosstalk @ 30 mm)	**8.9**	1.9	**5.2**	**5.6**	**3.4**	%
Mechanical Mounting	**Above busbar**	**Above busbar**	**Inside busbar**	**Above busbar**	**Through busbar**	–

Table 4: Performance summary for ±1200 A application

Symbol (Characteristic)	Bare	Notch	Slit	Rift	Double Vertical Slit	Unit
W (Width)	21					mm
T (Thickness)	3					mm
L (Length)	n/a	6	10	6	10	mm
N (Notch width)	n/a	6	14	10	5	mm
S (Slit width)	n/a	n/a	n/a	1.25	n/a	mm
P1	n/a	n/a	n/a	n/a	6.0	mm
P2	n/a	n/a	n/a	n/a	–6.0	mm
ΔR (Resistance increase)	0.0	4.1	5.5	2.3	2.5	µΩ
AG (Air Gap)	2	2	–1.5	2	–1.5	mm
CF (Nominal coupling factor)	42	237	81	85	180	mG/A
ICsens (Required IC sensitivity)	40	7	21	20	9	mV/G
CFΔZ (Sensitivity to Z misplacement)	0.6	3.6	0.1	0.3	0.6	%/100 µm
CFAC (Coupling factor variation @ 2 kHz)	–74.9	–7.0	–3.3	–29.2	2.3	%
PD (Phase Delay @ 2 kHz)	–35.5	–9.5	–0.5	–26	–0.5	°elec
CT (Crosstalk @ 30 mm)	15	2.3	10.7	5.6	6.2	%
Mechanical Mounting	Above busbar	Above busbar	Inside busbar	Above busbar	Through busbar	–

Table 5: Geometry comparison summary

Characteristic	Bare	Notch	Slit	Rift	Vertical Slit
					
Coupling factor / resolution	Poor	Good	Fair	Fair	Good
Sensitivity to mechanical tolerance	Good	Poor [1] / Good [2]	Good	Good	Good
Sensitivity to AC current	Poor	Good	Fair	Poor	Good
Inherent crosstalk immunity	Poor	Good	Poor	Poor	Fair
Mechanical mounting	Good	Good	Fair	Good	Fair

[1] Without calibration once mounted in the application.
[2] With calibration once mounted in the application and good control of the relative movement between the busbars and the IC.

The results are summarized in Table 5. The best busbar design for a given application depends on its requirements (current range, AC or DC, single or multi-phases, etc.). Overall, the notch and the vertical slit configurations are the most robust designs and have the best performances. The vertical slit configuration main drawback is the mechanical mounting which can be challenging. The slit configuration suffers from poor inherent crosstalk immunity, but this could be overcome with a smart busbar and IC layout or by software. The drawback of the notch configuration is the sensitivity to mechanical placement along the air gap direction, Z. Nevertheless, this configuration is usually the preferred option by customers because of its overall good performances and easy mounting. The sensitivity to mechanical placement is overcome by calibrating the ACS37610 once mounted in the application and by a good control of the relative movement between the busbars and the IC (vibrations, thermal expansion, etc.).

From Table 5, the rift design does not appear better than the bare busbar, but it usually has a higher coupling factor leading to better resolution. Based on AC and crosstalk performances, the rift design would most likely be limited to DC and single-phase applications.

Conclusions

This application note indicates that the ACS37610 should be used with the right busbar design to achieve the best performance in each application. Depending on the application specifications and mechanical constraints, one design might be preferred.

This application note also reports some reference designs for various current ranges and their corresponding expected performances.

Allegro technical support can assist with the selection and design for the best busbar approach for a specific application.

Table 6: Full results for ±300 A application

Symbol	Bare			Notch			Single Vertical Slit			Units
W	8									mm
T	2									mm
L	n/a			6			10			mm
N	n/a			4			3			mm
S	n/a			n/a			n/a			mm
P1	n/a			n/a			0.5			mm
P2	n/a			n/a			n/a			mm
ΔR	0.0			3.2			6.5			µΩ
AG	1	2	3	1	2	3	–1	0	1	mm
CF	259	206	160	628	376	242	580	444	179	mG/A
CFΔX	0	0.1	0.2	0.8	0.7	0.5	0.7	0.4	0.7	%/100 µm
CFΔY	0	0	0	0.1	0.1	0.1	0	0	0	%/100 µm
CFΔZ	2.1	2.4	2.5	5.5	4.8	4.1	1.3	6	12.2	%/100 µm
CF@X	0.1	0.1	0.1	0.1	0.1	0.1	0	0.1	0.1	%/°
CF@Y	0.3	0.3	0.3	0.2	0.2	0.2	0.2	0.1	0	%/°
CF@Z	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	%/°
CFAC @ 1 kHz	–5.3	–3.9	–2.9	–0.4	–0.3	–0.3	0.1	0	0	%
CFAC @ 2 kHz	–17.3	–12.5	–9	–1.4	–1.2	–1.2	–0.3	–0.3	–0.2	%
CFAC @ 3 kHz	–30	–21.3	–15.3	–3	–2.4	–2.3	–1.2	–1.1	–0.3	%
CFAC @ 10 kHz	–64.3	–44.6	–31.7	–16.6	–11.3	–8.8	–6.6	–5.7	–0.4	%
PD @ 1 kHz	–14.5	–9	–6	–2	–1	–1	–0.5	–0.5	0	°elec
PD @ 2 kHz	–25.5	–15.5	–10	–4	–2.5	–2	–1.5	–1	0	°elec
PD @ 3 kHz	–32.5	–19	–12	–6	–3.5	–2.5	–2	–2	0	°elec
PD @ 10 kHz	–28.5	–15.5	–9.5	–11.5	–6	–4	–3.5	–2.5	1	°elec
ICsens	26	32	42	11	18	28	11	15	37	mV/G
CT @ 30 mm	2.3	2.8	3.5	0.9	1.5	2.2	1	1.3	3.3	%

Table 7: Full results for ±600 A application

Symbol	Bare			Notch			Slit			Rift			Single Vertical Slit			Units
W	16															mm
T	2															mm
L	n/a			6			10			6			10			mm
N	n/a			4.5			10			10			5			mm
S	n/a			n/a			n/a			1.25			n/a			mm
P1	n/a			n/a			n/a			n/a			2			mm
P2	n/a			n/a			n/a			n/a			n/a			mm
ΔR	0.0			8.3			9.0			2.7			2.4			μΩ
AG	1	2	3	1	2	3	–1	0	1	1	2	3	–1	0	1	mm
CF	76	71	65	566	351	229	142	131	103	54	87	86	223	194	127	mG/A
CFΔX	0.1	0	0	0.5	0.5	0.4	0.4	0.3	0.1	4.1	0.9	0.3	0.3	0.2	0.3	%/100 μm
CFΔY	0	0	0	0.1	0.1	0.1	0	0	0	0.1	0.1	0.1	0	0	0	%/100 μm
CFΔZ	0.6	0.8	1	4.9	4.6	4	0.2	1.6	3.2	11.9	1.2	0.8	0.7	3.2	5.4	%/100 μm
CF@X	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	%/°
CF@Y	0.3	0.3	0.3	0.3	0.2	0.3	0.3	0.3	0.3	0.9	0.4	0.3	0.2	0.2	0.1	%/°
CF@Z	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.2	0.1	0.1	0.1	0.1	0.1	%/°
CFAC @ 1 kHz	–30.6	–26.6	–22.4	–0.3	–0.3	–0.7	–0.8	–0.8	–0.8	–10.8	–8.6	–7.2	0.1	0	–0.4	%
CFAC @ 2 kHz	–63.2	–53.8	–44.6	–1.5	–1.4	–2	–1.7	–1.7	–1.7	–30.8	–23.1	–18.4	–1.9	–2	–2.3	%
CFAC @ 3 kHz	–77.3	–65.1	–54	–3.9	–3.1	–3.6	–2.3	–2.3	–2.3	–49.2	–34.7	–27	–3.1	–3.2	–3.5	%
CFAC @ 10 kHz	–84.5	–73.3	–62.8	–22.6	–15	–12.4	–3.6	–3.6	–3.6	–90.6	–55.6	–43.4	–4.3	–4.7	–5.8	%
PD @ 1 kHz	–46	–33.5	–25.5	–2.5	–1.5	–1.5	–0.5	–0.5	–0.5	–29	–15	–11	–1.5	–1	–1	°elec
PD @ 2 kHz	–62	–41	–29.5	–5.5	–3.5	–3	–0.5	–0.5	–0.5	–51.5	–23	–16	–2	–1.5	–1.5	°elec
PD @ 3 kHz	–55	–35.5	–25.5	–8.5	–5	–4	–0.5	–0.5	–0.5	–67.5	–26	–17	–2	–1.5	–1.5	°elec
PD @ 10 kHz	–22	–15	–11.5	–15	–8	–5.5	–0.5	–0.5	–0.5	–38.5	–15.5	–11.5	–1	–0.5	–1	°elec
ICsens	44	47	52	6	9	15	23	25	33	61	39	39	15	17	26	mV/G
CT @ 30 mm	8.2	8.6	9.2	1.1	1.6	2.3	5.1	5.5	6.9	7.5	5.5	5.5	3.2	3.7	5.6	%

Table 8: Full results for ±900 A application

Symbol	Bare			Notch			Slit				Rift			Single Vertical Slit				Units
W	16																	mm
T	3																	mm
L	n/a			6			10				6			10				mm
N	n/a			4.5			10				10			5				mm
S	n/a			n/a			n/a				1.25			n/a				mm
P1	n/a			n/a			n/a				n/a			2				mm
P2	n/a			n/a			n/a				n/a			n/a				mm
ΔR	0.0			5.5			6.0				1.8			1.6				μΩ
AG	1	2	3	1	2	3	–1.5	–1	0	1	1	2	3	–1.5	–1	0	1	mm
CF	73	68	61	469	296	196	137	135	116	86	66	85	81	210	204	159	96	mG/A
CFΔX	0	0	0	0.5	0.5	0.4	0.3	0.3	0.2	0	2.4	0.6	0.2	0.3	0.3	0.3	0.4	%/100 μm
CFΔY	0	0	0	0.1	0.1	0.1	0	0	0	0	0.1	0.1	0	0	0	0	0	%/100 μm
CFΔZ	0.7	0.9	1.1	4.8	4.4	3.9	0.2	0.8	2.3	3.7	6.4	0.4	1	0.6	1.8	3.9	6.1	%/100 μm
CF@X	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	%/°
CF@Y	0.3	0.3	0.3	0.3	0.2	0.3	0.3	0.3	0.3	0.3	0.6	0.4	0.3	0.2	0.2	0.1	0.1	%/°
CF@Z	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.2	0.1	0.1	0.1	0.1	0.1	0.1	%/°
CFAC @ 1 kHz	–43.1	–37.4	–31.5	–0.4	–0.7	–1.2	–1.3	–1.3	–1.3	–1.3	–15.7	–13.1	–11.1	–1.1	–1.1	–1.2	–1.4	%
CFAC @ 2 kHz	–73.7	–62.2	–51.5	–2.3	–2.3	–3.1	–2.5	–2.5	–2.4	–2.3	–38.3	–30	–24.4	–3.9	–3.9	–3.8	–3.6	%
CFAC @ 3 kHz	–81.4	–68.8	–57.6	–5.3	–4.5	–5.1	–3.4	–3.3	–3.2	–2.9	–55.4	–41.4	–32.7	–5.3	–5.3	–5.1	–4.5	%
CFAC @ 10 kHz	–84.8	–74	–63.7	–23.1	–15.3	–12.9	–5.9	–5.9	–5.2	–4.2	–84.9	–59.2	–46.4	–9.3	–9.1	–7.7	–5.4	%
PD @ 1 kHz	–53.5	–38.5	–28.5	–3	–2	–2	–1	–1	–1	–0.5	–31.5	–18	–13.5	–2	–2	–2	–1.5	°elec
PD @ 2 kHz	–59	–38	–27	–6	–4	–3.5	–1.5	–1.5	–1	–1	–51.5	–25.5	–17.5	–2.5	–2.5	–2	–1.5	°elec
PD @ 3 kHz	–42.5	–28.5	–21	–8.5	–5	–4	–1.5	–1.5	–1	–1	–62.5	–27	–17.5	–2.5	–2.5	–2	–1	°elec
PD @ 10 kHz	–21	–14	–10.5	–13	–6.5	–4.5	–1.5	–1	–1	–0.5	–59.5	–17	–11	–3	–2.5	–1.5	0.5	°elec
ICsens	30	33	36	5	8	11	16	16	19	26	33	26	27	11	11	14	23	mV/G
CT @ 30 mm	8.4	8.9	9.5	1.2	1.9	2.6	5.2	5.3	6.1	8.1	6.7	5.6	5.8	3.4	3.5	4.5	7.2	%

Table 9: Full results for ±1200 A application

Symbol	Bare			Notch			Slit				Rift			Double Vertical Slit				Units
W	21																	mm
T	3																	mm
L	n/a			6			10				6			10				mm
N	n/a			6			14				10			5				mm
S	n/a			n/a			n/a				1.25			n/a				mm
P1	n/a			n/a			n/a				n/a			6.0				mm
P2	n/a			n/a			n/a				n/a			–6.0				mm
ΔR	0.0			4.1			5.5				2.3			2.5				µΩ
AG	1	2	3	1	2	3	–1.5	–1	0	1	1	2	3	–1.5	–1	0	1	mm
CF	44	42	40	339	237	167	81	80	73	61	68	85	80	180	175	135	81	mG/A
CFΔX	0	0	0	0.1	0.2	0.3	0.2	0.2	0.1	0.1	2.4	0.7	0.2	0.7	0.7	0.7	0.7	%/100 µm
CFΔY	0	0	0	0.1	0.1	0.1	0.1	0.1	0	0	0.1	0.1	0.1	0	0	0	0	%/100 µm
CFΔZ	0.4	0.6	0.7	3.5	3.6	3.4	0.1	0.5	1.3	2.2	5.9	0.3	1.1	0.6	1.8	4	6.2	%/100 µm
CF@X	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	%/°
CF@Y	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.6	0.4	0.3	0.2	0.1	0.2	0.7	%/°
CF@Z	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.2	0.1	0.1	0.1	0.1	0.1	0.1	%/°
CFAC @ 1 kHz	–63.2	–56.9	–49.9	–2	–1.9	–2.4	–2.4	–2.4	–2.4	–2.3	–13.9	–12.6	–11.4	1.7	1.5	0.1	–3.3	%
CFAC @ 2 kHz	–84.5	–74.9	–65.7	–8.6	–7	–6.8	–3.3	–3.3	–3.3	–3.3	–36	–29.2	–24.5	2.3	2.1	0.2	–4.7	%
CFAC @ 3 kHz	–86	–77.1	–68.5	–16.6	–12.5	–11	–3.7	–3.7	–3.7	–3.7	–53.5	–40.9	–33	2.3	2.1	0.1	–5.1	%
CFAC @ 10 kHz	–88.5	–80.3	–72.2	–45.6	–30.4	–23.5	–4.4	–4.4	–4.4	–4.5	–84.2	–59.7	–47.7	–1.5	–1.5	–1.7	–3.9	%
PD @ 1 kHz	–69	–50	–38	–8	–5	–4	–1	–1	–1	–1	–30	–18	–13.5	0	0	0	–1	°elec
PD @ 2 kHz	–50.5	–35.5	–27	–15	–9.5	–7	–0.5	–0.5	–0.5	–0.5	–50	–26	–18	–0.5	–0.5	0	–0.5	°elec
PD @ 3 kHz	–34	–25	–20	–20	–11.5	–8	–0.5	–0.5	–0.5	–0.5	–61	–27.5	–18.5	–1.5	–1	–0.5	0	°elec
PD @ 10 kHz	–19.5	–13.5	–10.5	–22.5	–11	–7	–0.5	–0.5	–0.5	0	–56	–18	–12	–3.5	–3	–1	1.5	°elec
ICsens	38	40	42	5	7	10	21	21	23	27	25	20	21	9	10	12	21	mV/G
CT @ 30 mm	14.7	15	15.4	1.7	2.3	3.1	10.7	10.8	11.6	13.4	6.7	5.6	5.8	6.2	6.4	8	13	%

Revision History

Number	Date	Description	Responsibility
–	May 14, 2020	Initial release	Y. Vuillermet
1	September 14, 2020	Updated Figure 3, Optimum Designs section, Tables 1 to 9.	Y. Vuillermet
2	January 6, 2021	Updated Tables 4, 6-9.	Y. Vuillermet
3	October 26, 2021	Updated Figure 1.	Y. Vuillermet

955 PERIMETER ROAD • MANCHESTER, NH 03103 • USA
+1-603-626-2300 • FAX: +1-603-641-5336 • ALLEGROMICRO.COM