SIGNAL PATH DELAY FOR A31315 3D SENSOR

By Ahmad Nour Halawani
Allegro MicroSystems

INTRODUCTION

The delay in a signal path can be described as the trail between the real-time angle and the displayed output angle. This delay represents the time needed to convert the magnetic field data sensed by the Hall plates into angle information.

In actuator systems, the position sensor is part of the feedback loop, and it is critical to understand the dynamic behavior and transmit delay of the sensor so that the cut-off frequency and response time of the system can be defined. A properly defined signal path delay can be used to help determine the proper time delay between a position reading and the actual error, which enables estimation of the mechanical angle error due to the signal path delay.

When using SENT (SAE J2716 Single Edge Nibble Transmission) or analog output communication protocols, the mechanical angle output of the Allegro A31315 3D position sensor is affected by several contributors to the signal path delay. This application note describes these contributors and quantifies their effects based on their different settings.

CHANNEL PROCESSING DELAY

An in-chip signal delay can occur in two locations: 1) in each channel separately; or 2) in the signal processing that occurs between the two channels in performance of the angle calculation. The field received by each channel will pass separately through a set of signal processing blocks—namely, a low-pass filter block, a polarity checker, a sensitivity adjustment block, and, respectively, a temperature and an offset correction block—before angle processing. After the signal in each channel is processed, both channels will be joined in angular calculation.

The signal path toward the channel comprises the functional blocks shown in Figure 1. The delay elements can be divided into three parts—group delay from the filter and factory offset gain, customer trim delay (polarity, sensitivity, temperature compensation, and offset), and hysteresis calculation delay. These delay elements occur in series for each channel separately, and they serve to process the Hall-plate field measurements and to prepare the measurements for angle conversion.

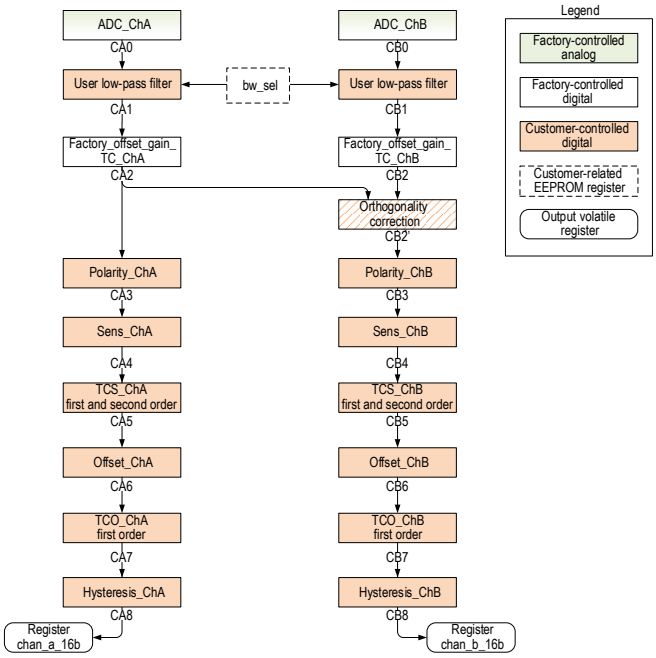

Figure 1: Signal Propagation Per Channel

Filter Signal Delay

A large contributor to the signal delay in the A31315 sensor is the filter setting programmed in the sensor EEPROM.

Signal blocks that relate to the filter settings are shown in Figure 2.

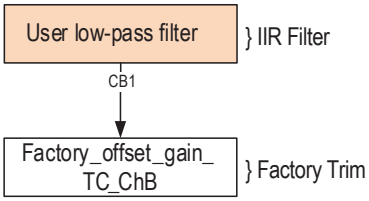

Figure 2: Signal Path Blocks Representing Group Delay

The factory trim block is not customer-programmable; however, the infinite impulse response (IIR) filter is customer-programmable for different bandwidths. These two delay values, which represent the filter calculations and signal processing, are considered together as the group delay (t_{group}). The IIR filter calculation represents the majority of the signal path delay calculation and thus contributes the most to the mechanical angle output delay. Because the IIR filter is user-programmable, the signal delay can be adjusted based on application needs; however, the IIR filter calculation will continue to occupy considerable processing time and will remain a major contributor to the signal delay.

Bandwidth-select filter parameter (bw_sel_filter) information from the A31315 datasheet is shown in Table 1. A change to the filter bandwidth will change the filter delay period. This changes the filter response profile, which affects the overall system signal delay.

Table 1: Settings for Bandwidth-Select Filter

bw_sel_filter	3 dB Frequency (Hz)
0	329.1
1	465.8
2	556
3	700
4	1000
5	1482
6	2024
7	Adaptive

Simulation results for the group delay curves for different bandwidth selections based on the bw_sel_filter register parameter are plotted in Figure 3. As shown, the lower the bandwidth, the higher the group delay: at 329.05 Hz (bw_sel_filter = 0), the delay exceeds 1000 µs; whereas, at 2024.1 Hz (bw_sel_filter = 6), the delay is slightly less than 200 µs.

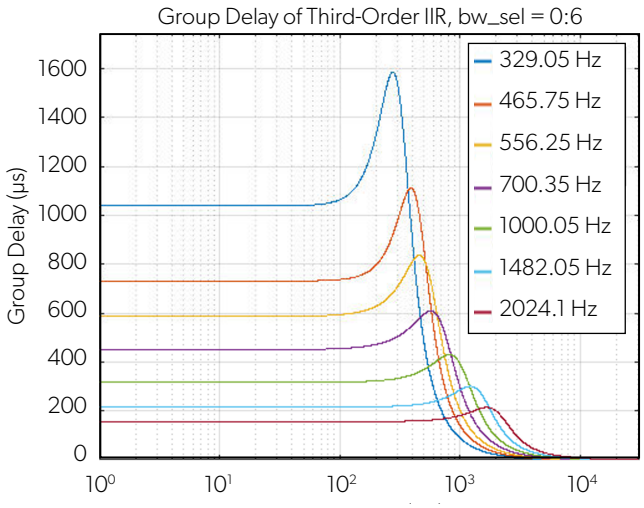

Figure 3: Simulated Value of Group Delay Over Bandwidth

The simulated filter response curve, however, is similar for all bw_sel_filter settings: for frequencies below their respective fc settings, there is a constant delay; for frequencies increasing from the fc setting, there is peak bell-shaped delay. The adaptive filter (bw_sel_filter = 7) alters the filter response, which enables new points for design freedom.

Selection of the adaptive filter setting (bw_sel_filter = 7) frees the following filter settings in registers 0x37 and 0x38:

- bw_adapt_exp (exponential gain of the feed-forward adaptive filter loop)
- bw_adapt_frac (fractional gain of the feed-forward adaptive loop)
- bw_adapt_delay (number of clock cycles at 8 MHz delay before the adaptive filter bandwidth decreases)
- bw_adapt_max (maximum bandwidth of the filter)
- bw_adapt_min (minimum bandwidth of the filter)

For more information regarding the parameters and EEPROM settings, refer to the A31315 datasheet. [1]

[1] https://www.allegromicro.com/en/products/sense/linear-and-angular-position/3d-magnetic/a31315

The different bits that can be set for bw_adapt_min and bw_adapt_max are presented in Table 2. As shown, the bandwidth can be decreased to 38.9 Hz or increased to 4734.2 Hz using the adaptive filter. By choosing the same value for both parameters, the bandwidth would be constant, thus dictating the cut-off frequency of the filter.

Table 2: LSB Values for bw_adapt_min/bw_adapt_max

bw_adapt_(min/max) (LSB)	Frequency (Hz)
0	38.9
1	77.8
2	156.3
3	314.8
4	638.7
5	1308.6
6	2672.1
7	4734.2

The simulation result for a signal group delay with adaptive filter versus frequency is plotted in Figure 4. In this mode, the group delay for bandwidths between 4000 Hz and 5000 Hz is 110 µs. By comparing Figure 3 with the adaptive filter data from Figure 4, the group delay can be reduced, which can enable use of increased bandwidth. Further testing is needed, however, to ensure optimal sensor performance.

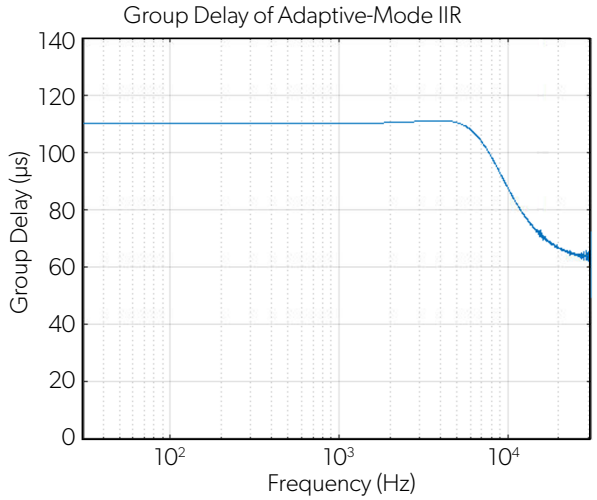

Figure 4: Filter Response Using Adaptive Settings

Customer Trim and Hysteresis Signal Delay

The second part of the delay per channel is the customer trim and hysteresis. These fields take into consideration all the customer-programmable optimization parameters for each channel, such as temperature, polarization, and offset compensation. These processing blocks typically consume less than 10% of the overall in-chip processing time.

ANGLE SIGNAL PROCESSING DELAY

After each channel is processed, both channels are combined inside a chain of functional blocks. These blocks perform final adjustments to the signal before the angle is output.

The last blocks that are required to determine the angle are shown in Figure 5. After the signal crosses these functional blocks, the angle is output as a 16-bit value.

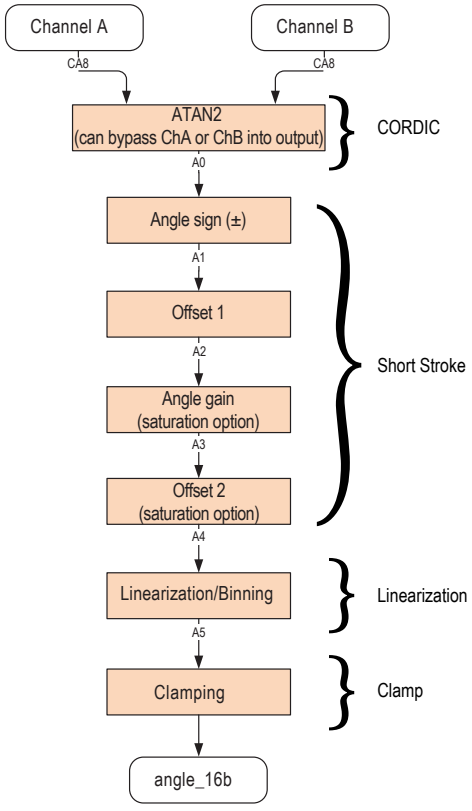

Figure 5: Final Signal Processing Blocks

CORDIC Signal Delay

The CORDIC calculation block applies an arctangent operation to both channels, thus calculating an angle from both channels. After this process completes, raw angle A0 is formed. This process spans 2 µs. Bypassing the CORDIC through customer settings limits the A31315 to a one-dimensional sensor, but also removes the CORIDIC calculation time. A delay of 0.25 µs is still added as part of the bypass circuitry.

Short Stroke, Linearization, and Clamping Signal Delay

Based on customer-specified settings, especially linearization, the signal delays of the last blocks may differ. The different linearization schemes that can be defined in EEPROM registry 0x21 are shown in Table 3. Based on the different customer-programmable linearization schemes, the signal delays may differ; variable segment linearization mode has the longest delay.

Table 3: Linearization Schemes

lin_set Code	Output Transfer Function Option
0	Fixed Segment Linearization
1	Fixed Segment Binning Mode
2	Variable Segment Linearization Mode
3	Variable Segment Binning Mode

In variable segment linearization mode, all of the angle signal-processing functional blocks—from CORDIC calculations until clamping—span ~6 µs; in fixed segment linearization mode, the functional blocks span ~2 µs. Filter response delay is, thus, concluded to be the largest contributor to the in-chip delay.

TRANSMISSION DELAY

SENT Output Delay

After the 16-bit angle is processed inside the chip, the message must be transmitted through the output pin. An estimate of the transmission delay for the SENT protocol can be calculated.

The SENT message components—synchronization, status, six data nibbles, and one CRC nibble—are shown in Figure 6. When an additional "pause" message is added, the number of ticks per message is constant. The A31315 sensor can output using the SENT protocol with a tick time between 0.25 µs and 10 µs (tick times below 0.5 µs are not recommended). The SENT frame rates used, with different settings to define the length of the SENT message, are shown in Table 4.

Table 4: sent_frame_rate Definition

sent_frame_rate	Frame Rate Including Pause Pulse
0	3 data nibbles: frame length 210 t_{tick} 4 data nibbles: frame length 228 t_{tick} 6 data nibbles: frame length 282 t_{tick}
1	0.5 ms
2	1.0 ms
3	2.0 ms

When using SENT without the pause pulse, i.e., dig_out_sel = 1, the data transfer duration is dependent on the value that is transmitted, which results in variations in the transfer duration.

When using SENT with a pause pulse, i.e., dig_out_sel = 2, the transfer duration is fixed, and a pause pulse will be added after data transmission to ensure that each SENT message reaches the defined duration, thus taking a pre-defined number of ticks per transferred message. Assuming six data nibbles, similar to Figure 6, the estimated worst-case transmission time using SENT with a pause pulse would be 0.914 ms using t_{tick} = 3.24 µs (3 µs target plus 8% deviation); for the best-case scenario with t_{tick} = 0.5 µs, message transmission would take 0.141 ms.

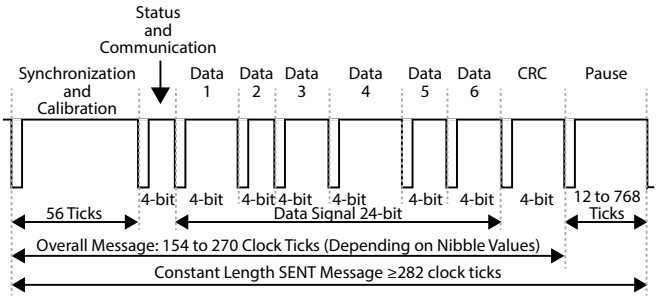

Figure 6: SENT Message Description

Analog Output Delay

When using the analog interface, the 16-bit angle is processed through a digital-to-analog converter and an analog driver to provide a voltage output relative to the angle data. In this case, the delay associated with the interface is simply that of the response time of the analog circuit. The analog response time for the A31315 is estimated to be a maximum of 600 µs. If further filtering is required by external circuitry, the response time of the additional filter stages must be taken into account as well.

CONCLUSION

The filter delay is the largest in-chip delay element in the A31315 3-D position sensor, contributing to at least 90% of the calculated delay time, and different signal delays are expected with different bandwidths. When the SENT protocol is used with a pause signal, with t_{tick} = 3.24 µs, a transmit delay can be in the range of 0.9 µs, which is approximately eight times the in-chip signal delay of the adaptive filter.

The best- and worst-case scenarios for the low-pass filter operation and transmission are shown in Table 5.

Table 5: Best-Case/Worst-Case Low-Pass Filter Comparison

Component	Best Case	Worst Case
Filter	110 µs	1050 µs
SENT Interface	141 µs	914 µs
Analog Interface	–	≤600 µs

Considering the best-case EEPROM, the signal delay from the Hall plate to the output pin—consisting of filter (~110 µs), channel processing blocks (~11 µs), angle calculation blocks (~2 µs), transmission delay (141 µs, given the optimal case for SENT output with t_{tick} = 0.5 µs; this delay is 600 µs for the analog output)—the best-case signal delay in the A31315 sensor would span ~264 µs using the SENT protocol, compared to 723 µs using the analog output.

Considering the worst-case settings, the signal delay would be 2.0 ms using the SENT output protocol and 1650 µs using the analog output protocol.

Revision History

Number	Date	Description	Responsibility
–	July 13, 2022	Initial release	A. Halawani

955 PERIMETER ROAD • MANCHESTER, NH 03103 • USA
+1-603-626-2300 • FAX: +1-603-641-5336 • ALLEGROMICRO.COM