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MOTOR DRIVE DISCRETE MOSFET BRIDGE CIRCUIT DESIGN AND LAYOUT

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Introduction

This application note is intended to familiarize the reader with bridge circuit switching for motor drive applications. Recommendations for circuit design and layout to mitigate EMI and switching transients are provided.

Bridge Circuit Switching Transients

Figure 1 shows the power section of a half-bridge discrete MOSFET design. Typically during operation, Q_H and Q_L are alternately enabled to regulate the current in the inductive motor winding.
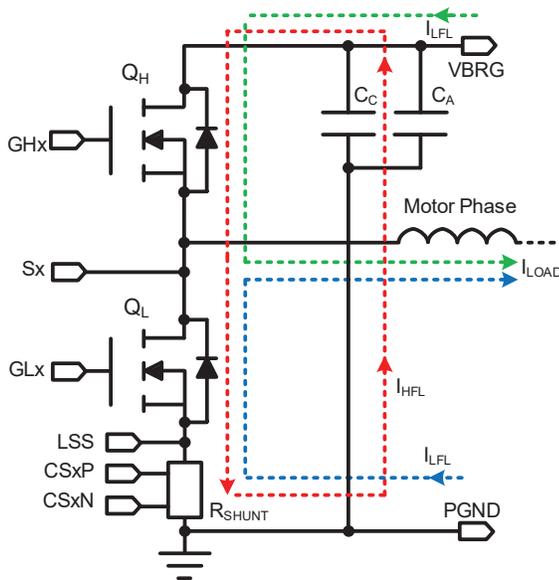

Figure 1: Power section of half-bridge discrete MOSFET design

The blue and green I_{LFL} current paths illustrate the case when the flow of current is unidirectional into the motor phase during the PWM cycle. For an initial state, assume that Q_L is on, synchronously rectifying the current recirculating around the bottom of the half bridge. When transitioning from Q_L to Q_H conducting, both drivers will typically be in the off state during the dead time, and the body diode of Q_L will forward bias for a short time to conduct the load current.

When Q_H is enabled the motor phase voltage will transition high, but during the transition, in addition to sourcing the load current, Q_H must also source enough current to recover the low side body diode, and charge any parasitic capacitance including the MOSFET intrinsic capacitances.

This additional high-frequency loop current, I_{HFL}, primarily flows from the local ceramic decoupling capacitor C_C, through the power transistors and gate driver circuitry to ground. The aluminum electrolytic capacitor, C_A, although larger in value, also has much higher parasitic inductance and resistance and primarily functions to replenish charge on C_C and provide supply decoupling for the lower frequency load current loops. The high di/dt of the high frequency loop current and resulting energy stored in the parasitic inductance of the circuit components and PCB routing, can result in phase voltage overshoot which can exceed the absolute maximum ratings of the gate drive circuitry if not mitigated.

Also, because power stage in Figure 1 has very little resistance, the parasitic inductance and capacitance form a high Q resonant circuit that can ring for many cycles if overshoot is present.

For the example in Figure 1, where current is into the motor phase, ringing will also be present when the phase voltage goes low. On the falling transition, without the body diode recovery current, there is less risk of excessive voltage overshoot.

Although the example in Figure 1 illustrates the case when the low-side body diode is forward biased, there is an analogous case where the high-side body diode will forward bias when current is flowing out of the motor phase.

To limit the amount of overshoot and ringing, there are several preventative measures that can be taken:

1. Each half-bridge high-frequency power switching loop, shown in red in Figure 1, should have a PCB layout that minimizes the parasitic inductances around the loop and includes appropriate ceramic capacitors to decouple the supply voltage.

2. To reduce EMI and high voltage overshoot, snubber circuits should be used to dampen excessive motor phase ringing.

3. The driver turn-on rate when recovering body diode conduction should be limited to prevent excessive phase voltage overshoot. For gate drivers that have internally programmable current gate drive, the gate turn-on current can be set to control the switching transients. Series gate resistors, which allow a limited degree of cross conduction, are an alternative effective method to control switching voltage transients.

4. Additional circuitry can be added to protect the gate driver if required.

These items will be covered in more detail in the subsequent text. Controlling the bridge voltages in a high-power 48-volt system can be challenging. To ensure a robust design, the absolute voltages of the gate drive circuitry should not be exceeded. The terminal voltages present on the gate driver should be measured with a tip and barrel (spring clip) close to the gate driver. When measuring the terminal voltages, the time base of the oscilloscope should be short enough to observe the peak voltages of the high-frequency transients. The voltage transients should be verified over the full temperature range, as they are often worst case at cold temperature.
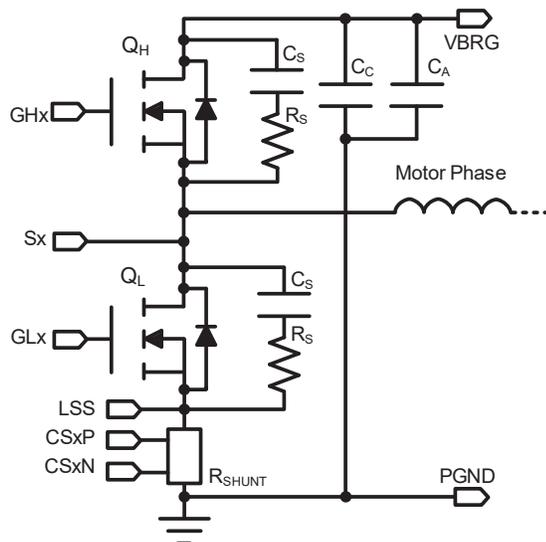
Bridge Circuit Layout

Figure 2 : Bridge Circuit Layout

In Figure 2, snubber networks have been added across the power transistors to reduce EMI. Figure 3 shows an example of component placement and top-level PCB metal pattern for the half bridge in Figure 2. The components have been

placed to minimize the stray inductance and resistance around the high frequency current loop, marked with the red dashed line.
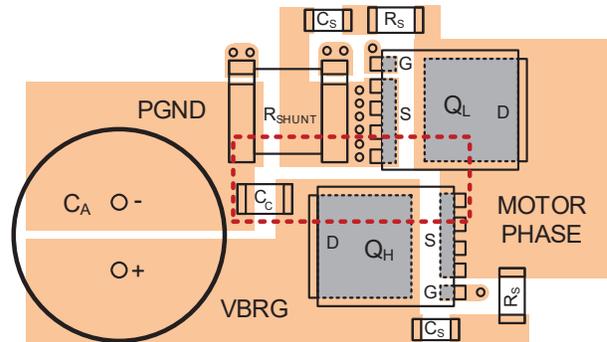

Figure 3: PCB Layout

Recommendations for the half bridge layout are:

1. Arrange Q_L, Q_H, R_{SHUNT} and C_C in a tight loop, because the parasitic loop inductance is a function of total loop distance.

2. Use wide PCB traces for the loop connections to minimize inductance and resistance and help dissipate device heating.

3. Assuming a 4-layer PCB, PGND, and VBRG should be connected to an internal PCB power ground and supply plane. These connections should be made with numerous vias to carry the phase current and help with thermal power dissipation.

4. The top-level metal pattern for the power loop should be duplicated on the bottom side of the PCB. These top and bottom metal patterns should be connected with numerous vias to carry the phase current and help with thermal power dissipation.

5. The snubber network connections should be made with short wide traces to reduce EMI and minimize parasitic inductance. Connections directly to the power and ground planes should be avoided.

6. If more than one ceramic capacitor is used for C_C, they should be placed as close together as possible to avoid forming a resonant LC circuit between the capacitors. Typical values of C_C are in the range of 2.2 to 4.7 µF. The capacitance voltage and temperature coefficient should be considered when selecting the value of C_C.

7. The half bridge layout can be replicated for other motor phases. To avoid potential interactions between half bridges the PGND and VBRG connections should be made to the internal power planes and not connected on the top and bottom PCB layers.

Snubber Network Design

Assuming the snubber networks are not present in the circuit in Figure 2, the frequency of the motor phase voltage ringing is given by:

Equation 1: $$f_R = \frac{1}{2\pi\sqrt{L_P \times C_P}}$$

where L_P and C_P are the equivalent sum series parasitic inductance and capacitance of the power output stage. For the snubber network to be effective in dampening ringing, C_S needs to be several times greater than C_P. To reduce phase voltage overshoot, the required value of C_P can be considerably higher depending on the speed of the output switching and body diode reverse recovery characteristics.

In practice, it is difficult to calculate the exact values of L_P and C_P from device specifications and examination of the PCB layout. A practical way to determine the value of C_P is to add a known additional capacitance, C_A, to the half-bridge output and observe the change in ringing frequency.

Since most of the parasitic capacitance is due to the MOSFET output capacitance, a reasonable value to select C_A is to use roughly four times the value of the MOSFET output capacitance, C_{OSS}. The exact value is not critical, but it must be large enough to observe an appreciable shift in frequency when added to the circuit.

For the snubber capacitors, C_S, it is best to use a low temperature and voltage coefficient ceramic capacitor to achieve consistent snubbing performance across operating conditions.

If the PCB has been laid out to accommodate snubber components, R_S can be replaced with a zero-ohm jumper and C_A can be fitted in both C_S locations.

By measuring the change in the ringing frequency from the original circuit, f_R, to the added capacitance case, f_{RA}, the approximate value of parasitic capacitance can be calculated as:

Equation 2: $$C_P = \frac{C_A}{\frac{f_R^2}{f_{RA}^2} - 1}$$

Once C_P is known, the value of the parasitic inductance can be approximated as:

Equation 3: $$L_P = \frac{1}{C_P \times (2\pi f_R)^2}$$

And first estimates for snubber network components can be calculated as:

Equation 4: $$R_{SN} = \sqrt{\frac{L_P}{C_P}}$$

Equation 5: $$C_{SN} = \frac{1}{\pi \times R_{SN} \times f_R}$$

The power dissipation of the snubber resistors can be estimated as:

Equation 6:
$$P_{R_{SN}} = f_{PWM} \times C_{SN} \times (2 \times (V_{VBRG} + V_{OS})^2 - (V_{VBRG})^2)$$

where f_{PWM} is the motor phase PWM switching frequency, V_{OS} is the value of any residual overshoot voltage, and the output is assumed to always be active. If there is no voltage overshoot this equation simplifies to:

Equation 7: $$P_{R_{SN}} = f_{PWM} \times C_{SN} \times V_{VBRG}^2$$

Once the calculated component values for C_{SN} and R_{SN} have been fitted to the PCB, some further tuning may be needed to improve performance. If the circuit is under-damped, increasing the resistance or capacitance will increase the dampening. If there is voltage overshoot present, and the design uses a gate drive turn-off that is considerably stronger that the gate drive turn-on, increasing C_{SN} while reducing R_{SN} can reduce the overshoot.

Gate Drive Control Methods

Gate drivers are typically designed to drive a wide range of MOSFET devices that have dissimilar gate charge. Figure 4 shows an example of excessive overshoot and ringing that can occur when a high-current gate driver is used to drive a low-capacitance MOSFET.
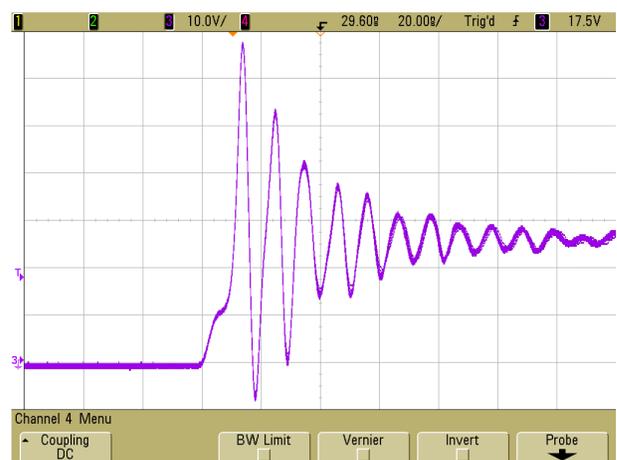

Figure 4: Example of excessive overshoot and ringing

In Figure 4, although the supply voltage is only 25 volts, the output voltage at turn on reaches nearly 70 volts. For this case, the rapid turn-on of the high-side MOSFET results in a very high peak body diode recovery current of the low-side MOSFET, which energizes the parasitic inductance, creating the excessive overshoot and ringing. For the test condition in Figure 4, no snubbing is present in the circuit.

Figure 5

To better control MOSFET switching, many of the drivers manufactured by Allegro MicroSystems allow the user to program the gate drive current through SPI. Figure 5 shows same circuit as Figure 4, but in this case the gate driver has been programmed to reduce the gate charging current during the initial high-side MOSFET turn-on and then boost the drive current near the end of the switching to rapidly enhance the MOSFET. With the slower initial turn-on, the peak diode recovery current is reduced, eliminating the overshoot entirely. No snubbers or series gate resistors are used for this case.
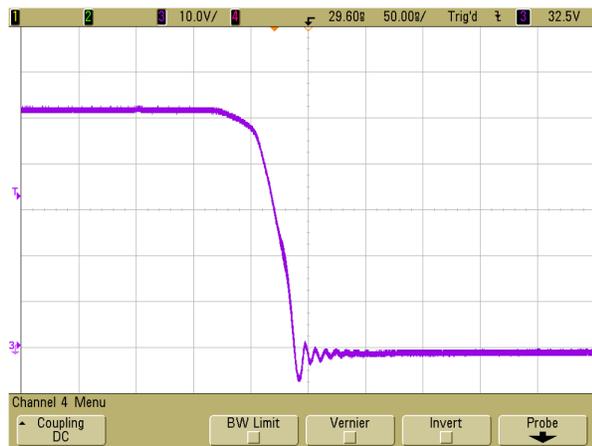

Figure 6

In Figure 6, the programmable current gate drive of the gate

driver controls the high side MOSFET turn-off during the negative output transition. The controlled gate discharge results in acceptable overshoot and minimal ringing that can be further reduced with the addition of snubber networks.

Figure 7

In Figure 7, the gate driver is still the driving device, but the current-limited gate drive is disabled, and 22-ohm series gate resistors have been added to the high- and low-side MOSFETs. Compared to Figure 4, the series gate resistor has increased the turn on time from 10 to 30 ns and the overshoot is well controlled. If series gate resistors are used, to obtain similar results, the resistor value can be adjusted depending on the chosen MOSFET characteristics, keeping in mind the absolute maximum ratings of the gate driver and other circuit components. Snubber circuits are typically added to help reduce EMI due to output ringing.

Figure 8

Figure 8 provides some additional insight on the effect of using series gate resistors. The yellow and green traces are the gate and source of the low side MOSFET, and the pink

trace is the difference between these traces, the V_{GS} of the low side MOSFET. When gate resistors are used, the MOSFET in the off-state, in this case the low-side MOSFET, will partially turn on during switching transition, which helps to limit output overshoot at the expense of some cross conduction loss.

Gate Driver Protection Circuitry

For some 48-volt designs with high switching speed requirements, if after optimizing the PCB layout, gate drive, and snubber design, there are still excessive voltages on the gate driver terminals, additional circuitry may be needed to protect the gate driver.

For the circuit in Figure 9, R_1 has an impedance of 2 to 4 ohms and effectively decouples the motor phase from the S_X node of the gate driver so that the clamping circuit can limit the voltage on the gate driver S_X and C_X terminals.

The breakdown voltage of D_1 should be chosen to turn on Q_1 to clamp the S_X node voltage at less than the maximum rating of the S_X terminal. C_1 and R_2 act to keep Q_1 off during normal switching transients. Diode D_2 can be chosen to allow S_X to be clamped at a negative voltage by conduction through the body diode of Q_1.
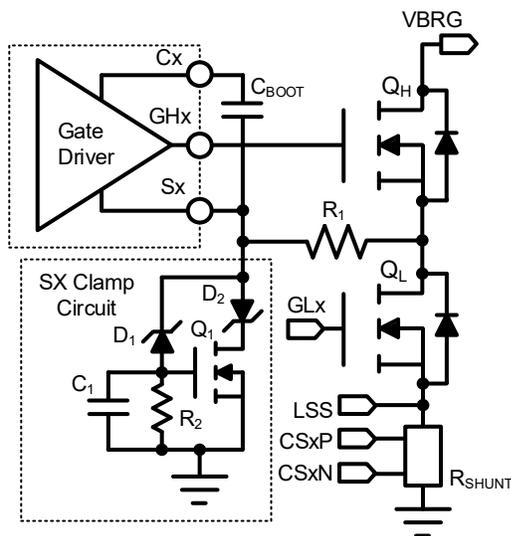
During negative switching transients, because G_{HX} is driven with respect to S_X, the S_X negative clamp voltage will effectively allow Q_H to remain conductive clamping the phase node at a negative voltage given by:

Equation 8:

$$V_{CLNEG} = - (V_{D2BV} + V_{BDQ1} + V_{GSQH})$$

Other shared clamp configurations are possible when R_1 is included. For information regarding gate drivers that are compatible with resistance added in series with S_X, refer to specific device documentation or contact the applications support team.

Figure 9 : Gate driver protection circuitry

Revision History

Number	Date	Description	Responsibility
–	November 19, 2020	Initial release	A. Wood

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