Wide Input Voltage, Adjustable Output, Synchronous Buck Controller with PWM Frequency Dithering, Synchronization, and NPOR

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Wide operating voltage range: 3.0 to 45 V
- Adjustable output voltage
- PWM frequency dithering reduces EMI/EMC signature and minimizes input filtering
- Programmable base frequency (f_{OSC}): 200 kHz to 2.2 MHz
- For low frequency, high current designs (<520 kHz), applying a clock to $SYNC_{IN}$ will synchronize the PWM frequency to avoid AM band harmonic interference
- Soft recovery from dropout avoids overshoot of V_{OUT}
- External compensation provides flexibility to tune the system for maximum stability or optimum transient response
- Adjustable soft-start time controls inrush current to accommodate a wide range of output capacitances
- Pre-bias startup allows quick, monotonic restart and avoids reset
- High-voltage ENBAT input for ignition/key control
- Logic enable (EN) input for microcontroller or DSP control
- NPOR open-drain output with adjustable rising delay
- Overvoltage, pulse-by-pulse current limit, hiccup mode short circuit, and thermal protections
- Robust FMEA: pin open/short and component faults

APPLICATIONS

- Infotainment
- Navigation systems
- Instrument clusters
- Audio systems
- ADAS applications
- Battery-powered systems
- Industrial systems
- Network and telecom
- Home audio
- HVAC systems

DESCRIPTION

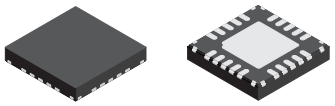
Designed to satisfy the power supply requirements of automotive, industrial, and consumer applications, the A8660 includes all the control and protection circuitry to produce a robust PWM controller delivering high current.

The A8660 includes PWM frequency dithering, which has been shown to reduce EMI/EMC. A soft recovery feature prevents output voltage overshoot when the converter comes out of a low VIN dropout condition. For high current, low frequency designs (<520 kHz), an external clock can be applied to the $SYNC_{IN}$ pin to shift the PWM harmonics, thus avoiding AM band interference with a tuner or other sensitive electronics.

The A8660 has external compensation so it can be tuned to satisfy various system goals over a wide range of PWM frequencies and external components. It includes adjustable soft start to minimize inrush current. Additionally, it monitors the feedback voltage to provide an open-drain NPOR signal with adjustable delay time.

Extensive protection features of the A8660 include pulse-by-pulse current limit, hiccup mode short-circuit protection, BOOT open/short voltage protection, VIN undervoltage lockout, V_{OUT} overvoltage protection, and thermal shutdown. The A8660 is supplied in a low profile 20-pin QFN package (suffix "ES") with exposed power pad.

PACKAGE:



20-pin 4 × 4 mm QFN (ES) with wettable flank

Not to scale

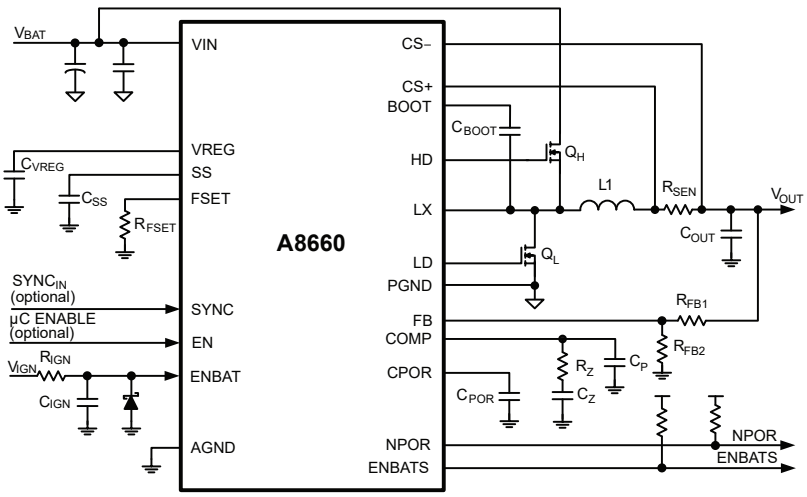


Figure 1: Typical Application Schematic

SELECTION GUIDE

Part Number	Temperature Range	Packing [1]	Package
A8660KESTR-J	–40°C to 150°C	1500 pieces per 7-inch reel	20-pin QFN with thermal pad and wettable flank

[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]: with respect to ground, unless otherwise noted

Characteristic	Symbol	Notes	Rating	Unit
VIN, SS, EN, ENBAT	V_{VIN}, V_{SS}, V_{EN}, V_{ENBAT}		–0.3 to 50	V
BOOT, HD	V_{BOOT}, V_{HD}		–0.3 to V_{VIN} + 9	V
LX	V_{LX}	continuous	−0.6 to V_{VIN} + 1	V
		t < 50 ns	–2 to V_{VIN} + 3	V
LD, VREG	V_{LD}, V_{VREG}		–0.3 to 9	V
CS+	V_{CS+}	With respect to CS–	–0.5 to 0.5	V
CS+, CS–, FB	V_{CS+}, $V_{CS–}$, V_{FB}		–0.3 to 22	V
FSET, NPOR, CPOR, COMP, ENBATS	V_{FSET}, V_{NPOR}, V_{CPOR}, V_{COMP}, V_{ENBATS}		–0.3 to 6.5	V
Junction Temperature Range	T_J(max)		–40 to 150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	QFN-20 (ES) package, 4-layer PCB based on JEDEC standard	37	°C/W
	$R_{\theta JC}$	QFN-20 (ES) package, Junction to thermal pad	2	°C/W

[3] Additional thermal information available on the Allegro website.

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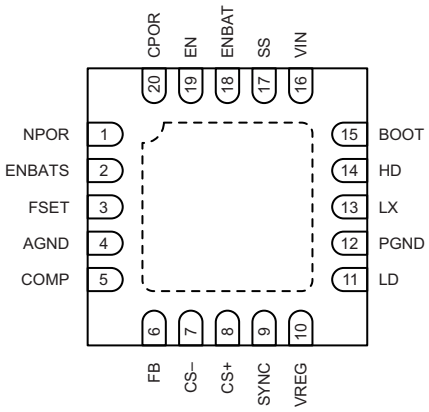
PINOUT DIAGRAM AND TERMINAL LIST



Package ES, 20-Pin QFN Pinout Diagram

Terminal List Table

Number	Symbol	Function
1	NPOR	Open-drain “power-good” output with programmable rising-delay. A logic low at this pin indicates the voltage at the FB pin is not within regulation. The NPOR delay is programmable via the CPOR pin. An external pull-up resistor must be provided if this pin is used by the system.
2	ENBATS	Open-drain output pin indicating the status of the ENBAT pin. An external pull-up resistor must be provided if this pin is used by the system.
3	FSET	Connect a resistor from this pin to ground to set the base PWM oscillator frequency (f_{OSC}). See the applications section for an R_{FSET} versus PWM oscillator frequency equation and graph.
4	AGND	Analog ground pin. Refer to the PCB layout section for further information on grounding.
5	COMP	Error amplifier output pin. There must be a compensation network (R_Z, C_Z, C_P) connected to this pin to stabilize the current control loop.
6	FB	Negative input pin of the error amplifier. Connect this pin to the output of a resistor divider from V_{OUT} to ground to set the converter output voltage.
7	CS–	Negative input to the current sense amplifier.
8	CS+	Positive input to the current sense amplifier.
9	SYNC	External synchronization input pin. Applying an external clock to this pin forces synchronization of the internal oscillator to the external clock frequency for low frequency designs (<520 kHz). If this pin is not used, it has an internal pull-down resistor so it can be left open or connected to ground.
10	VREG	Internal voltage regulator bypass capacitor pin. The voltage at this pin is the main supply for the both the internal circuitry and the low-side gate drive (LD). A 1 µF ceramic capacitor should be connected from this pin to ground.
11	LD	Low-side gate driver output. Drive is taken from VREG with respect to ground.
12	PGND	Power ground. Refer to the PCB layout section for further information on grounding.
13	LX	Switching node for the external MOSFETs and output inductor. Also, this pin is the reference for the BOOT supply.
14	HD	High-side gate driver output. Drive is taken from BOOT with respect to LX.
15	BOOT	High-side gate drive supply input. A quality ceramic capacitor should be connected from this pin to LX.
16	VIN	Input supply voltage. This pin should be bypassed by several high-quality ceramic capacitors chosen to address various frequencies. Refer to the applications section for additional details.
17	SS	Soft-start timing adjustment pin. A capacitor connected to this pin defines the rise time of the output voltage either at start-up, low VIN soft recovery, or recovery from an overload.
18	ENBAT	Enable input from an ignition key switch. An R-C low-pass filter, as shown in the Recommended Applications Schematic, should be used if this pin is connected to VBAT via a key switch. This pin is rated for 50 V maximum. Connect this pin to ground if unused.
19	EN	Logic-enable input from a microcontroller or DSP. If this pin is not used, it must be connected to ground. This pin is rated for 50 V maximum.
20	CPOR	NPOR rising-delay programming pin. A capacitor connected to this pin defines the NPOR rising delay at start-up or recovering from a fault.
–	PAD	Exposed pad of the package. Provides optimal thermal performance when connected to the ground plane(s) of the PCB using multiple vias.

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Block Diagram / Typical 3.3 V, 5 A, 2.2 MHz Applications Schematic

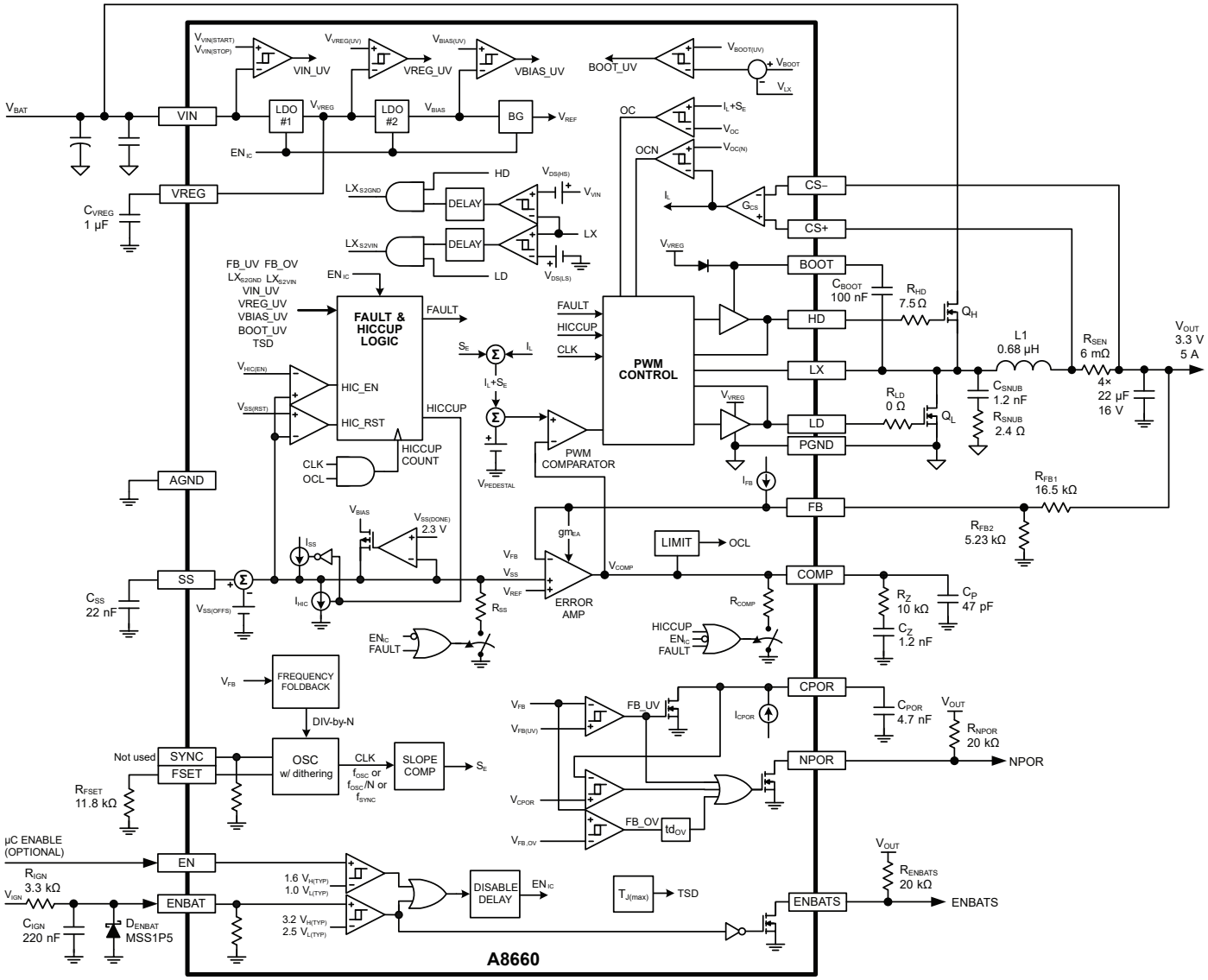

Figure 2: High Frequency Design Example: 12 V_{IN}, 3.3 V_{OUT}, 5 A at 2.2 MHz

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Typical 5 V, 10 A, 410 kHz Applications Schematic

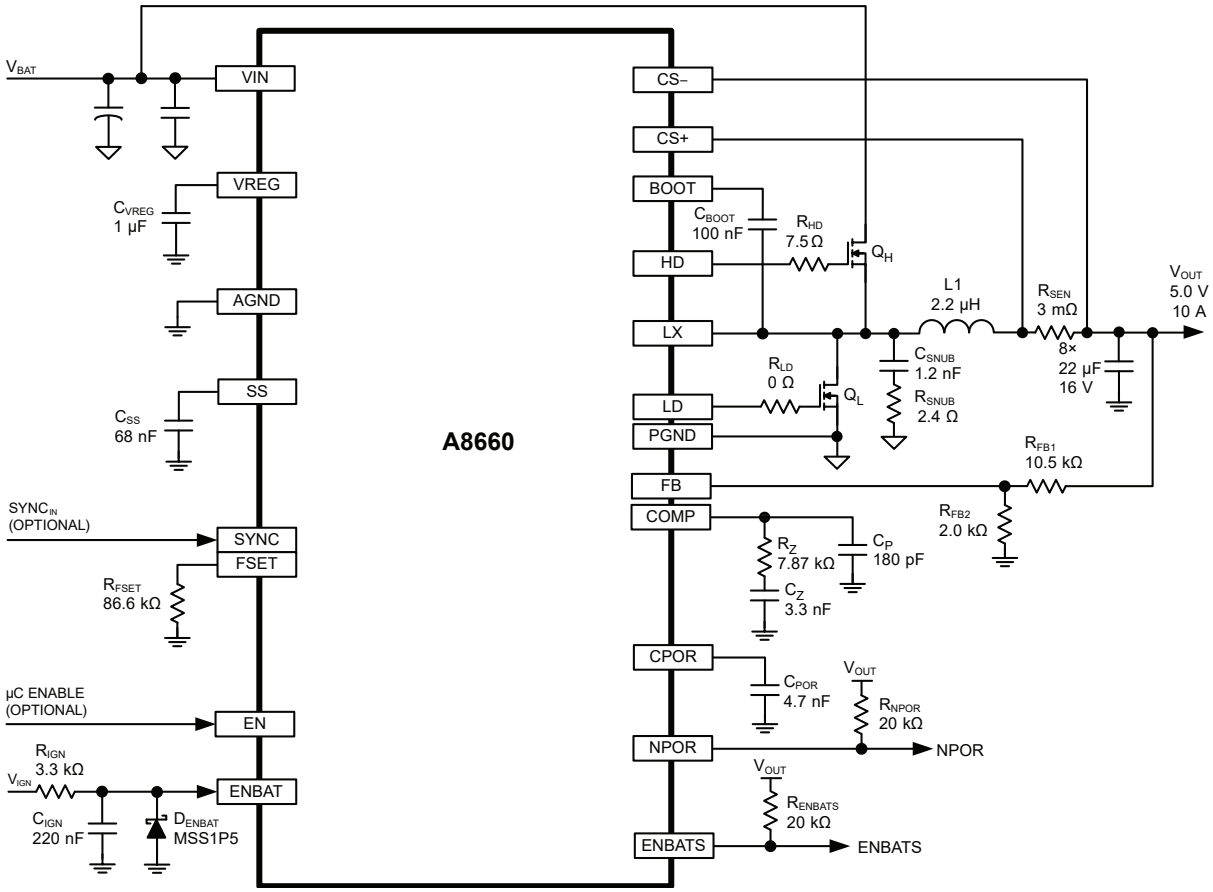

Figure 3: Low Frequency Design Example: 12 V_{VIN}, 5 V_{OUT}, 10 A at 410 kHz

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ELECTRICAL CHARACTERISTICS: Valid at V_{VIN} = 13 V, –40°C ≤ T_J ≤ 150°C, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
INPUT VOLTAGE SPECIFICATIONS (VIN)						
Input Voltage Range	V_{VIN}	V_{VIN} must first rise above $V_{UVLO(START,MAX)}$	3.0	–	45	V
VIN UVLO Start	$V_{VIN(START)}$	V_{VIN} rising	3.1	3.4	3.7	V
VIN UVLO Stop	$V_{VIN(STOP)}$	V_{VIN} falling	2.3	2.6	2.9	V
VIN UVLO Hysteresis	$V_{VIN(HYS)}$	$V_{VIN(START)} – V_{VIN(STOP)}$	–	800	–	mV
INPUT SUPPLY CURRENT						
Input Sleep Current [1][3]	$I_{VIN(SLEEP)}$	T_J = 25°C, $V_{EN} = V_{ENBAT}$ = LO, V_{FB} < 200 mV	–	2	10	µA
Input Current, PWM Mode [1]	$I_{VIN(PWM)}$	V_{EN} = HI, V_{FB} = 0.8 V, V_{COMP} = 0 V	–	2.5	5.0	mA
REGULATION ACCURACY (FB PIN) AND OUTPUT VOLTAGE						
Feedback Voltage Accuracy	V_{FB}	T_J = 150°C, $V_{FB} = V_{COMP}$	792	800	808	mV
		$V_{FB} = V_{COMP}$	784	–	816	mV
Output Voltage Setting Range [2]	V_{OUT}		0.8	–	20	V
SWITCHING FREQUENCY AND DITHERING (FSET PIN)						
Switching Frequency	f_{OSC}	R_{FSET} = 11.8 kΩ	1.96	2.2	2.5	MHz
		R_{FSET} = 86.6 kΩ	–	410	–	kHz
Frequency Dithering	Δf_{OSC}	As a percent of f_{OSC}	–	±10	–	%
Dithering Modulation Frequency [3]	f_{MOD}		9	12	15	kHz
PULSE-WIDTH MODULATION (PWM) TIMING AND CONTROL						
Minimum Controllable On-Time	$t_{ON(MIN)}$		–	70	90	ns
Minimum Off-Time	$t_{OFF(MIN)}$		–	85	150	ns
Current Sense Amplifier Gain	G_{CSA}		–	7.5	–	V/V
Slope Compensation [3]	S_E	Measured at the input to the current sense amp and from $t_{ON(MIN)}$ to $t_{ON(MAX)}$	–	16	–	mV
MOSFET GATE DRIVERS (HD, LD)						
High-Side Driver, Source Current	$I_{HD(SRC)}$	$V_{BOOT} – V_{LX}$ = 5.6 V, V_{HD} = 1.5 V	–	0.8	–	A
High-Side Driver, Sink Current	$I_{HD(SINK)}$	$V_{BOOT} – V_{LX}$ = 5.6 V, V_{HD} = 1.5 V	–	1.5	–	A
Low-Side Driver, Source Current	$I_{LD(SRC)}$	V_{VREG} = 6.3 V, V_{LD} = 1.5 V	–	2.0	–	A
Low-Side Driver, Sink Current	$I_{LD(SINK)}$	V_{VREG} = 6.3 V, V_{LD} = 1.5 V	–	1.8	–	A
MOSFET PROTECTIONS						
High-Side Current Limit	$I_{LIM(HS1)}$	$t_{ON} = t_{ON(MIN)}$	50	70	90	mV
	$I_{LIM(HS2)}$	$t_{ON} = t_{ON(MAX)}$ [3]	–	54	–	mV
Low-Side Current Limit	$I_{LIM(LS)}$	$t_{ON} = t_{ON(MIN)}$	–	–12	–	mV
High-Side Protection Voltage	$V_{DS(HS)}$	LX node shorted to GND, $V_{VIN} – V_{LX}$	–	390	–	mV
Low-Side Protection Voltage	$V_{DS(LS)}$	LX node shorted to VIN, $V_{LX} – V_{GND}$	–	420	–	mV

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ELECTRICAL CHARACTERISTICS (continued): Valid at V_{VIN} = 13 V, –40°C ≤ T_J ≤ 150°C, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Synchronization Input ($SYNC_{IN}$ Pin)						
Synchronization Frequency Range	$f_{LX(SYNC)}$	$f_{OSC(TYP)}$ ≤ 666 kHz	1.2 × $f_{OSC(TYP)}$	–	1.5 × $f_{OSC(TYP)}$	–
Maximum Synchronization Frequency [3]	$f_{SYNC(MAX)}$	$f_{OSC(TYP)}$ = 666 kHz	–	–	1.0	MHz
$SYNC_{IN}$ Pulse Width	$t_{PW(SYNC)}$		200	–	500	ns
$SYNC_{IN}$ Rise/Fall Time [3]	$t_{R/F(SYNC)}$		–	–	15	ns
$SYNC_{IN}$ Voltage Thresholds [3]	$V_{SYNC(HI)}$	$V_{SYNC(IN)}$ rising	–	1.6	2.0	V
	$V_{SYNC(LO)}$	$V_{SYNC(IN)}$ falling	0.8	1.1	–	V
ERROR AMPLIFIER (COMP PIN)						
Feedback Input Bias Current [1]	I_{FB}	V_{FB} = 800 mV	–40	–	–12	nA
Open-Loop Voltage Gain	A_{VOL}		–	65	–	dB
Transconductance	gm	V_{FB} > 400 mV	550	750	950	µA/V
		0 V < V_{FB} < 400 mV	275	375	475	µA/V
Output Current	I_{COMP}		–	±75	–	µA
COMP Pull-Down Resistance	R_{COMP}	FAULT = HI or HICCUP = HI	–	1	–	kΩ
SOFT START (SS PIN)						
Startup (Source) Current	I_{SS}	HICCUP = FAULT = LO	−30	−20	−10	µA
Hiccup (Sink) Current	I_{HIC}	HICCUP = HI	1	2.2	5	µA
Soft-Start Delay Time [3]	$t_{SS(DELAY)}$	C_{SS} = 22 nF	–	440	–	µs
Soft-Start Ramp Time [3]	t_{SS}	C_{SS} = 22 nF	–	880	–	µs
Soft-Start Offset Voltage [3]	$V_{SS(OFFS)}$		–	400	–	mV
FAULT/HICCUP Reset Voltage	$V_{SS(RST)}$	V_{SS} falling due to HICCUP or FAULT	–	200	–	mV
Hiccup Counter Enable Threshold	$V_{HIC(EN)}$	V_{SS} rising	–	2.3	–	V
Soft-Start Frequency Foldback	$f_{LX(SS)}$	0 V < V_{FB} < 200 mV	–	f_{OSC}/4	–	–
		200 mV < V_{FB} < 400 mV	–	f_{OSC}/2	–	–
		V_{FB} > 400 mV	–	f_{OSC}	–	–
Pull-Down Resistance	$R_{SS(FLT)}$	V_{ENBAT} = V_{EN} = 0 V or FAULT	–	2	–	kΩ
Maximum Voltage [3]	$V_{SS(MAX)}$		–	3.3	–	V
HICCUP MODE COUNTING						
High-Side Overcurrent Count	HIC_{OC}	After V_{SS} > $V_{HIC(EN)}$	–	120	–	f_{OSC} counts
LX Short-to-Ground Count [3]	$HIC_{LX(GND)}$		–	2	–	f_{OSC} counts
LX Short-to-VIN Count [3]	$HIC_{LX(VIN)}$		–	2	–	f_{OSC} counts
BOOT Short Circuit Count [3]	$HIC_{BOOT(SC)}$		–	120	–	f_{OSC} counts
BOOT Open Circuit Count [3]	$HIC_{BOOT(OC)}$		–	7	–	f_{OSC} counts

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ELECTRICAL CHARACTERISTICS (continued): Valid at V_{VIN} = 13 V, –40°C ≤ T_J ≤ 150°C, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE MONITORING (V_{FB}) AND NPOR/CPOR PINS						
V_{FB} Overvoltage Threshold	$V_{FB(OV)}$	V_{FB} rising	860	880	900	mV
V_{FB} Overvoltage Hysteresis	$V_{FB(OV,HYS)}$	V_{FB} falling, relative to $V_{FB(OV)}$	–	20	–	mV
V_{FB} Undervoltage Threshold	$V_{FB(UV)}$	V_{FB} rising	719	750	782	mV
V_{FB} Undervoltage Hysteresis	$V_{FB(UV,HYS)}$	V_{FB} falling, relative to $V_{FB(UV)}$	–	15	–	mV
NPOR Startup Delay	$t_{dNPOR(SU)}$	C_{POR} = 22 nF, V_{FB} increasing	–	2	–	ms
NPOR Undervoltage Delay [3]	$t_{dNPOR(UV)}$	Decreasing V_{FB}	–	4	–	µs
NPOR Overvoltage Delay	$t_{dNPOR(OV)}$	After an overvoltage detection	–	120	–	f_{OSC} cycles
NPOR Low Output Voltage	$V_{NPOR(L)}$	NPOR asserted, I_{NPOR} = 4 mA	–	–	400	mV
NPOR Leakage [1]	$I_{NPOR(LKG)}$	NPOR not asserted, V_{NPOR} = 5.5 V	–1	–	+1	µA
CPOR Charge Current [1]	I_{CPOR}		–	–12	–	µA
CPOR Voltage Threshold	V_{CPOR}	V_{CPOR} rising	–	1.25	–	V
ENABLE INPUT (EN PIN)						
Enable High Threshold	$V_{EN(H)}$	V_{EN} rising	–	1.6	2.0	V
Enable Low Threshold	$V_{EN(L)}$	V_{EN} falling	0.8	1.0	–	V
Enable Input Hysteresis	$V_{EN(HYS)}$	$V_{EN(H)} – V_{EN(L)}$	–	600	–	mV
Enable Input Bias Current [1]	I_{EN}	V_{EN} = 12 V	–	6	20	µA
IGNITION ENABLE INPUT (ENBAT PIN)						
ENBAT Low Voltage Threshold	$V_{ENBAT(L)}$	V_{ENBAT} falling	2.2	2.5	3.0	V
ENBAT High Voltage Threshold	$V_{ENBAT(H)}$	V_{ENBAT} rising	2.9	3.2	3.6	V
ENBAT Hysteresis	$V_{ENBAT(HYS)}$	$V_{ENBAT(H)} – V_{ENBAT(L)}$	–	700	–	mV
ENBAT Input Current	I_{ENBAT}	V_{ENBAT} = 12 V	–	16	50	µA
DISABLE DELAY						
EN (or ENBAT) Disable Delay	t_{DIS}	V_{EN} (or V_{ENBAT}) transition low	110	150	190	µs
IGNITION STATUS OUTPUT (ENBATS PIN)						
ENBATS Output Voltage	$V_{ENBATS(L)}$	I_{ENBATS} = 4 mA	–	–	400	mV
ENBATS Output Leakage [1]	$I_{ENBATS(LKG)}$	V_O = 5.5 V, ENBAT = high	–1	–	+1	µA
BOOT REGULATOR (BOOT PIN)						
BOOT Voltage	V_{BOOT}	$V_{BOOT} – V_{LX}$	–	5.5	6.0	V
BOOT Enable Threshold	$V_{BOOT(EN)}$	V_{BOOT} rising, HICCUP = LO after SS	–	3.0	–	V
BOOT Disable Threshold	$V_{BOOT(DIS)}$	V_{BOOT} falling, HICCUP = HI	–	2.5	–	V
BOOT Enable Hysteresis	$V_{BOOT(HYS)}$	$V_{BOOT(EN)} – V_{BOOT(DIS)}$	–	500	–	mV
INTERNAL REGULATOR (VREG PIN)						
VREG Output Voltage	V_{VREG}	V_{ENBAT} or V_{EN} = HI, 7 V < V_{VIN} < 45 V	6.0	6.2	6.4	V
THERMAL SHUTDOWN PROTECTION (TSD)						
TSD Rising Threshold [3]	T_{TSD}	T_J rising, PWM stops immediately and both COMP and SS are pulled low	155	170	–	°C
TSD Hysteresis [3]	$T_{TSD(HYS)}$	T_J falling, relative to T_{TSD}	–	20	–	°C

[1] Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[2] Thermally limited depending on input voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[3] Ensured by design and characterization, not production tested.

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FUNCTIONAL DESCRIPTION

Overview

The A8660 is a fixed-frequency, synchronous buck controller that incorporates all the control and protection circuitry necessary to satisfy a wide range of automotive and industrial applications. The A8660 employs peak current-mode control to provide simple compensation and robust loop stability along with excellent regulation during load transients and virtually instantaneous response to input voltage deviations.

Features of the A8660 include a precision voltage reference, adjustable switching frequency, PWM frequency dithering, high-current integrated gate drivers, a high-voltage rated enable input (ENBAT), a logic-level enable input (EN), a synchronization input ($SYNC_{IN}$), adjustable soft-start time (SS), pre-bias startup capability, low current sleep mode, and an NPOR output with adjustable delay.

The protection features of the A8660 include VIN undervoltage lockout (UVLO), pulse-by-pulse overcurrent protection (OCP), hiccup mode short-circuit protection (HIC), overvoltage protection (OVP), and thermal shutdown (TSD). In addition, the A8660 provides open-circuit, adjacent pin short-circuit and pin-to-ground short-circuit protection.

PWM Switching Frequency

The PWM switching frequency of the A8660 is adjustable from 200 kHz to 2.2 MHz and has an accuracy of –11%, +13% over the operating temperature range. Connecting a resistor from the FSET pin to GND sets the switching frequency. A graph of switching frequency versus R_{FSET} and an equation to calculate R_{FSET} are provided in the Component Selections section of this datasheet.

PWM Frequency Dithering

The A8660 includes PWM frequency dithering—a state-of-the-art technique to help reduce EMI/EMC for demanding automotive applications.

The A8660 performs dithering of the PWM frequency. Dithering the PWM frequency spreads the energy above and below the "base" switching frequency (f_{OSC}). A typical fixed-frequency PWM regulator will create distinct "spikes" of energy at the switching frequency and at multiples of the switching frequency. Conversely, the A8660 spreads the spectrum around the switching frequency, thus creating a lower magnitude at any comparative frequency. However, frequency dithering is disabled if an external clock is applied to $SYNC_{IN}$.

The dithering sweep is internally set at Δf_{OSC} (±10%)—the switching frequency will ramp from 0.90 to 1.10 times the base frequency (f_{OSC}). The modulation frequency sweeps a triangular pattern operating at f_{MOD} (12 kHz).

The following figures compare the conducted and radiated emissions of the A8660 with dithering disabled and enabled: 12 V_{VIN}, 3.3 V_{OUT}, at 2.2 MHz with a 3 A load. The external components and PCB layouts of the two setups were identical. It is clear that PWM dithering significantly reduces the peak levels of energy produced by a traditional, non-dithering regulator.

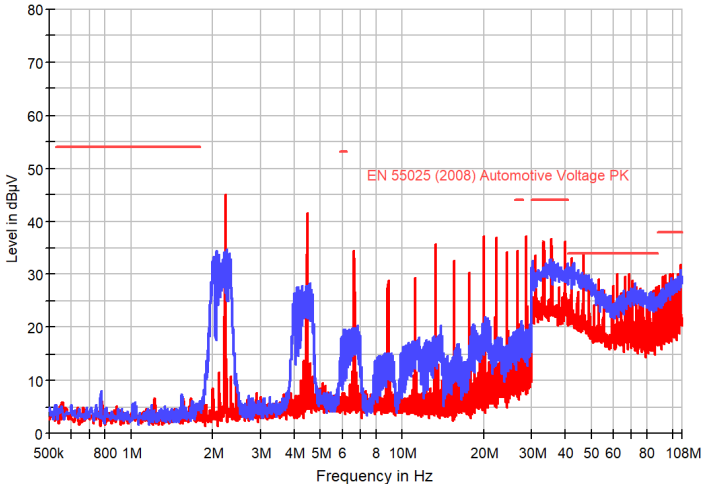

Figure 4: Comparison of Dithering (blue) to Non-Dithering (red) Conducted Emissions (Peak) in dBµV

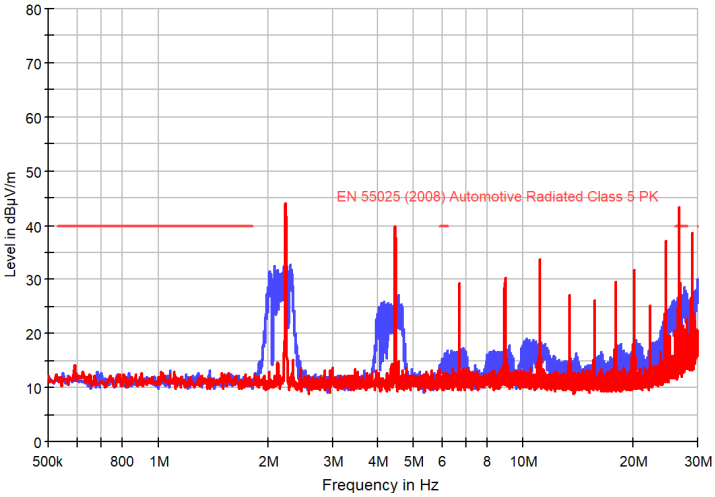

Figure 5: Comparison of Dithering (blue) to Non-Dithering (red) Radiated Emissions (Peak) in dBµV/m

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Soft Recovery from Dropout, Low Battery

Automotive electronics are often exposed to severe dips in the battery voltage that, although temporary, occur very quickly. A typical regulator responds to a voltage dip by raising its duty cycle to a very high value, near 95%. Unfortunately, when the battery returns to normal, the typical regulator cannot reduce its duty cycle as fast as the battery recovers, so the regulators output overshoots. Too much overshoot can result in damage to the load. The A8660 incorporates a unique "soft recovery" technique to eliminate overshoot. Figure 6 displays the effectiveness of the soft recovery technique employed by the A8660.

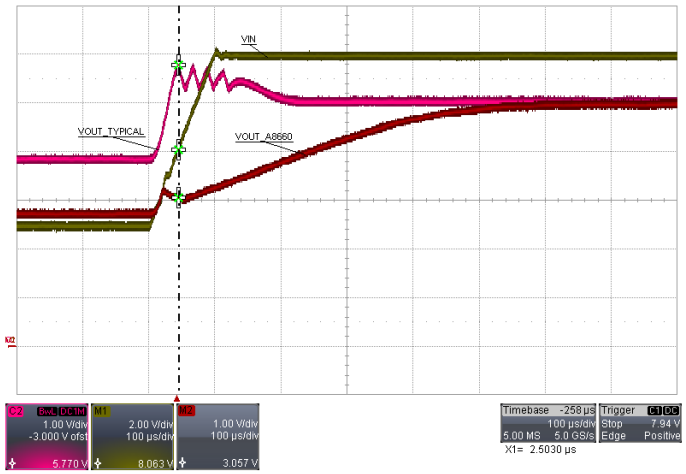

Figure 6: Soft Recovery, VIN = 5 to 12 V in 100 µs
CH1 = VIN, CH2 = VOUT

When VIN recovers, V_{OUT} from the A8660 does not overshoot. Instead, it returns to the set point in a controlled manner. The typical regulator overshoots by 770 mV and begins activating its OV protection.

Reference Voltage

The A8660 incorporates an internal reference that allows output voltages as low as 0.8 V. The accuracy of the internal reference is ±1% at 150°C and ±2% over the entire operating temperature range.

PWM Synchronization ($SYNC_{IN}$)

For designs below the AM band (f_{OSC} < 520 kHz), the synchronization input can be used to shift the base PWM frequency (f_{OSC}) and its harmonics to prevent interference. When an external clock is applied to the $SYNC_{IN}$ pin, the A8660 synchronizes its PWM frequency to the external clock. The external clock may be used to increase the A8660's typical PWM frequency ($f_{OSC(TYP)}$). Synchronization is guaranteed to operate from 1.2 × $f_{OSC(TYP)}$ to 1.5 × $f_{OSC(TYP)}$ which allows for oscillator frequency tolerances plus margin. When synchronizing, the external clock must satisfy the pulse width, duty-cycle, and rise/fall time requirements shown in the Electrical Characteristics table shown in this datasheet.

Pulse-Width Modulation (PWM)

A high-speed PWM comparator capable of pulse widths less than 90 ns is included in the A8660. The inverting input of this comparator is connected to the output of the error amplifier minus the slope compensation. The non-inverting input is connected to the sum of the current sense signal and a PWM Ramp Offset (PWM_{OFFS}).

At the beginning of each PWM cycle, the CLK signal sets the PWM flip-flop and the high-side MOSFET is turned on. When the summation of the DC offset and the current sense signal rises above the error amplifier minus the slope compensation, the comparator resets the PWM flip-flop and the high-side MOSFET is turned off. After a short delay to prevent cross-conduction, the low-side MOSFET is turned on.

Error Amplifier

The error amplifier's primary function is to regulate the converter output voltage. The error amplifier is shown in Figure 7. It is shown as a three-terminal input device with two positive and one negative input. The negative input is simply connected to the FB pin and is used to sense the feedback voltage for regulation. The two positive inputs are used for soft start and regulation. The error amplifier performs an "analog OR" selection between its two positive inputs. The error amplifier regulates to either the soft-start pin voltage minus the soft-start offset (400 mV) or the A8660's internal reference, whichever is lower.

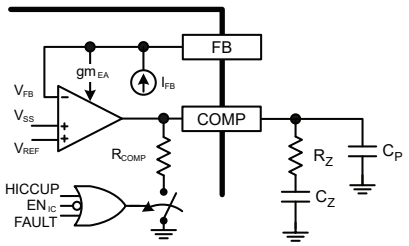

Figure 7: The A8660 Error Amplifier

To stabilize the regulator, a series RC compensation network (R_Z and C_Z) must be connected from the error amplifier's output (COMP pin) to GND as shown in the applications schematic. In most applications, an additional low value capacitor (C_P) should be connected in parallel with the R_Z-C_Z compensation network to roll-off the loop gain at higher frequencies. However, if the C_P capacitor is too large, the phase margin of the converter may be reduced.

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If the regulator is disabled or a fault or hiccup mode occurs, the COMP pin is immediately pulled to GND via approximately 1.0 kΩ and PWM switching is disabled.

Slope Compensation

The A8660 incorporates internal slope compensation to allow PWM duty cycles near or above 50% for a wide range of input/output voltages, switching frequencies, and inductor values. The magnitude of internal slope compensation (S_E) is fixed and is specified, in mV, at the input to the current sense amplifier. During loop compensation, it's often necessary to compare S_E to the inductor current slope in A/µs. However, mV can be converted to A/µs via the sense resistor (R_{SEN}) and the following equation:

Equation 1:

$$S_E \text{ (in A/µs)} = \frac{S_E / R_{SEN}}{1/f_{OSC} - t_{off(min)}}$$

where S_E is in mV, R_{SEN} is in mΩ, f_{OSC} is in MHz, and $t_{OFF(MIN)}$ is in µs.

Current Sense Amplifier

A high-bandwidth current sense amplifier monitors the current in the output inductor. This is accomplished by measuring differentially across a sense resistor (R_{SEN}) connected in series with the inductor. The PWM comparator, pulse-by-pulse current limiters, and the hiccup mode counter require the current signal.

MOSFET Gate Drivers

The A8660 includes high current gate drivers optimized to drive N-channel MOSFETs. The gate drivers employ a non-overlap algorithm to prevent cross-conduction or "shoot-through". An adaptive dead-time circuit monitors the GH and GL outputs and prevents the opposite-side MOSFET from turning on until the MOSFET is fully off. The circuit allows the high-side driver (GH) to turn on only after the lower-side (GL) has turned off. Conversely, the low-side driver is allowed to turn on only after the high-side has turned off. The non-overlap times are usually in the range of 10 to 30 ns.

BOOT Regulator

A boot capacitor must be connected between BOOT and LX. The A8660 contains a relatively high-current LDO (V_{REG}) and a series diode, with a forward voltage of V_F, dedicated to charging the boot capacitor. When the lower MOSFET is on (LX ≈ 0 V) the boot capacitor is charged: $C_{BOOT} = V_{REG} - V_F$. At the start of the next PWM cycle, the charged boot capacitor provides the gate voltage, via the high-side driver, to turn on the high-side MOSFET. The value of the boot capacitor is determined by the amount of gate voltage ripple permitted and the amount of gate charge required by the high-side MOSFET. The Component Selections section of this datasheet covers boot capacitor calculation.

The BOOT regulator has the following protections:

- Undervoltage detection
- Current limit
- Shorted BOOT capacitor
- Missing BOOT capacitor

Soft-Start and Inrush Current Control

Inrush current is controlled by the soft-start function. When the A8660 is enabled and all faults are cleared, the soft-start pin will source I_{SS} (20 µA) and the voltage on the soft-start capacitor, C_{SS}, will ramp up linearly from 0 V. When the voltage at the soft-start pin exceeds the Soft-Start Offset ($V_{SS(OFFS)}$, approximately 400 mV), the error amplifier will raise its output. When the COMP voltage rises above the PWM pedestal, switching will begin. As shown in Figure 8, there is a short delay ($t_{SS(DELAY)}$) between when the enable pin transitions high and when the soft-start voltage reaches ≈400 mV.

Once the A8660 starts switching, the error amplifier will regulate the voltage at the FB pin to the soft-start voltage minus $V_{SS(OFFS)}$. The voltage at the SS pin will rise from 400 mV to 1200 mV, a difference of 800 mV. At the same time, the voltage at the FB pin will rise from 0 V to 800 mV and the regulator's output voltage will rise from 0 V to the desired output, determined by the feedback resistor divider (R_{FB1} and R_{FB2}).

When the voltage at the soft-start pin is high enough, the error amplifier will transition from the soft-start voltage to the A8660's

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internal reference, 800 mV. The voltage at the soft-start pin will continue to rise to approximately 3.3 V. Complete soft-start operation is shown in Figure 8.

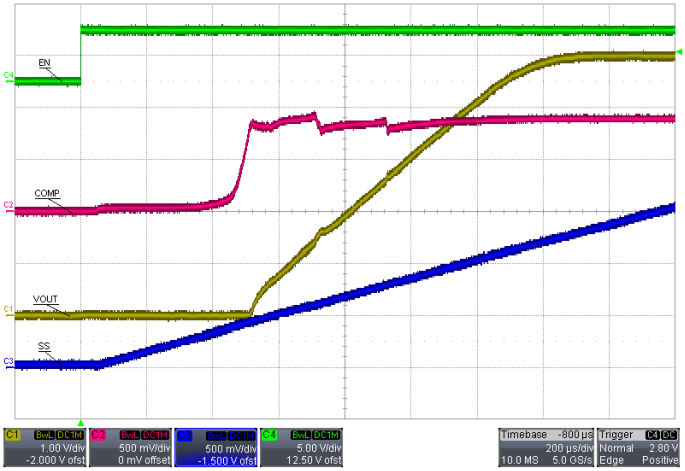

Figure 8: Soft-Start Operation
CH1 = V_{OUT}, CH2 = COMP, CH3 = SS, CH4 = EN

After EN transitions high, there is a delay ($t_{SS(DELAY)}$) as SS charges from 0 V to about 400 mV. After $t_{SS(DELAY)}$, the Error Amp (COMP) requires a short time to raise its output to the point where PWM switching starts. V_{OUT} ramps from 0 V to the desired set-point.

During startup, the PWM switching frequency is folded back to $f_{OSC}/4$, $f_{OSC}/2$, and finally f_{OSC} as the voltage at the FB pin increases from 0 V to 200 mV and finally 400 mV. Frequency foldback is done to provide lower minimum duty cycles and longer off-times during startup. Lower duty cycles result in better control and improved stability when V_{OUT} is near 0 V. Longer off-times allow the inductor current to decay to lower, safer levels before starting the next PWM cycle, in case V_{OUT} is shorted to ground.

Pre-Biased Startup

If the output capacitors are pre-biased, the A8660 will "shift" the startup routine to prevent discharging the output capacitors. Normally, PWM switching starts when the voltage at the soft-start pin reaches approximately 400 mV. However, in the case with pre-bias, the voltage at the FB pin is non-zero, V_{FB}. Switching will not start until the voltage at the soft-start pin increases to approximately V_{FB} + 400 mV. At this voltage, the error amplifier will slew its output upward. Shortly thereafter, PWM switching starts and V_{OUT} ramps upward from the pre-bias level. Figure 9 shows startup when the output voltage is pre-biased to 1.5 V.

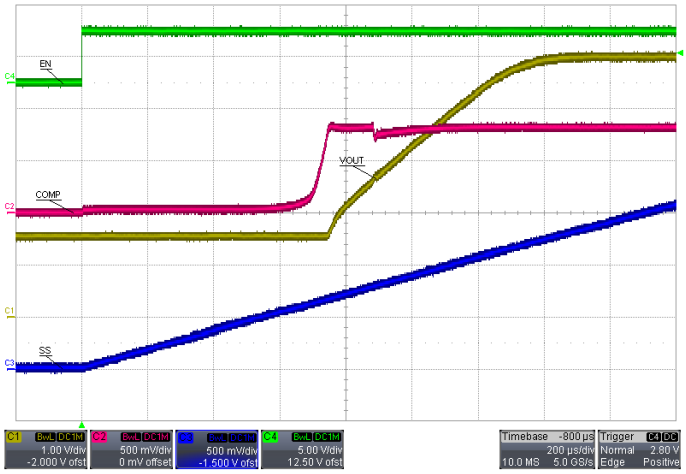

Figure 9: Startup with V_{OUT} Pre-Biased to 1.5 V
CH1 = V_{OUT}, CH2 = COMP, CH3 = SS, CH4 = EN

With a pre-biased output, SS must charge to a higher voltage before the Error Amp (COMP) and PWM switching become active. V_{OUT} ramps monotonically from the pre-bias value to the desired set-point.

Enable Inputs (EN and ENBAT)

Two enable pins are available on the A8660. A logic high on either of these pins enables the controller. One enable (EN) is logic-level compatible for microcontroller or DSP control. The other input (ENBAT) can be connected directly to the high-voltage ignition (IGN) or accessory (ACC) switch. However, considering the unpredictable, fast transients that can occur on V_{BAT} (both positive and negative) a low-pass filter and negative clamp are strongly recommended at the ENBAT input, as shown in the Applications Schematic.

ENBATS Output

This pin provides feedback to the system on the status of the ENBAT pin. This pin is an open-drain output, so an external pull-up resistor must be connected.

SLEEP Mode

If both EN and ENBAT pins are low for more than 150 µs, the A8660 will de-bias its internal circuits and shut down. At that time, it enters sleep mode and draws less than $I_{IN(SLEEP)}$ (10 μA_{MAX}) from VIN. However, the total current drawn from the input supply will be the sum of the current drawn by the control circuitry plus any leakage due to the high- and low-side MOSFETs.

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Output Voltage Monitoring (NPOR/CPOR)

Internal comparators monitor the voltage at the FB pin and control the open-drain NMOS at the NPOR pin. NPOR is high when the voltage at the FB pin is within regulation. The NPOR comparator incorporates hysteresis to prevent chattering due to voltage ripple at the FB pin. The NPOR output is an open-drain output, so an external pull-up resistor must be connected.

NPOR transitions low if:

- V_{FB}, falling < 735 mV_{TYP} (–91.9%), or
- V_{FB}, rising > 880 mV_{TYP} (+110%), or
- EN and ENBAT are low for more than 150 µs and V_{OUT} decays.

If EN and ENBAT are low for more than 150 µs, NPOR transitions low and remains low only as long as the internal circuitry is able to enhance the open-drain output device. Once the internal rail collapses, NPOR will return to the high-impedance state.

The CPOR pin provides a programmable delay from the instant V_{FB} crosses its rising undervoltage threshold ($V_{FB(UV)}$, 750 mV_{TYP}) to when NPOR transitions high. This delay is desirable to allow the output voltage to achieve 100% regulation before the microcontroller or processor starts. The NPOR delay can be as short as 50 µs or as long as 10 ms.

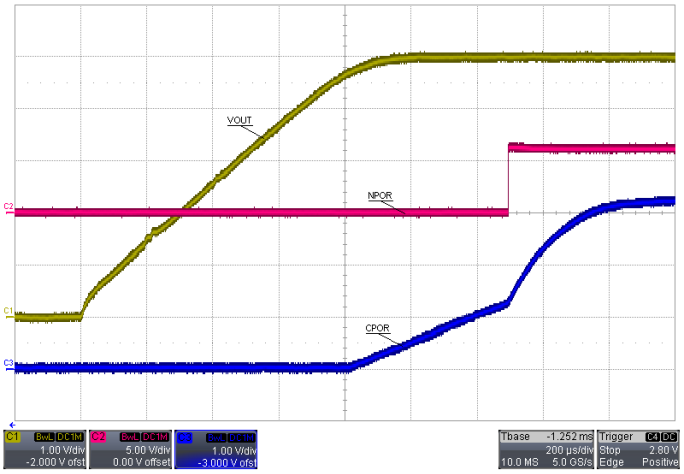

Figure 10: Operation of CPOR and NPOR
CH1 = V_{OUT}, CH2 = NPOR, CH3 = CPOR

When V_{FB} (i.e. V_{OUT}) crosses its rising undervoltage threshold ($V_{FB(UV)}$, 750 mV_{TYP}), the CPOR capacitor begins charging (I_{CPOR}, 12 $µA_{TYP}$). When CPOR reaches its threshold (V_{CPOR}, 1.25 V_{TYP}), the NPOR pin transitions high. In this example, a 4.7 nF CPOR capacitor results in a 490 µs NPOR delay.

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PROTECTION FEATURES

VIN Undervoltage Lockout (UVLO)

An Undervoltage Lockout (UVLO) comparator monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the lockout threshold ($V_{VIN(START)}$). The UVLO comparator incorporates enough hysteresis ($V_{VIN(HYS)}$) to prevent ON/OFF cycling of the regulator due to IR drops in the VIN path during heavy loading or during startup.

Overvoltage Protection (OVP)

The A8660 makes use of the FB pin to provide a basic level of overvoltage protection. Overvoltage can occur if the load current decreases very quickly or the regulator's output is pulled high by some external voltage. When an overvoltage condition is detected: (1) NPOR is pulled low, (2) the high-side MOSFET switching stops, and (3) the low-side MOSFET is turned on during the Minimum Off-Time, $t_{OFF(MIN)}$, 85 ns_{TYP}. The low-side MOSFET sinks a small amount of current, attempting to correct the overvoltage condition.

The COMP and SS voltages are not directly affected by OVP. Therefore, if the regulator's output comes back to its normal range, NPOR will transition high and PWM switching will automatically resume.

Pulse-by-Pulse Overcurrent Protection (OCP)

The A8660 monitors the current in the output inductor and, if the current exceeds the pulse-by-pulse overcurrent threshold (I_{LIM}), the high-side MOSFET is turned off. Normal PWM operation resumes on the next clock pulse from the oscillator.

Because of the subtraction of the slope compensation ramp from the error amp output, the A8660 delivers more current at lower duty cycles and less current at higher duty cycles. For a given switching frequency, this results in more current available at lower duty cycles than higher duty cycles.

Figure 11 shows the typical and worst-case pulse-by-pulse current limits (in mV) versus duty cycle at 410 kHz and 2.2 MHz. To convert the current limit values from millivolts to amps, simply divide by the current sense resistor, R_{SEN}.

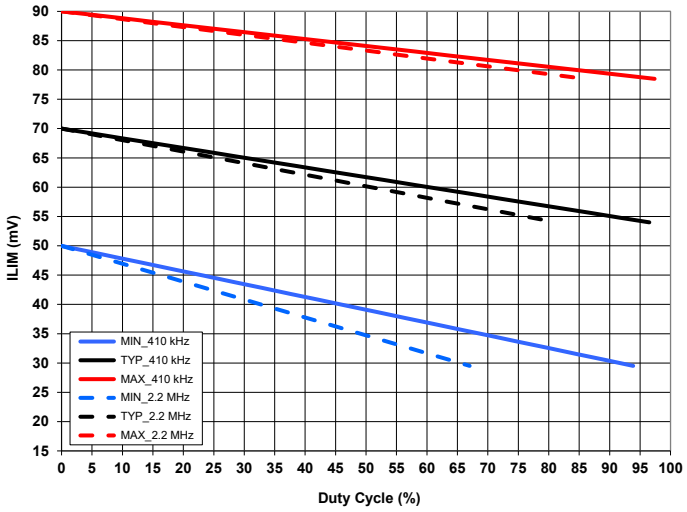

Figure 11: Pulse-by-Pulse Current Limit vs. Duty Cycle at 410 kHz and 2.2 MHz

Output Short-Circuit (Hiccup Mode) Protection

Hiccup mode protects the A8660 when the load is either too high or when the output of the regulator is shorted to ground. When the voltage at the SS pin is below the Hiccup Counter Enable Threshold ($V_{HIC(EN)}$, 2.3 V_{TYP}), Hiccup mode protection is disabled. When the voltage at the SS pin is rises above $V_{HIC(EN)}$, Hiccup mode protection is enabled.

Hiccup Mode overcurrent protection monitors the number of overcurrent events. If more than 120 consecutive overcurrents are detected, then the Hiccup latch is set and PWM switching is stopped. The Hiccup signal causes the COMP pin to be pulled low. Hiccup mode also enables a current sink connected to the soft-start pin (I_{HIC}, 2.2 μA_{TYP}), so that the voltage at the soft-start pin very slowly ramps downward.

When the voltage at the soft-start pin decays to a low level ($V_{SS(RST)}$, 200 mV_{TYP}), the Hiccup latch is cleared and the 2.2 µA current sink is turned off. Also, the soft-start pin begins charging the soft-start capacitor with 20 µA and the voltage at

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the soft-start pin ramps upward. When the voltage at the soft-start pin exceeds the Soft Start Offset ($V_{SS(OFFS)}$, 400 mV_{TYP}) the Error Amp forces the voltage at the COMP pin upward and, shortly thereafter, PWM switching resumes. If the short circuit at the converter's output remains, another Hiccup cycle will occur. Hiccups will repeat until the short circuit is removed or the converter is disabled. If the short circuit is removed, the A8660 will soft start normally and the output voltage will be ramped to the desired level. Hiccup mode operation and recovery is shown in Figure 12.

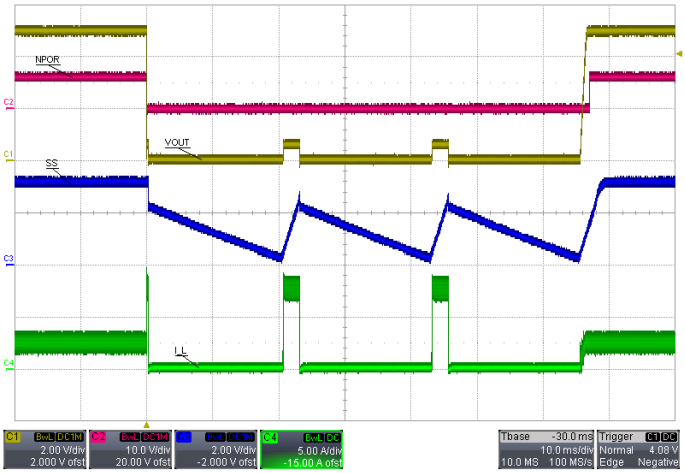

Figure 12: Hiccup Mode Protection and Recovery
CH1 = V_{OUT}, CH2 = NPOR, CH3 = SS, CH4 = IL

When V_{OUT} is shorted to ground, the A8660 enters Hiccup mode. In Hiccup mode, the SS voltage ramps down (slowly), and up (quickly), to provide "cool down" and soft-start timing. The peak inductor current is set by the current sense resistor. V_{OUT} automatically recovers when the output short-circuit is removed.

MOSFET V_{DS} Protection

If the high-side MOSFET is expected to be on, but after approximately 30 ns the V_{DS} voltage is not low enough ($V_{DS} > V_{DS(HS)}$, 390 mV_{TYP}), then a fault is declared and the high-side MOSFET is turned off. If two consecutive $V_{DS(HS)}$ faults occur, the controller enters Hiccup mode. Similarly, if the low-side MOSFET is expected to be on, but after approximately 30 ns, the V_{DS} voltage is not low enough ($V_{DS} > V_{DS(LS)}$, 420 mV_{TYP}), a fault is declared and the low-side MOSFET is turned off. If two consecutive $V_{DS(LS)}$ faults occur, the controller enters Hiccup mode. With these protections, the A8660 can protect against faults such as LX short-to-ground.

Thermal Shutdown (TSD)

The A8660 protects itself from overheating with an internal thermal monitoring circuit. If the junction temperature exceeds the upper thermal shutdown threshold (T_{TSD}, 170°C_{TYP}), the voltages at the soft-start and COMP pins will be pulled to GND and both the upper and low-side MOSFETs shut off. The A8660 will automatically restart when the junction temperature decreases more than the thermal shutdown hysteresis ($T_{TSD(HYS)}$, 20°C_{TYP}).

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COMPONENT SELECTIONS

Setting the Output Voltage (RFB1, RFB2)

The output voltage of the A8660 is programmed by connecting a resistor divider from the output node (V_{OUT}) to the FB pin. The feedback resistors must satisfy the ratio shown below.

Equation 2:

$$\frac{R_{FB1}}{R_{FB2}} = \left(\frac{V_{OUT}}{0.8\ (V)} - 1\right)$$

There are tradeoffs when choosing the values of the feedback resistors. If the series combination ($R_{FB1} + R_{FB2}$) is low, then the light load efficiency of the regulator will be reduced. So it would seem best to choose high values of resistors. On the other hand, if the parallel combination of R_{FB1} // R_{FB2} is very high, the regulator may be susceptible to noise coupling into the FB pin, resulting in pulse-width jitter.

Table 1 shows common output voltages and recommended feedback resistors, assuming less than 0.2% efficiency loss at 100 mA and a parallel combination of 4 kΩ presented to the FB pin. For optimal accuracy, it is recommended that the feedback resistors have ±1% or less tolerances.

Table 1: Recommended Feedback Resistors

V_{OUT}	R_{FB1} (V_{OUT} to FB pin)	R_{FB2} (FB pin to GND)
1.2 V	6.04 kΩ	12.1 kΩ
1.5 V	7.50 kΩ	8.45 kΩ
1.8 V	9.09 kΩ	7.15 kΩ
2.5 V	12.4 kΩ	5.76 kΩ
3.3 V	16.5 kΩ	5.23 kΩ
5.0 V	24.9 kΩ	4.75 kΩ
8.0 V	40.2 kΩ	4.42 kΩ

Switching Frequency (R_{FSET})

The PWM switching frequency (f_{OSC}) is set by connecting a resistor from the FSET pin to ground. The switching frequency must be calculated to avoid steady-state operation near the minimum on time, $t_{ON(MIN)}$, or the minimum off time, $t_{OFF(MIN)}$.

If external synchronization is used, this should be factored into the f_{OSC} calculations.

Ensure the following two equations are satisfied:

Equation 3:

$$f_{OSC} < \frac{V_{OUT}}{t_{ON(MIN)} \times V_{VIN(MAX)}}$$

Equation 4:

$$f_{OSC} < \frac{V_{VIN(MIN)} - V_{OUT}}{t_{OFF(MIN)} \times V_{VIN(MIN)}}$$

where

V_{OUT} is the output voltage,

$t_{ON(MIN)}$ is the minimum on-time (90 ns),

$t_{OFF(MIN)}$ is the minimum off-time (150 ns),

$V_{VIN(MIN)}$ is the minimum steady-state input voltage, and

$V_{VIN(MAX)}$ is the maximum steady-state input voltage, for example, 16 V or 18 V. It is not a voltage from a fault or transient condition, like 40 V load dump.

After the desired switching frequency (f_{OSC}) is known, R_{FSET} can be calculated with the following equation.

Equation 5:

$$R_{FSET} = \left(\frac{37366}{f_{OSC}} - 5.20\right)$$

where f_{OSC} is in kHz and R_{FSET} is in kΩ.

A graph of switching frequency versus R_{FSET} is shown below.

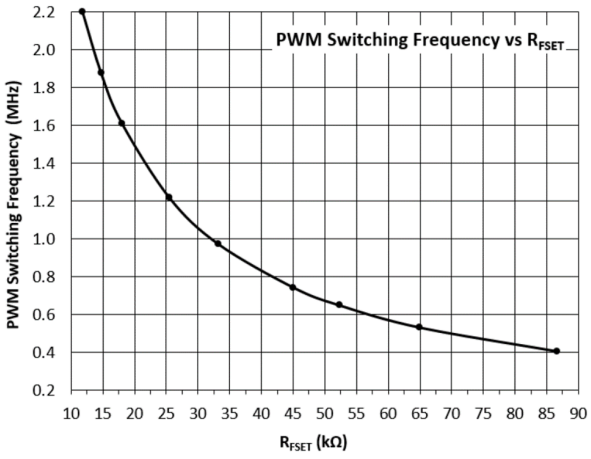

Figure 13: Switching Frequency versus R_{FSET}

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Soft-Start Capacitor (C_{SS})

The soft-start capacitor (C_{SS}) can be calculated to produce a desired soft-start time (t_{SS}) with the following equation,

Equation 6:

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{0.8\ V}$$

where t_{SS} is in ms, I_{SS} is in µA, and the resultant C_{SS} is in nF.

For high-frequency designs with relatively low output capacitance, soft start should be about 0.5 to 2 ms. For low-frequency designs with higher output capacitance, soft start should be higher, 2.5 to 10 ms.

After C_{SS} is known, the soft-start delay can be calculated with the following equation,

Equation 7:

$$t_{SS(DELAY)} = \left(\frac{V_{SS(OFFS)} \times C_{SS}}{I_{SS}} \right)$$

where $V_{SS(OFFS)}$ is in mV, C_{SS} is in nF, I_{SS} is in µA, and the resultant $t_{SS(DELAY)}$ is in µs.

Setting the NPOR Delay (CPOR)

The NPOR delay is programmable, from µs to ms, to satisfy a very wide range of requirements. When V_{FB} (i.e. V_{OUT}) crosses its rising undervoltage threshold, the CPOR pin sources current, charging its capacitor. NPOR transitions high after the voltage at the CPOR pin rises to a specific value. The following formula calculates C_{POR} to provide a given NPOR delay in ms (t_{dNPOR}):

Equation 8:

$$C_{POR} = 9.6 \times t_{dNPOR}$$

where t_{dNPOR} is in ms, and the result, C_{POR}, is in nF.

Sense Resistor (R_{SEN})

The pulse-by-pulse current limit of the converter is set by the value of the sense resistor (R_{SEN}). It's important to calculate the sense resistor at the worst-case expected operating conditions: low input voltage (maximum duty cycle), minimum pulse-by-pulse current limit, and a reduced inductor value.

To a first-order, the maximum duty cycle occurs at:

Equation 9:

$$D_{MAX} = \left(\frac{V_{OUT}}{V_{IN(MIN)}} \right)$$

where $V_{IN(MIN)}$ is the minimum steady-state input voltage.

After D_{MAX} is calculated, the Current Limit versus Duty Cycle curve, introduced in the Overview section of this datasheet, should be used to determine the minimum current limit, in mV, at the typical switching frequency. The next plot, Figure 14, indicates a minimum current limit of 30.0 mV with D_{MAX} = 66% for 2.2 MHz (3.3 V_{OUT}, 5.0 $V_{IN(MIN)}$).

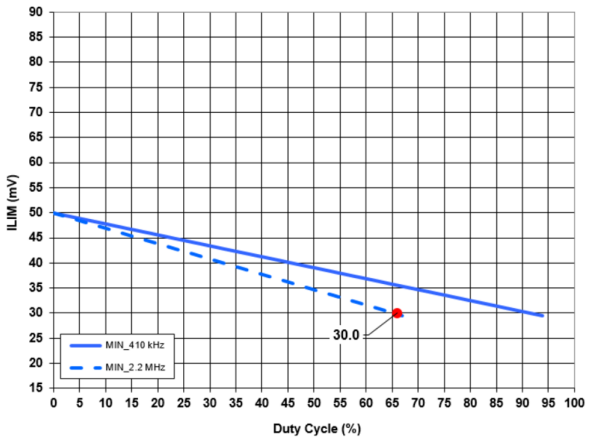

Figure 14: Minimum Current Limit at 2.2 MHz for 66% Duty Cycle is $V_{ILIM(MIN)}$ = 30 mV

After the minimum current limit value is known ($V_{ILIM(MIN)}$), the sense resistor value can be calculated with the following equation. This equation allows 10% margin for peak inductor current (at low V_{VIN}, the ripple is lower, so ±10% should be adequate) and 5 A of output current.

Equation 10:

$$R_{SEN} = \left(\frac{90\% \times 30\ mV}{5\ A} \right) = 5.4\ m\Omega$$

The closest available resistor value should be chosen: 5 mΩ allows a bit more output current, but 6 mΩ provides a slightly larger current signal for the PWM control loop.

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Slope Compensation (S_E)

Like the pulse-by-pulse current limit, slope compensation (in A/µs) depends on the sense resistor and can be calculated with the following equation.

Equation 11:

$$S_E\,(\text{in A/µs}) = \frac{S_E\,(\text{in V})}{R_{SEN} \times \left(\frac{1}{f_{OSC}} - t_{OFF(MIN)}\right)}$$

where S_E (in V) is listed in the Electrical Characteristics table as 16 mV, R_{SEN} is in mΩ, f_{OSC} is the PWM switching frequency in MHz, and $t_{OFF(MIN)}$ is the minimum PWM off-time in µs.

Output Inductor (L1)

Compared to other regulators, the A8660 controller has approximately twice the typical amount of slope compensation. This lowers its sensitivity to noise and reduces pulse-width jitter, but sacrifices a very small amount of phase margin. Therefore, to have a reasonable inductor value and a normal amount of ripple current (25% to 35%), the inductor value must be calculated so the slope compensation (S_E) is 2× the down-slope of the inductor current. Use the following equation to calculate the output inductor, L1.

Equation 12:

$$L1 = \frac{V_{OUT}}{\left(\frac{S_E}{2}\right)}$$

The inductor must be able to support two operating conditions: peak current at maximum load with highest steady-state input voltage, and peak current when V_{OUT} is shorted to ground.

The inductor should not saturate, given the peak operating current shown in the next equation. In this equation, $V_{VIN(MAX)}$ is the maximum continuous input voltage, such as 16 or 18 V.

Equation 13:

$$I_{PEAK} = \frac{90\text{ mV}}{R_{SEN}} - \frac{S_E\,(\text{in A/µs}) \times V_{OUT}}{1.21 \times f_{OSC} \times V_{VIN(MAX)}}$$

Also, if the output of the regulator is shorted to ground, the inductor should be able to support the current given by the next equation, without being damaged.

Equation 14:

$$I_{PEAK} = \frac{90\text{ mV}}{R_{SEN}} - S_E\,(\text{in A/µs}) \times t_{ON(MIN)}$$

For a given input voltage (V_{VIN}), the peak-to-peak inductor ripple (ΔI_{L1}) can be calculated with the following two equations. The on-time (t_{ON}) should not be less than the minimum on-time ($t_{ON(MIN)}$) specified in the Electrical Characteristics.

Equation 15:

$$t_{ON} = \frac{V_{OUT}}{V_{VIN}} \times \frac{1}{f_{OSC}}$$

Equation 16:

$$\Delta I_{L1} = \frac{(V_{OUT} - V_{VIN})}{L1} \times t_{ON}$$

Output Capacitance (C_{OUT})

In the case of ceramic output capacitors, the output voltage ripple (ΔV_{OUT}) is determined by the output capacitors integrating the inductor current ripple.

Equation 17:

$$C_{OUT} \geq \frac{V_{OUT} \times \left[1 - \frac{V_{OUT}}{V_{VIN(MIN)}}\right]}{8 \times f_{OSC}^{\,2} \times L1 \times \Delta V_{OUT}}$$

Regulators usually have a much higher output capacitance than predicted by the simple ripple-voltage equation.

A much more realistic value of output capacitance can be calculated assuming a fast downward step in load (from I_{LOAD1} to I_{LOAD2}) and a maximum allowable voltage deviation (ΔV_{OUT}). This is the worst-case scenario as it assumes there is no influence from the control loop.

The following calculation assumes all the energy from the inductor is simply transferred to the output capacitors. The minimum output capacitance for a required output voltage deviation (ΔV_{OUT}) can be calculated with the following:

Equation 18:

$$C_{OUT} = \frac{L1 \times (I_{LOAD1}^{\,2} - I_{LOAD2}^{\,2})}{(V_{OUT} + \Delta V_{OUT})^2 - V_{OUT}^{\,2}}$$

where I_{LOAD1} is the maximum load, I_{LOAD2} is the minimum load, and ΔV_{OUT} is the maximum allowed output voltage deviation.

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Input Capacitance (C_{IN})

Three factors should be considered when choosing the input capacitors. First, they must be able to support the maximum expected input voltage with adequate design margin. Second, their RMS current rating must be higher than the expected RMS input current to the regulator. Third, they must have enough capacitance and a low enough ESR to limit the input voltage dV/dt to a value much less than the hysteresis of the UVLO circuitry ($V_{VIN(HYS)}$, 800 mV_{TYP}) at maximum load and minimum input voltage.

The input capacitor(s) must limit voltage deviations at the VIN pin to significantly less than the A8660's UVLO hysteresis during maximum load and minimum input voltage. The following equation calculates the minimum input capacitance.

Equation 19:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{0.79 \times f_{OSC} \times \Delta V_{VIN(MIN)}}$$

where D is the duty cycle, $\Delta V_{VIN(MIN)}$ is a value less than the hysteresis of the VIN UVLO comparator ($\Delta V_{VIN(MIN)} \leq 200$ mV is recommended), and f_{OSC} is the nominal PWM frequency.

The $D \times (1 - D)$ term in Equation 19 has an absolute maximum value of 0.25 at 50% duty cycle. So, for example, a very conservative design based on I_{OUT} = 5 A, f_{OSC} = 79% of 2.2 MHz, $D \times (1 - D)$ = 0.25, and ΔV_{VIN} = 100 mV,

$$C_{IN} \geq \frac{5\ A \times 0.25}{0.79 \times 2.2\ MHz \times 100\ mV} = 7.2\ \mu F$$

The input capacitors must deliver the RMS current according to the next equation, where the duty cycle $D = V_{OUT} / V_{VIN}$.

Equation 20:

$$I_{RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

Figure 15 shows the normalized input capacitor RMS current versus duty cycle. To use this graph, simply find the operational duty cycle (D) on the x-axis and determine the input/output current multiplier on the y-axis. For example, at 27.5% duty cycle (3.3 V_{OUT} / 12 V_{VIN}), the input/output current multiplier is near 0.45. Therefore, if the regulator is delivering 5 A of steady-state load current, the input capacitor(s) must support 0.45 × 5A or 2.25 A_{RMS}.

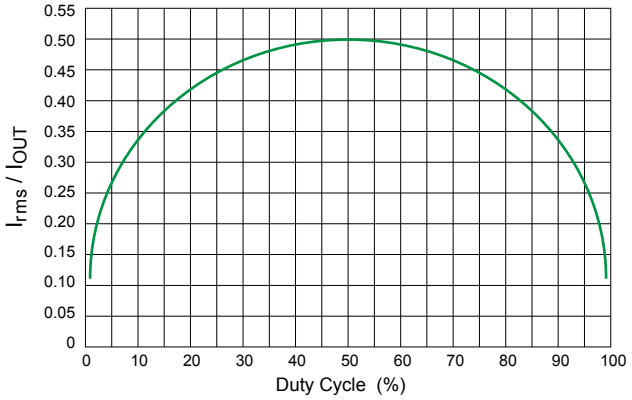

Figure 15: Input Capacitor Ripple versus Duty Cycle

A good design should consider the DC bias effect on a ceramic capacitor—as the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction), so these types should be avoided. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

For all ceramic capacitors, the DC bias effect is even more pronounced on smaller case sizes, so a good design will use the largest affordable case size (i.e., 1206 or 1210). Also, it's advisable to select input capacitors with plenty of design margin in the voltage rating to accommodate the worst-case transient input voltage.

MOSFET Selections (Q1, Q2)

There are several parameters to consider when selecting the MOSFETs. First, the drain-to-source voltage of the MOSFETs must be able to withstand the transient peak input voltage from the system. Second, N-channel MOSFETs with $R_{ds(on)}$ clearly specified at V_{GS} = 4.5 V should be used. Lastly, the MOSFET thermal characteristics and external thermal solution must be capable of dissipating the expected power to maintain the junction temperature in a safe range.

Given the maximum ambient operating temperature of the module ($T_{A(MAX)}$), maximum MOSFET junction temperature ($T_{J(MAX)}$), and thermal resistance of its package ($R_{\theta JA}$), the maximum allowable power dissipation (P_{MAX}) can be calculated:

Equation 21:

$$P_{MAX} = \frac{T_{J(MAX)} - T_{A(MAX)}}{R_{\theta JA}}$$

Knowing P_{MAX}, the following equations calculate limits for the

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low-side and high-side MOSFETs.

Begin with the low-side MOSFET. Dissipation in this device is primarily from conduction and body-diode losses during the non-overlap time. Assume 20 ns of non-overlap time and calculate the body diode losses:

Equation 22:

$$P_{DIODE} = 20\ ns \times V_{SD} \times f_{OSC} \times I_{OUT}$$

where V_{SD} is the source-to-drain voltage of the body diode when it is forward biased (typically 0.8 to 1.2 V).

The next equation sets a limit for $R_{ds(on)}$ of the low-side MOSFET:

Equation 23:

$$R_{ds(on)LS} @ 25°C \leq \frac{P_{MAX} - 2 \times P_{DIODE}}{1.8 \times I_{LS(RMS)}^2}$$

In the preceding equation, 1.8 in the denominator accounts for $R_{ds(on)}$ increase at high temperature. The maximum RMS current in the low-side MOFET occurs when V_{VIN} is high. $I_{LS(RMS)}$ can be approximated with:

Equation 24:

$$I_{LS(RMS)} \approx I_{OUT} \times \sqrt{1 - (V_{OUT} / V_{VIN(MAX)})}$$

where $V_{VIN(MAX)}$ is the maximum steady-state input voltage (i.e., 16 V), not a momentary or transient voltage due to a fault condition (i.e. 40 V).

Calculations for the high-side MOSFET are more involved because this device is subject to both conduction and switching losses.

Assume the same maximum power dissipation calculated earlier (P_{MAX}). However, assign a percentage to conduction losses (k) and the remainder to switching losses (1 – k). The exact distribution of losses depends on the PWM switching frequency. At high PWM frequency, switching losses are greater than conduction losses, so k must be low ($k \ll 0.5$). At low PWM frequency, switching losses are less than conduction losses, so k can be high ($k \gg 0.5$).

The following equation sets a limit for $R_{ds(on)}$ of the high-side MOSFET:

Equation 25:

$$R_{ds(on)HS} @ 25°C \leq \frac{P_{MAX} \times k}{1.8 \times I_{HS(RMS)}^2}$$

The maximum RMS current in the high-side MOFET occurs when V_{VIN} is low. $I_{HS(RMS)}$ can be approximated with:

Equation 26:

$$I_{HS(RMS)} \approx I_{OUT} \times \sqrt{(V_{OUT} / V_{VIN(MIN)})}$$

The next equation calculates switching losses:

Equation 27:

$$\frac{V_{VIN} \times I_{OUT}}{2} \times f_{OSC} \times (t_{S(LH)} + t_{S(HL)}) = P_{MAX} \times (1 - k)$$

where $t_{S(LH)}$ is the switching time from low to high, and $t_{S(HL)}$ is the switching time from high to low.

The switching times can be calculated with:

Equation 28:

$$t_{S(LH)} = \frac{Q_{G(SW)}}{I_{HD(SRC)}}$$

Equation 29:

$$t_{S(HL)} = \frac{Q_{G(SW)}}{I_{HD(SINK)}}$$

where $I_{HD(SRC)}$ and $I_{HD(SINK)}$ are the source and sink currents from the high-side gate drivers, and $Q_{G(SW)}$ is the gate charge required to switch the MOSFET.

From the Electrical Characteristics table, note that $I_{HD(SINK)} \approx 2 \times I_{HD(SRC)}$. Making this substitution into the total switching time equation and simplifying:

Equation 30:

$$t_{S(LH)} + t_{S(HL)} = \frac{3 \times Q_{G(SW)}}{2 \times I_{HD(SRC)}}$$

Finally, substituting this into the switching losses equation and solving for $Q_{G(SW)}$:

Equation 31:

$$Q_{G(SW)} \leq \frac{4 \times P_{MAX} \times (1 - k) \times I_{HD(SRC)}}{3 \times V_{VIN} \times I_{OUT} \times f_{OSC}}$$

MOSFET datasheets do not often specify $Q_{G(SW)}$ as a stand-alone parameter. Usually, they only specify two values of gate charge in their electrical characteristics: Q_{GS} and Q_{GD}. A third gate charge value, $Q_{G(TH)}$, is required. This can be found on the gate charge curve at the gate threshold voltage, $V_{GS(TH)}$. This gate voltage is clearly specified in every datasheet. Figure 16 shows a typical gate charge curve. Along with Equation 32, it should be straightforward to derive $Q_{G(SW)}$.

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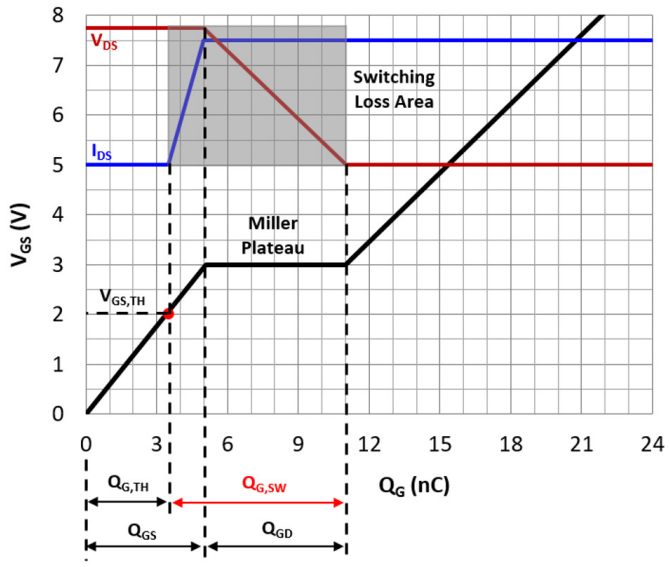

Figure 16: Typical MOSFET Gate Charge Curve

Equation 32:

$$Q_{G(SW)} = (Q_{GS} + Q_{GD}) - Q_{G(TH)}$$

$$Q_{G(SW)} = (5\text{ nC} + 6\text{ nC}) - 3.5\text{ nC} = 7.5\text{ nC}$$

BOOT Capacitor Calculation (C_{BOOT})

The value of the boot capacitor is determined by the allowable amount of boot ripple voltage (ΔV_{BOOT}) and the total gate charge required ($Q_{G(TOTAL)}$) to raise the gate voltage of the high-side MOSFET to about 5.5 V.

Assume a MOSFET is selected with the V_{GS} versus Q_G curve, previously shown in Figure 16. From this plot, it can be seen that to achieve a gate voltage of 5.5 V will require a total gate charge of 16.5 nC. Assuming an allowable boot voltage ripple of 200 mV, the BOOT capacitor can be calculated:

Equation 33:

$$C_{BOOT} \geq \frac{Q_{G(TOTAL)}}{\Delta V_{BOOT}} = \frac{16.5\text{ nC}}{200\text{ mV}} = 82.5\text{ nF}$$

To allow for capacitor tolerances, a value of 100 nF is recommended. The dielectric of the BOOT capacitor must be a quality type that is very stable from –40°C to 150°C, such as X7R or X7S. The voltage rating should be at least 16 V.

VREG Capacitor Recommendations (C_{VREG})

The VREG capacitor is an important component for stable, reliable regulator operation. As show here, the two internal LDOs and the voltage reference all depend on this capacitor.

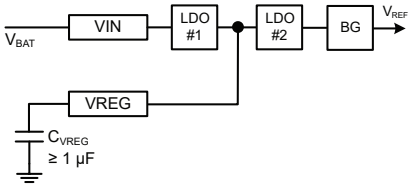

Figure 17: Internal LDOs and V_{REF} depend on C_{VREG}

The VREG capacitor (C_{VREG}) should typically be 1 µF, and its dielectric must be stable from –40°C to 150°C, such as X7R or X7S. Its voltage rating should be at least 16 V. The VREG capacitor must be located as close as possible to the VREG pin and grounded to analog (quiet) ground.

Loop Compensation (R_Z, C_Z, C_P)

Numerous papers and datasheets cover the topic of current mode control compensation. A simplified tuning procedure is presented here.

1. Choose the system bandwidth, f_C, the frequency at which the magnitude of the gain will cross 0 dB. Based on the PWM switching frequency, recommended values for f_C are $f_{LX}/20 < f_C < f_{LX}/7.5$. A higher value of f_C will generally provide a better transient response, while a lower value of f_C will be easier to obtain good gain and phase margins.

2. Calculate the transconductance of the power stage:

   Equation 34:

$$gm_{POWER} = \frac{1}{G_{CSA} \times R_{SEN}}$$

   where G_{CSA} is the gain of the current sense amplifier from the Electrical Characteristics table (7.5 V/V_{TYP}), and R_{SEN} is the current sense resistor calculated previously.

3. Calculate the R_Z resistor value to set the desired system bandwidth (f_C):

   Equation 35:

$$R_Z = f_C \times \frac{V_{OUT}}{V_{FB}} \times \frac{2 \times \pi \times C_{OUT}}{gm_{POWER} \times gm}$$

   where gm is the error amplifier transconductance from the Electrical Characteristics table (750 $\mu A/V_{TYP}$).

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4. Determine the frequency of the pole (f_{P1}) formed by C_{OUT} and a relatively low load resistance, R_L, (i.e., heavy load) with the following equation:

Equation 36:

$$f_{P1} = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

5) Calculate a range of values for the C_Z capacitor,

Equation 37:

$$\frac{4}{2\pi \times R_Z \times f_C} < C_Z < \frac{1}{2\pi \times R_Z \times 1.5 \times f_{P1}}$$

6) Given the range of C_Z values from the previous step, calculate the frequencies of the low frequency zero (f_{Z2}) from the error amplifier:

Equation 38:

$$f_{Z2} = \frac{1}{2\pi \times R_Z \times C_Z}$$

To maximize system stability (i.e., have the most gain margin), keep f_{Z2} relatively low (i.e., use a higher value of C_Z). To optimize transient recovery time at the expense of some phase margin, keep f_{Z2} at a higher frequency (i.e. use a lower value of C_Z). Exactly where to place the starting value of f_{Z2} is up to the user.

The following figure compares load step responses for two systems: one with f_{Z2} at 16 kHz (73° phase margin) and another with f_{Z2} at 50 kHz (51° phase margin). The system with f_{Z2} at 50 kHz recovers to within 0.5% approximately three times faster than the system with f_{Z2} at 16 kHz.

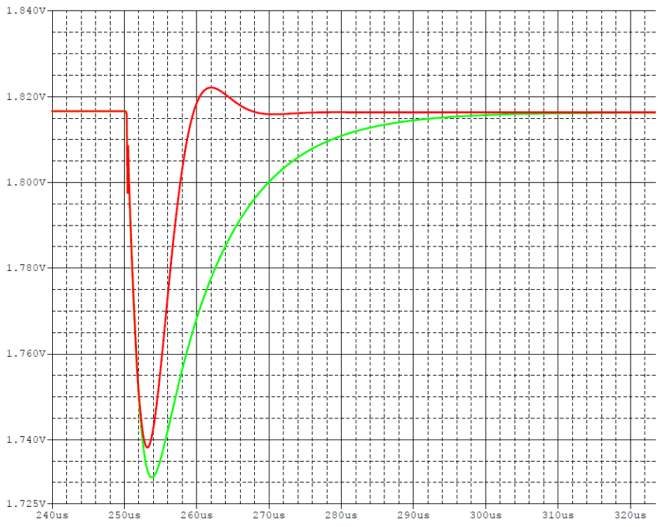

Figure 18: Transient recovery comparison for f_{Z2} at 16 kHz/73° and 50 kHz/51°

7) Calculate the frequency of the ESR zero (f_{Z1}) formed by the output capacitor(s) with the following formula:

Equation 39:

$$f_{Z1} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

a) If f_{Z1} is at least 1 decade higher than the target crossover frequency (f_C), then f_{Z1} can be ignored. This is usually the case for a design using ceramic output capacitors. Use the following equation to calculate the value of C_P by setting f_{P3} somewhere between $5 \times f_C$ to $f_{LX} / 2$.

Equation 40:

$$C_P = \frac{1}{2\pi \times R_Z \times f_{P3}}$$

b) On the other hand, if f_{Z1} is near or below the target crossover frequency (f_C), then use the previous equation to calculate C_P by setting f_{P3} equal to f_{Z1}. This is usually the case for a design using high ESR electrolytic output capacitors.

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PCB LAYOUT RECOMMENDATIONS

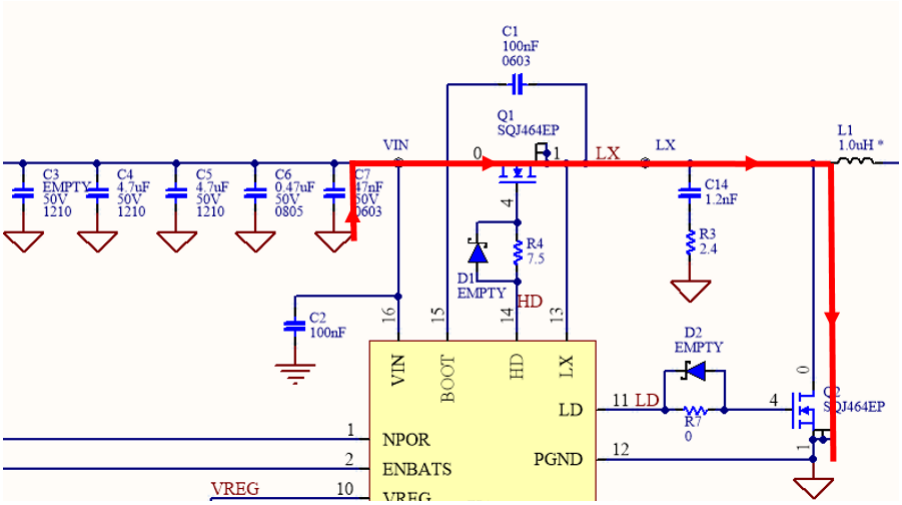

Figure 19: The most critical power component connections for the buck converter.
Place these components so the loop from C7, Q1, and Q2 is short and uninterrupted.

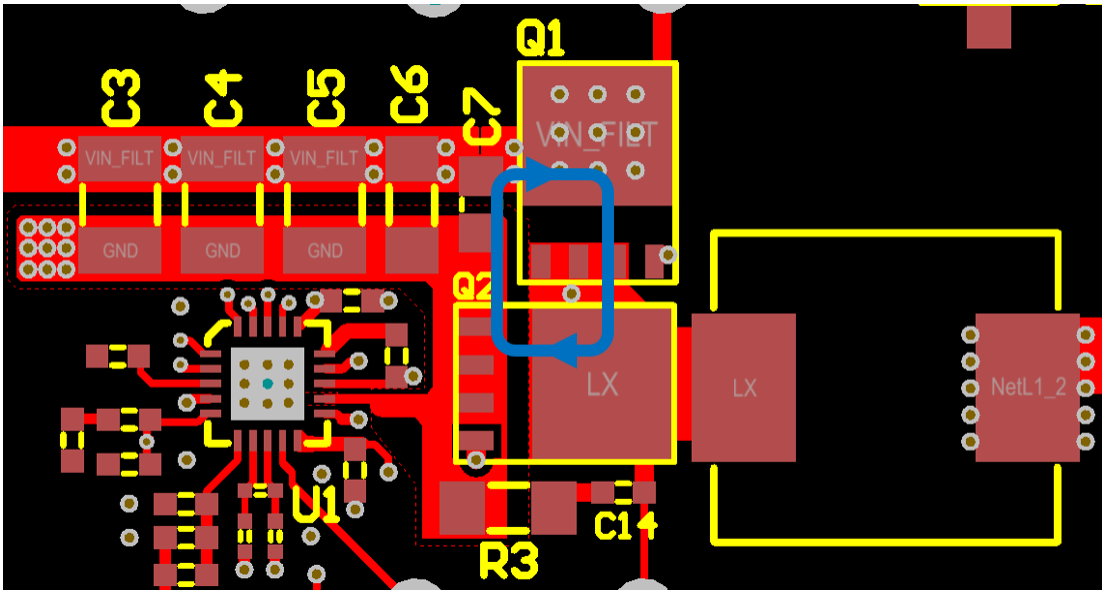

Figure 20: Recommended placement and routing of the most critical power components.

1) All these components must be on the same layer as the A8660.
2) Routing of these components must not be interrupted by other traces.
3) Minimize the loop area from C5, C6, and C7 through Q1 + Q2.
4) The nine ground vias 'East' of C3 are placed so they only conduct DC current.
5) The switch node trace (LX1) is very short and wide enough to carry 6 A.
6) In this high frequency loop, the ground reference is connected to PGND (pin 12).
7) The snubber components (R3, C14) should connect directly from LX node to PGND.

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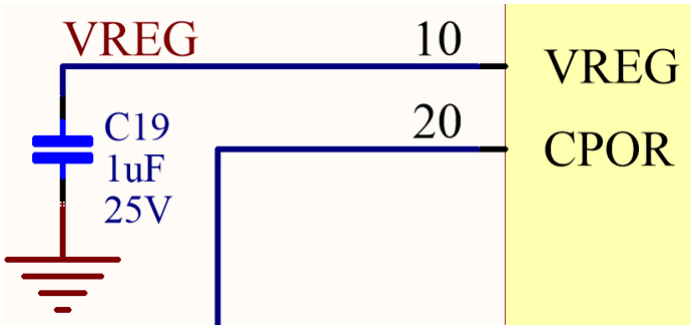

Figure 21: The VREG capacitor (C19) must be connected to AGND.
The VREG capacitor provides stable voltage for internal logic rails.

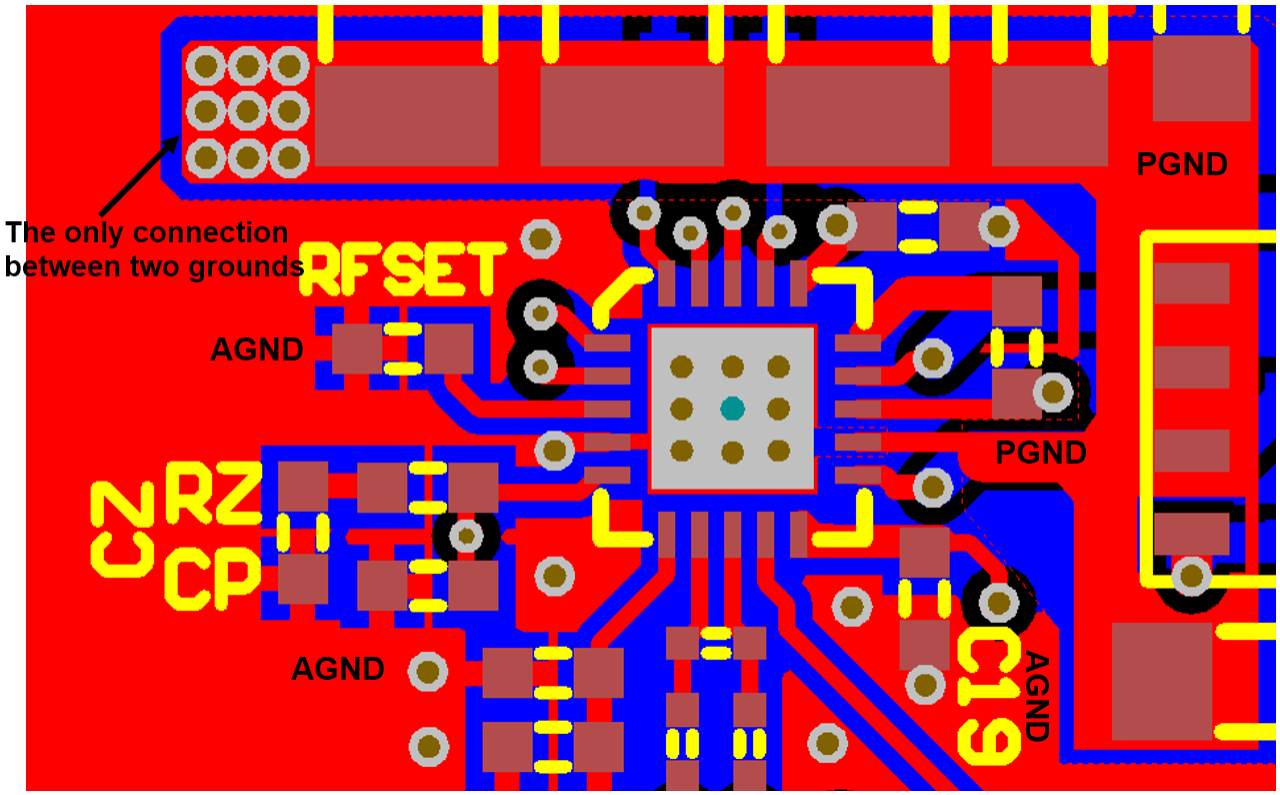

Figure 22: Recommended placement and routing of PGND and AGND.

1) AGND is the internal logic reference. PGND is the power ground for gate charge loop.
2) The two grounds should be connected only at one place.
3) VREG capacitor C19 must be connected with the AGND to provide solid logic rail voltage.
4) All other internal logic signal grounding should be connected to AGND

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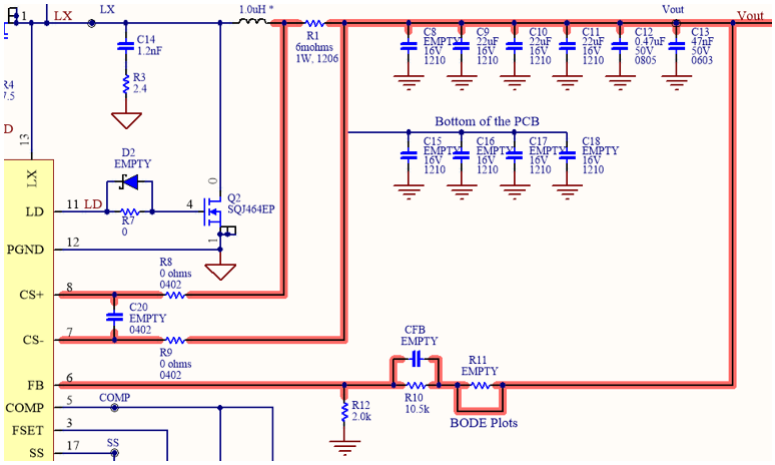

Figure 23: Current Sense and Feedback

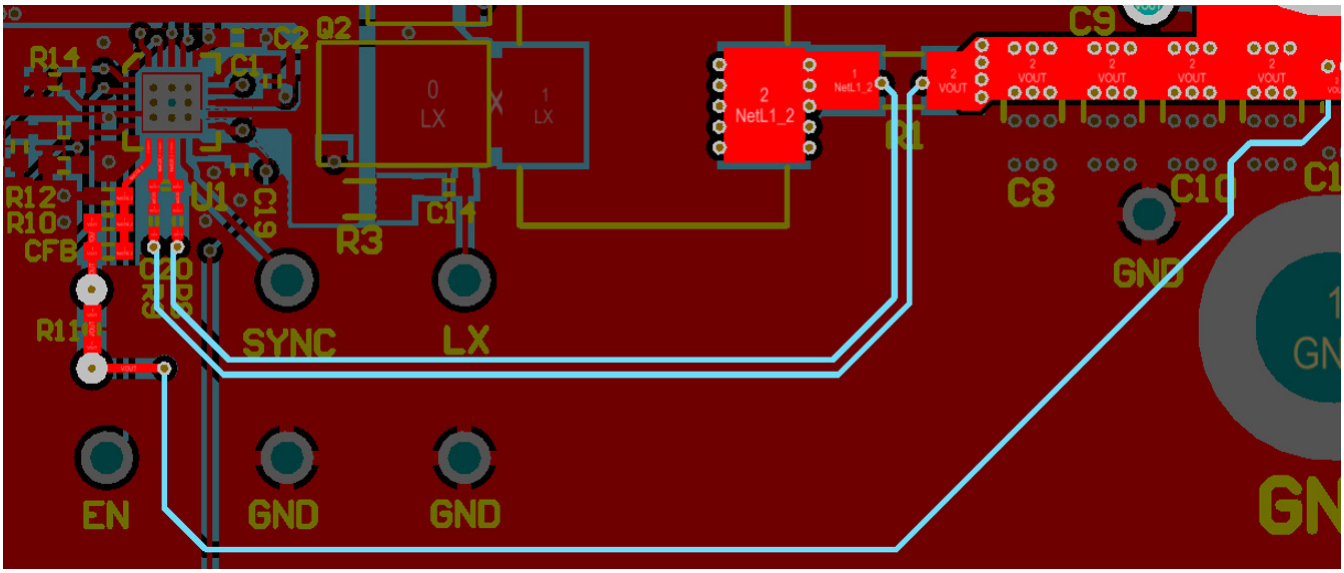

Figure 24: Recommended placement and routing of current sense and feedback.

1) Current sense resistor R1 should be placed between the power inductor and output capacitor.
2) Current sense signal traces should be connected to the inner side of the current sense resistor.
3) Minimize the loop area of current sense trace.
4) The VOUT feedback trace is routed to the point of loading and after any filtering.
5) The VOUT feedback resistor divider (R12, R10) must be located near the FB pin.

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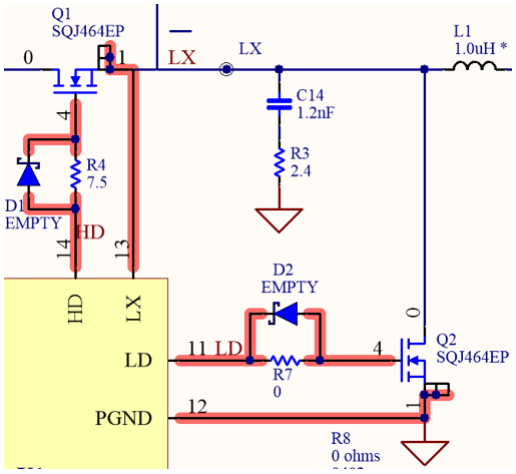

Figure 25a: Gate connection for the external FSETs

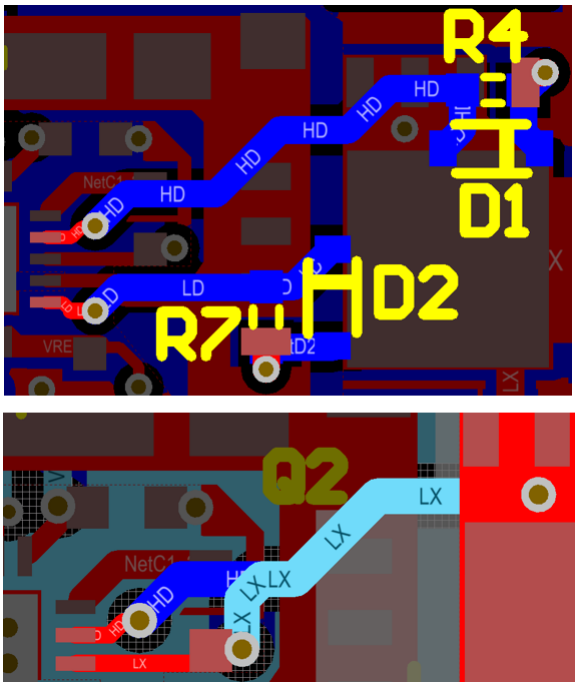

Figure 25b: Recommended placement and routing of gate connection for the external FETs.

1) Gate trace on both FETs must be short and at least 25 mil wide.
2) The return path for the gate signal should be directly underneath or on top of the gate signal.

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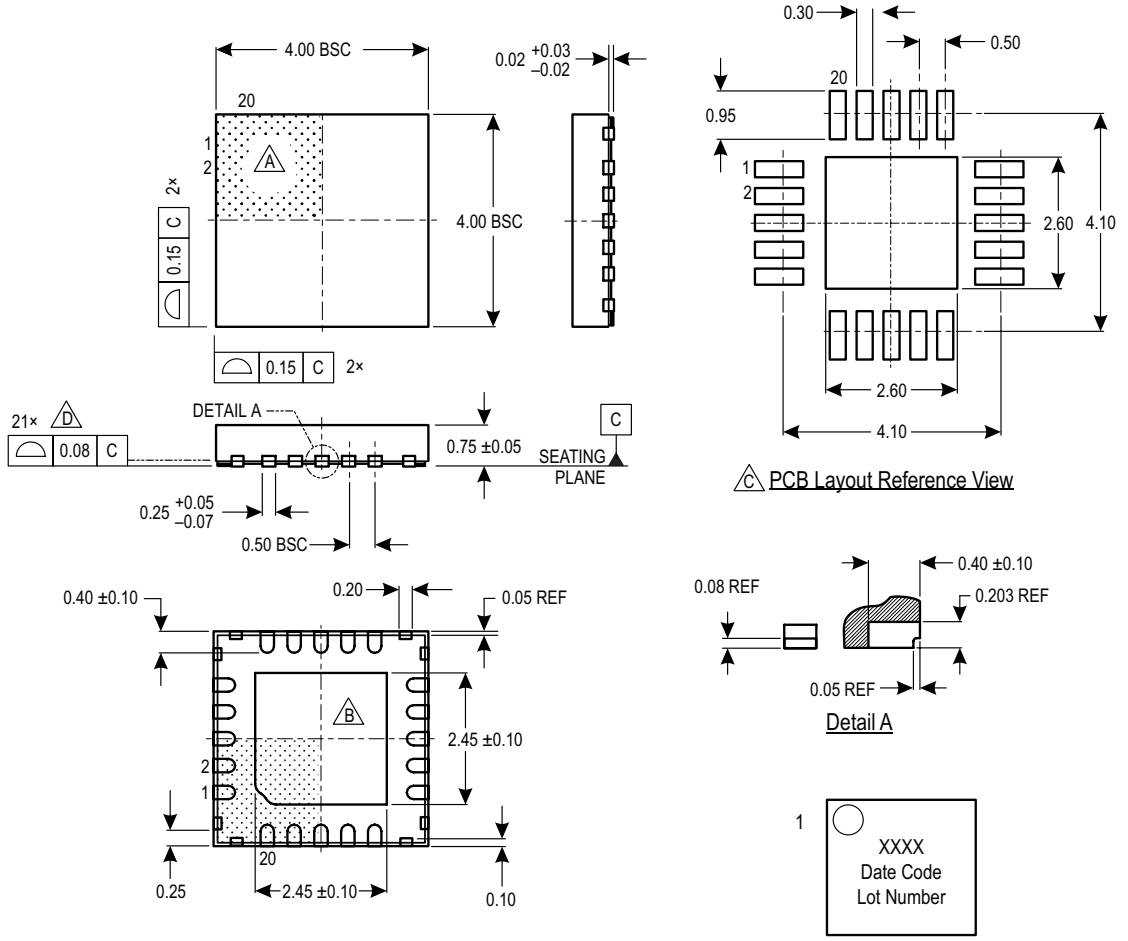
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WGGD)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area.

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion).

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-21BM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

D Coplanarity includes exposed thermal pad and terminals.

E Branding scale and appearance at supplier discretion.

E Standard Branding Reference View

Lines 1, 2, 3 = 6 characters

Line 1: Part Number
Line 2: 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Pin 1 Dot top left
Center align

Figure 26: Package ES, 20-Pin QFN with Exposed Thermal Pad and Wettable Flank

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Revision History

Number	Date	Description
–	June 19, 2018	Initial release
1	August 22, 2018	Corrected typo in Equation 35 (page 21).
2	September 13, 2019	Minor editorial updates
3	August 10, 2020	Updated “ENB” with “EN” (pages 1, 9, 12), Enable Inputs (EN and ENBAT) section (page 12), and Application Schematics (pages 1, 4, 5)
4	August 12, 2021	Updated package drawing (page 27)

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