Package Thermal Characteristics

This document provides test information about the standard packages offered by Allegro MicroSystems. The data given is intended as a general reference only and is based on certain simplifications such as constant chip size and standard bonding methods.

To use this document, in the Allegro Package Code column, locate the package designator for the device. To locate package variants, use the JEDEC Package Outline column to locate the corresponding JEDEC designator, or use the Quantity and Type of Terminals column to locate the variant by the configuration of terminals.

Three columns of results are presented:

- $R_{\theta JA}$ High K. This test is performed using a high thermal conductivity, multilayer printed circuit board that closely approximates those specified in the JEDEC standards JESD51-7 (for surface-mount devices except area array devices), JESD51-9 (for area array devices), or JESD51-10 (for through-hole devices). For devices with exposed thermal pads, thermal vias are included per JESD51-5. These standards are available for download on the JEDEC Web site, www.jedec.org.
- $R_{\theta JA}$ Usual. This test is performed using a common printed circuit board. Where only one value is shown in this column, a single-layer printed circuit board with minimal exposed copper area is tested. Where two values are shown in this column, it indicates that the printed circuit board has multiple test locations, each having a different amount of exposed copper foil (2 oz. thickness). Both one- and two-layer boards are tested. The ground leads (power tabs) or exposed pad of the devices are connected to these areas of copper foil. The two results shown indicate the highest and the lowest test results

  Note that the paired results are text hyperlinks to other Web pages. Click the text to open the linked page, which provides information on the printed circuit board layout, as well as intermediate test results.

- $R_{\theta JC}$, $R_{\theta JP}$, $R_{\theta JT}$. This column provides results on other thermal dissipation paths:

  $R_{\theta JC}$ [c] Through the device case (measured using a cold-plate).

  $R_{\theta JP}$ [p] Through the exposed thermal pad (for related topic, see Application Note 26020, *Procedure for Measuring Pad-to-Ambient Thermal Resistance ($R_{\theta PA}$) for Exposed Pad Packages)*.

  $R_{\theta JT}$ [t] Certain devices have some leads joined together (fused) internally, and in some instances externally, to provide more efficient heat dissipation (referred to as a power tab or batwing configuration).

Allegro Package Code	Package Type (Common Package Designator)	JEDEC Package Outline	Quantity and Type of Terminals	$R_{\theta JA}$		$R_{\theta JC}$ $R_{\theta JP}$ $R_{\theta JT}$ (°C/W)
				High K (°C/W)	Usual (°C/W)	
A	Plastic Dual In-Line (DIP, PDIP, DIL, or PDIL)	MS-001 AA	14-Pin	40	73	38 [c]
		MS-001 BB	16-Pin	38	68	38 [c]
		MS-001 AC	18-Pin	36	65	25 [c]
		MS-001 AD	20-Pin	32	60	25 [c]
		MS-010 AA	22-Pin	30	56	21 [c]
		MS-001 AF	24-Pin	26	50	–
		MS-011 AB	28-Pin	–	45	16 [c]
		MS-011 AC	40-Pin	26	36	–
B	Semi-Tab Plastic Dual In-Line (DIP, PDIP, DIL, or PDIL)	MS-001 BB	16-Pin	28	41-63	6 [t]
		MS-001 AF	24-Pin	26	36-54	6 [t]
CG	Wafer-level Chip Scale Package (WLCSP): refer to device datasheet	–	–	–	–	–
EB	Semi-Tab (two) Plastic Leaded Chip Carrier (PLCC/PQCC)	MS-018 AB	28-J Lead	22	36	6 [t]
		MS-018 AC	44-J Lead	22	30-50	6 [t]
EC	Plastic Leadless Package with Exposed Thermal Pad (MLPQ/QFN)	MO-220 WGGE	4 x 4 mm 26-Contact	35	–	2 [p]
ED	Semi-Tab (four) Plastic Leaded Chip Carrier (PLCC/PQCC)	MS-018 AC	44-J Lead	22	30-50	6 [t]
EE	Plastic Leadless Package with Exposed Thermal Pad (MLPD/DFN/SON)	MO-229 UCCD	2 x 2 mm 8-Contact	49	92-219	–
EH	Plastic Leadless Package with Exposed Thermal Pad (MLPD/DFN/SON)	MO-229 WCED	3 x 2 mm 6-Contact	50	70-221	2 [p]
EJ	Plastic Leadless Package with Exposed Thermal Pad (MLPD/DFN/SON)	MO-229 WEED	3 x 3 mm 10-Contact	45	65-190	2 [p]
EK	Plastic Leadless Package with Exposed Thermal Pad (MLPD/DFN/SON)	MO-229 WEEA	3 x 3 mm 5-Contact	50	72-182	2 [p]
EL	Plastic Leadless Package with Exposed Thermal Pad (MLPD/DFN/SON)	MO-229 WCCD	2 x 2 mm 6-Contact	56	95-250	2 [p]
EP	Square Plastic Leaded Chip Carrier (PLCC/PQCC)	MS-018 AA	20-J Lead	41	78	35 [c]
		MS-018 AB	28-J Lead	37	68	30 [c]
		MS-018 AC	44-J Lead	30	54	25 [c]
EQ	Rectangular Plastic Leaded Chip Carrier (PLCC/PCC)	MS-016 AE	32 (7 x 9)-J Lead	37	52	30 [c]
ES	Plastic Leadless Package with Exposed Thermal Pad (MLPQ/QFN)	MO-220 WEED	3 x 3 mm 16-Contact	47	96-133	–
		MO-220 WGGD	4 x 4 mm 20-Contact	37	75-136	2 [p]

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Allegro Package Code	Package Type (Common Package Designator)	JEDEC Package Outline	Quantity and Type of Terminals	$R_{\theta JA}$		$R_{\theta JC}$ $R_{\theta JP}$ $R_{\theta JT}$ (°C/W)
				High K (°C/W)	Usual (°C/W)	
ET	Plastic Leadless Package with Exposed Thermal Pad (MLPQ/QFN)	MO-220 VHHD	5 x 5 mm 28-Contact	32	64-115	2 [p]
			5 x 5 mm 32-Contact	30	–	–
EU	Plastic Leadless Package with Exposed Thermal Pad (MLPQ/QFN)	MO-220 WGGC	4 x 4 mm 16-Contact	36	–	2 [p]
EV	Plastic Leadless Package with Exposed Thermal Pad (MLPQ/QFN)	MO-220 VJJD	6 x 6 mm 36-Contact	27	64-103	2 [p]
		MO-220 VJJD	6 x 6 mm 40-Contact	27	–	2 [p]
		MO-220 VKKD	7 x 7 mm 48-Contact	24	–	2 [p]
EW	Plastic Leadless Package with Exposed Thermal Pad (MLPD/DFN/SON)	MO-229 X2BCD	1.5 x 2 mm 6-Contact	64	125-235	–
JP	Plastic Low-Profile Quad Flatpack with Exposed Thermal Pad (eLQFP)	MS-026 BBC-HD	48-Gull Wing	23	44-86	2 [p]
JS	Plastic Thin-Profile Quad Flatpack with Exposed Thermal Pad (TQFP)	MS-026 ADD-HD	80-Gull Wing	21	–	2 [p]
K	Plastic Single In-Line (SIP)	–	4-Lead	–	177	–
KA	Plastic Single In-Line (SIP)	–	5-Lead	–	164	–
KB	Plastic Single In-Line (SIP)	–	3-Lead	–	177	–
KC	Plastic Single In-Line (SIP)	–	3-Lead	–	177	–
KN	Plastic Single In-Line (SIP)	–	4-Lead	–	170	–
KT	Plastic Single In-Line (SIP)		4-Lead	–	174	–
L	Plastic Small-Outline IC (SOIC)	MS-012 AA	8-Gull Wing	80	140	45 [c]
		MS-012 AB	14-Gull Wing	65	120	33 [c]
		MS-012 AC	16-Gull Wing	64	118	–
LB	Semi-Tab Plastic Small-Outline IC (SOIC)	MS-013 AA	16-Gull Wing	38	48-90	6 [t]
		MS-013 AC	20-Gull Wing	38	48-87	6 [t]
		MS-013 AD	24-Gull Wing	35	45-77	6 [t]
LD	Plastic Thin Shrink Small-Outline IC (TSSOP)	MO-153 BD-1	38-Gull Wing	51	127	–
LE	Plastic Thin Shrink Small-Outline IC (TSSOP)	MO-153 AA	8-Gull Wing	145	–	–
LG	Plastic Thin Shrink Small-Outline IC (TSSOP) with 6 internally-fused leads	MO-153 BD-1	38-Gull Wing	47	121	–
LH	Plastic Small-Outline Transistor (SOT23W)	–	3-Lead	–	110-228	–
LJ	Plastic Small-Outline IC (SOIC) with Exposed Thermal Pad	MS-012 BA	8-Gull Wing	35	62-147	2 [p]
LP	Plastic Thin Shrink Small-Outline IC with Exposed Thermal Pad (HTSSOP)	MO-153 ABT	16-Gull Wing	34	43-129	2 [p]
		MO-153 ADT	24-Gull Wing	28	32-100	2 [p]
		MO-153 AET	28-Gull Wing	28	32-100	2 [p]

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				High K (°C/W)	Usual (°C/W)	
LQ	Plastic Small-Outline IC (SOIC)	–	36-Gull Wing	44	85	–
LT	Plastic Small-Outline Transistor (SOT89)	TO-243 AA	3-Lead	–	78-180	–
LW	Wide-Body Plastic Small-Outline IC (SOIC)	MS-013 AA	16-Gull Wing	48	94	–
		MS-013 AB	18-Gull Wing	48	94	–
		MS-013 AC	20-Gull Wing	48	90	–
		MS-013 AD	24-Gull Wing	44	85	–
		MS-013 AE	28-Gull Wing	44	80	–
LY	Mini Small Outline (MSOP) with Exposed Thermal Pad	MO-187BA-T	10-Gull Wing	48	48-177	–
LZ	Mini Small Outline (MSOP)	MO-187BA	10-Gull Wing	103	180	–
M	Mini Plastic Dual In-Line (DIP or PDIP)	MS-001 BA	8-Pin	–	80	55 [c]
SA	Plastic (9 mm Ø x 9 mm long) SIP Module	–	4-Lead	–	147	–
SB	Plastic (8.9 mm Ø x 7 mm long) SIP Module	–	4-Lead	–	150	–
SE	Plastic (10 mm Ø x 7 mm long) SIP Module	–	4-Lead	–	77-101	–
SG	Plastic (8 mm Ø x 5.5 mm long) SIP Module	–	4-Lead	–	84-126	–
SH	Plastic (8 mm Ø x 5.5 mm long) SIP Module	–	4-Lead	–	84-126	–
SJ	Plastic (8 mm Ø x 5.5 mm long) SIP Module	–	4-Lead	–	84-126	–
U	Plastic Mini Single In-Line (SIP)	–	3-Lead	–	184	–
UA	Plastic Ultra-Mini Single In-Line (SIP)	–	3-Lead	–	165	–
W	Power-Tab Plastic Single In-Line (SIP)	–	12-Lead	–	38	2 [t]
		–	18-Lead	–	28	9 [t]
Z	Power-Tab Plastic Single In-Line (SIP)	TO-220 AB	3-Lead	–	67	3 [t]
		TS-001	5-Lead	–	65	3 [t]

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