LED Driver with Integrated Micropower Hall-Effect Switch

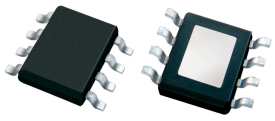
FEATURES AND BENEFITS

- Micropower (25 µA, typical) when LED is off
- Linear LED drive up to 150 mA
- Omnipolar Hall-effect switch
  - □ Low drift over temperature
  - □ Solid-state reliability
  - □ Insensitive to physical stress
- External LED-enable pin for direct on/off control
- Hall-effect switch output
  - □ Supports secondary switches and/or LED drivers
  - □ Provides switch state for other functions
  - □ Selectable output polarity
- Automotive-grade ruggedness and fault-tolerance
  - □ "K" temperature range qualified per AEC-Q100
  - □ Reverse-battery and load-dump protection
  - □ Short-circuit protection
  - □ Thermal protection
- Internal protection circuits enable 40 V load dump compliance without external protection components

APPLICATIONS

- Automotive glove boxes and storage
- Automotive vanity mirrors
- Task lighting
- Consumer electronics

PACKAGE:



8-Pin SOICN
with Exposed Thermal Pad
(Suffix LJ)

Not to scale

DESCRIPTION

The APS13568 is an integrated circuit that combines an ultrasensitive, omnipolar, micropower Hall-effect switch with a linear programmable current regulator providing up to 150 mA to drive high brightness LEDs. The omnipolar Hall-effect switch provides contactless control of the regulated LED current, which is set by a single reference resistor. This highly integrated solution offers high reliability and ease of design compared to a discrete solution.

The Hall-effect switch operates with either a north or a south magnetic pole. The switch output polarity can be set with an external pulldown on the POL input pin. This allows the user to select whether the APS13568 switch output goes low when a magnet is present or when the magnetic field is removed. Chopper stabilization provides low switch point drift over temperature.

The LED is turned on when the $\overline{EN}$ input goes low. This active-low input can be connected directly to the Hall switch output, $\overline{SO}$, to turn the LED on when the switch output goes low. This flexible solution allows the user to connect additional slave switches, LED drivers, PWM, or microprocessor inputs to control when the LED is on. Optionally, an external capacitor can be used to adjust the fade-in/fade-out feature.

On-board protection for shorts to ground and thermal overload prevents damage to the APS13568 and LED string by limiting the regulated current until the short is removed and/or the chip temperature has reduced below the thermal threshold.

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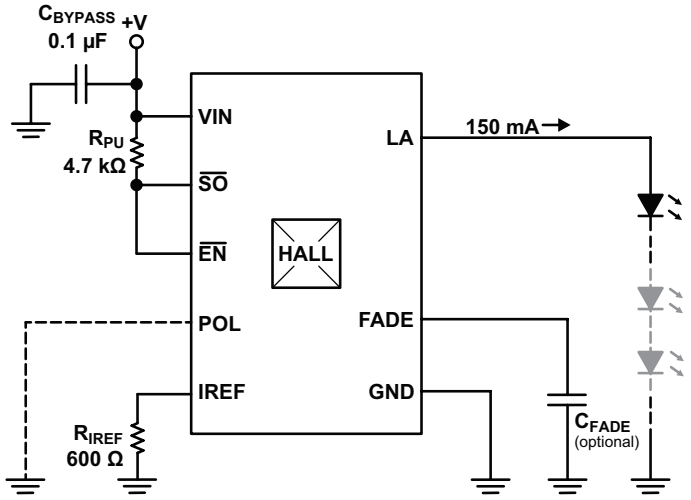

Figure 1: Typical Application Diagram

DESCRIPTION (continued)

The device is packaged in an 8-pin SOICN (LJ) with an exposed pad for enhanced thermal dissipation. It is RoHS-compliant, with 100% matte-tin leadframe plating.

The APS13568 is available in an "E" temperature version (up to 85°C) for industrial and consumer applications, as well as a "K" temperature version (up to 125°C) that is qualified per AEC-Q100 for automotive applications.

SELECTION GUIDE

Part Number	Packing	Package	Temperature Range, T_A (°C)
APS13568KLJATR-T	3000 pieces per 13-in. reel	8-pin SOICN surface mount	–40 to 125
APS13568ELJATR-T	3000 pieces per 13-in. reel	8-pin SOICN surface mount	–40 to 85

RoHS COMPLIANT

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage [1]	V_{IN} (V_{DD})		–18 to 30	V
Pin $\overline{EN}$	$V_{\overline{EN}}$		–18 to 30	V
Pin LA	V_{LA}		–0.3 to 30	V
Pin $\overline{SO}$	$V_{\overline{SO}}$		–0.3 to 30	V
Pin IREF	V_{IREF}		–0.3 to 6.5	V
Pin FADE	V_{FADE}		–0.3 to 6.5	V
Pin POL	V_{POL}		–0.3 to 6.5	V
Maximum Junction Temperature	$T_{J(MAX)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

[1] This rating does not apply to extremely short voltage transients such as Load Dump and/or ESD. Those events have individual ratings, specific to the respective transient voltage event.

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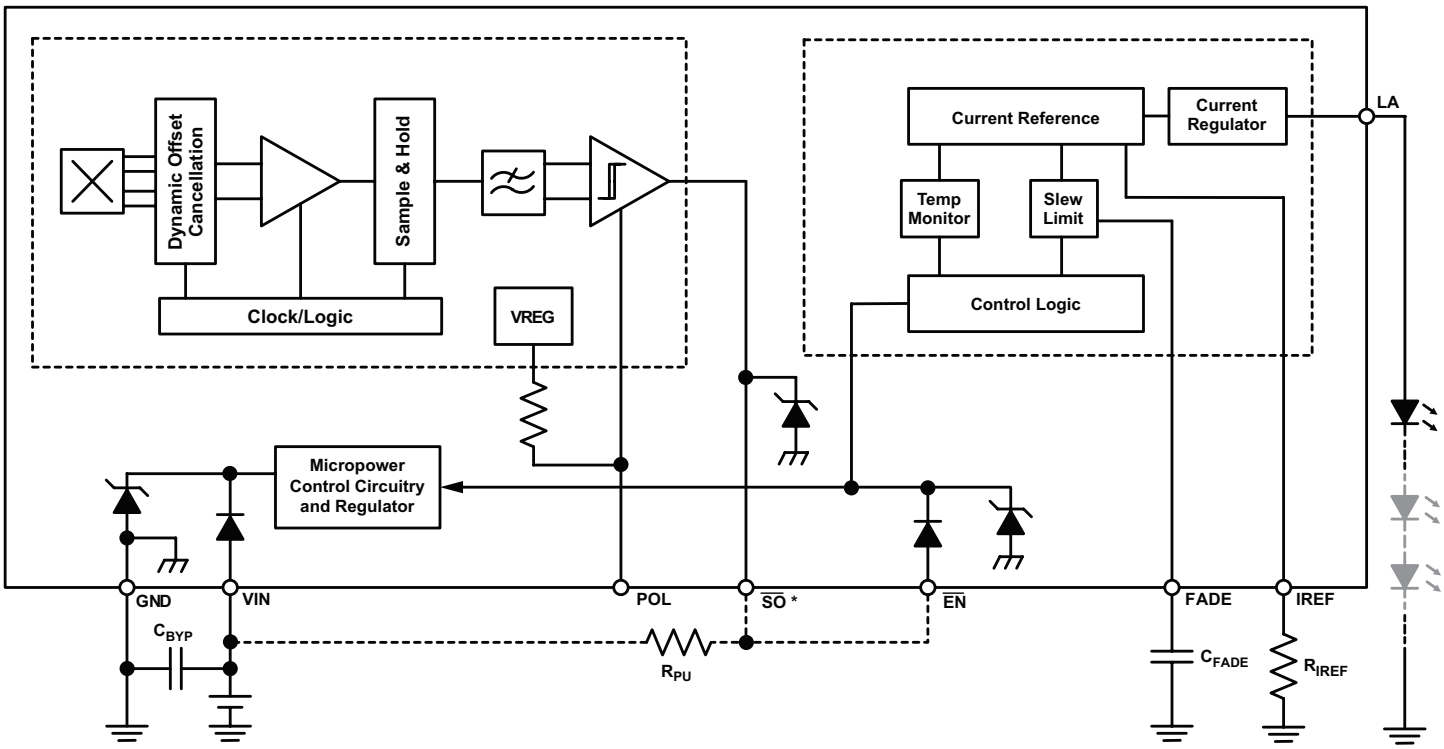
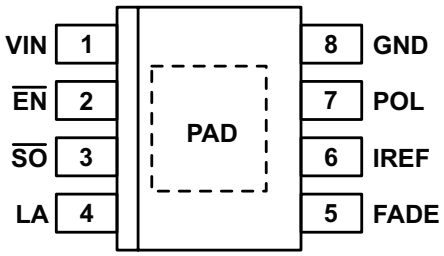
FUNCTIONAL BLOCK DIAGRAM



* $\overline{SO}$ can be pulled up to VIN or an external voltage source.

PINOUT DRAWING AND LIST



Package LJ, 8-Pin SOICN Pinout Drawing

Pinout List

Pin Number	Pin Name	Description
1	VIN	Supply voltage
2	$\overline{EN}$	Active-low LED drive enable input
3	$\overline{SO}$	Active-low Hall-effect switch output
4	LA	LED anode (+) connection
5	FADE	Fade-in/fade-out timing control
6	IREF	Current reference resistor connection
7	POL	Selects LED activation polarity relative to $\overline{SO}$
8	GND	Ground reference
–	PAD	Exposed thermal pad (may be left floating or tied to ground)

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ELECTRICAL CHARACTERISTICS: Valid at T_A = –40°C to 125°C (Range K); T_A = –40°C to 85°C (Range E); V_{IN} = 7 to 24 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Units
SUPPLY and STARTUP						
V_{IN} Functional Operating Range	V_{IN} (V_{DD})	Operating, T_J < 165°C	7	–	24	V
V_{IN} Average Current	I_{INAVG}	LED off, $\overline{EN}$ = high	–	25	50	µA
V_{IN} Quiescent Current	I_{INQ}	LED off, $\overline{EN}$ = high, see Figure 13	–	20	45	µA
V_{IN} Active Current	$I_{IN(ACT)}$	I_{LA} = 0 mA, $\overline{EN}$ = low, see Figure 13	–	4	6	mA
Startup Time	t_{ON}	Measured from V_{IN} > 7 V to I_{LA} > 90% of 150 mA with POL = GND, $\overline{EN}$ = low, R_{IREF} = 600 Ω, FADE disabled (see Fade pin description below)	–	–	1	ms
External Response Time	t_{EXT_ON}	Measured from $\overline{EN}$ < V_{IL} to I_{LA} > 90% of 150 mA with V_{IN} > 7 V, R_{IREF} = 600 Ω, FADE disabled (see Fade pin description below)	–	50	–	µs
Supply Zener Clamp Voltage	$V_{IN(Z)}$	$I_{IN(ACT)}$ = 6.5 mA, T_A = 25°C	32	45	–	V
MICROPOWER OPERATION						
Period	t_{PERIOD}	See Figure 13	–	50	–	ms
Awake Time	t_{AWAKE}		–	50	–	µs
LED CURRENT REGULATION						
Reference Voltage	V_{IREF}	267 µA < I_{REF} < 2 mA	–	1.2	–	V
Reference Current Ratio	G_H	I_{LA} ÷ I_{REF}	–	75	–	–
Current Accuracy [2][3][4]	E_{ILA}	4.5 kΩ > R_{IREF} > 600 Ω	–5	–	5	%
Output Source Current	I_{LA}	R_{IREF} = 600 Ω, LED driver enabled (see Table 1)	–	150	170	mA
Dropout Voltage	V_{DO}	V_{IN} – V_{LA} , I_{LA} = 150 mA	–	–	2.4	V
		V_{IN} – V_{LA} , I_{LA} = 75 mA	–	800	–	mV
Current Slew Time	$t_{FADE(MIN)}$	Current rising or falling between 10% and 90%, Fade disabled (see Fade pin description below)	–	10	–	µs
$\overline{EN}$ AND POL INPUTS						
$\overline{EN}$ Input Logic-Low Voltage	$V_{IL(EN)}$		–	–	0.8	V
$\overline{EN}$ Input Logic-High Voltage	$V_{IH(EN)}$		2	–	–	V
$\overline{EN}$ Input Current	$I_{LOGIC-IN(EN)}$		–2	–	2	µA
PWM Duty Cycle [5][6]	DC	PWM applied to $\overline{EN}$; 0 V ≤ V_{PWM} ≤ 5.25 V	0	–	100	%
PWM Frequency Range [5]	f_{PWM}	PWM applied to $\overline{EN}$; 0 V ≤ V_{PWM} ≤ 5.25 V	0	–	1	kHz
PWM Input Voltage	V_{PWM}	PWM applied to $\overline{EN}$	0	–	5.25	V
POL Input Logic-Low Voltage	$V_{IL(POL)}$		–	–	0.8	V
POL Average Leakage Current	$I_{LOGIC-IN(POL)}$	POL = GND	–	80	–	nA

Continued on next page...

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_A = –40°C to 125°C (Range K); T_A = –40°C to 85°C (Range E); V_{IN} = 7 to 24 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Units
LOGIC OUTPUTS						
Output On Voltage	$V_{OUT(SAT)}$	$\overline{SO}$, I_{OUT} = 20 mA, B > B_{OP}, POL = float	–	180	500	mV
Output Current Limit	$I_{OUTPUT(SINK)C}$	$\overline{SO}$, T_J < $T_{J(max)}$	30	–	60	mA
Output Rise Time	t_r	$\overline{SO}$, R_L = 820 Ω, C_S = 20 pF	–	0.2	–	µs
Output Fall Time	t_f	$\overline{SO}$, R_L = 820 Ω, C_S = 20 pF	–	0.1	–	µs
Power-On State	POS	$\overline{SO}$, POL = GND or POL = float		HIGH		–
ANALOG INPUTS						
Input Voltage Range	V_{INPUT}	IREF, FADE	0	–	5.5	V
PROTECTION						
Short Detect Voltage	V_{SCD}	Measured at LA	1.2	–	1.8	V
Short Circuit Source Current	I_{SCS}	Short present LA to GND	–	1	–	mA
Short Release Voltage Hysteresis	V_{SChys}		–	350	–	mV
Thermal Monitor Activation Temperature	T_{JM}		–	130	–	°C
Thermal Monitor Slope	$\Delta I_{SEN}/\Delta T_J$		–	–3.25	–	%/°C
Thermal Monitor Low Current Temperature	T_{JL}		–	150	–	°C
Overtemperature Shutdown	T_{JF}	Temperature increasing	–	170	–	°C
Overtemperature Hysteresis	T_{Jhys}		–	15	–	°C
MAGNETIC CHARACTERISTICS [7]						
Operate Point	B_{OPS}	$\lvert B_{FIELD}\rvert > \lvert B_{OP}\rvert$	–	40	70	G
	B_{OPN}		–70	–40	–	G
Release Point	B_{RPS}	$\lvert B_{FIELD}\rvert < \lvert B_{RP}\rvert$	5	25	–	G
	B_{RPN}		–	–25	–5	G
Hysteresis	B_{HYS}	$\lvert B_{OPX} - B_{RPX}\rvert$	5	15	25	G

[1] Typical data is at T_A = 25°C and V_{IN} = 12 V.
[2] Resistor tolerance is not included.
[3] When EN = low, $E_{ILA} = 100 \times [(\lvert I_{LA} \rvert \times R_{IREF} / 90) - 1]$, with I_{LA} in mA and R_{IREF} in kΩ.
[4] Current Accuracy cannot be guaranteed once the device is in Thermal Monitor Actuation Protection.
[5] Guaranteed by design, not tested in production.
[6] At high PWM input frequencies, the current slew time may not provide sufficient time for I_{LA} to reach either the user-selected maximum current or minimum current as the duty cycle approaches 0% and/or 100%. See Dimming Frequency and Duty Cycle section.
[7] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields and is a positive value for south-polarity magnetic fields.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Value	Units
Thermal Resistance (Junction to Ambient)	$R_{\theta JA\ (High\text{-}K)}$	JEDEC Package MS-012 BA. Test is performed using a high thermal conductivity, multilayer printed circuit board that approximates those specified in the JEDEC standards JESD51-7. Thermal vias are included per JESD51-5. See Figure 2 for more detail.	35	°C/W
	$R_{\theta JA\ (Usual\text{-}K)}$	JEDEC Package MS-012 BA. Multiple measurement points on both single- and dual-layer printed circuit boards with minimal exposed copper (2-oz) area. See Figure 2 for more detail.	62-147	°C/W

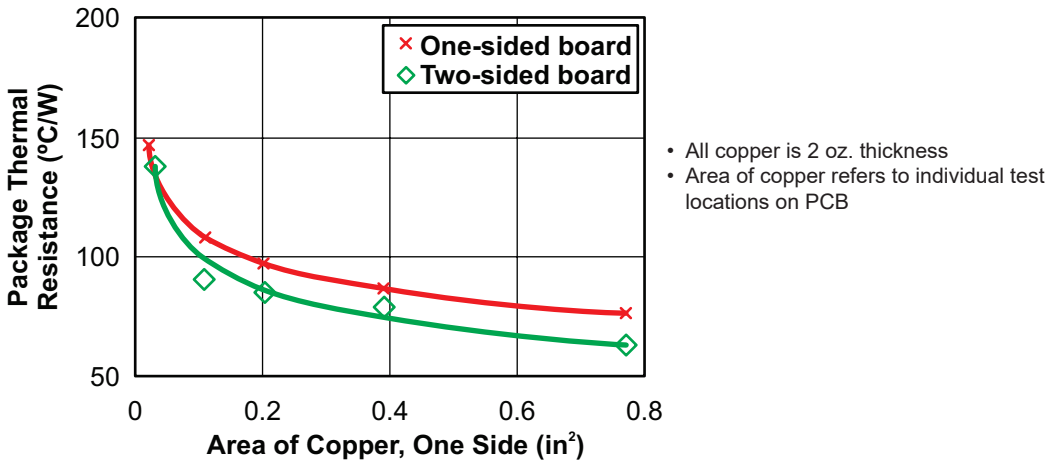

Figure 2: Thermal Resistance ($R_{\theta JA}$) versus Copper Area on Printed Circuit Board (PCB)

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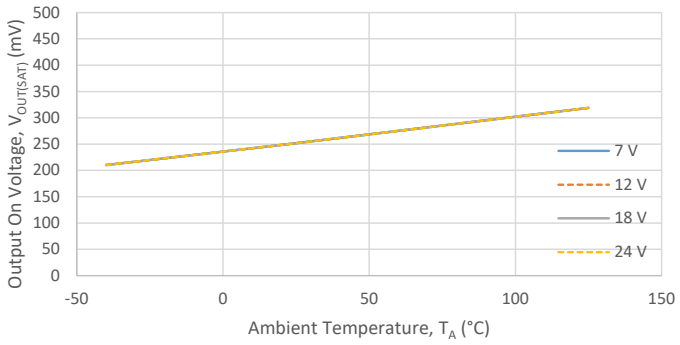
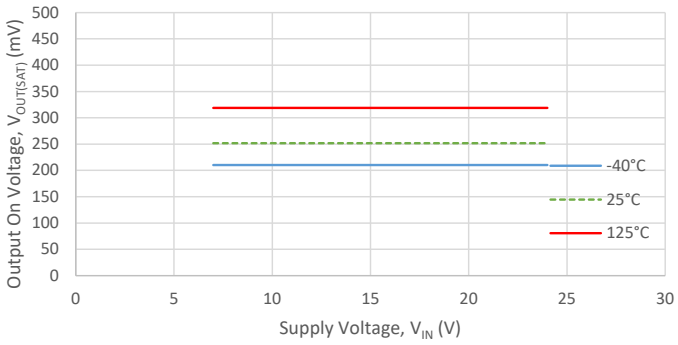
CHARACTERISTIC PERFORMANCE

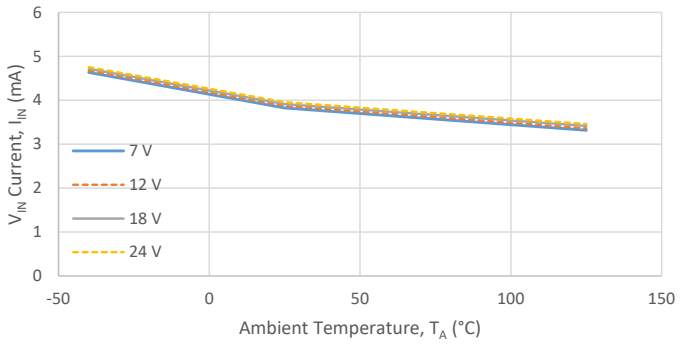
Output On Voltage ($V_{OUT(SAT)}$ v. T_A)



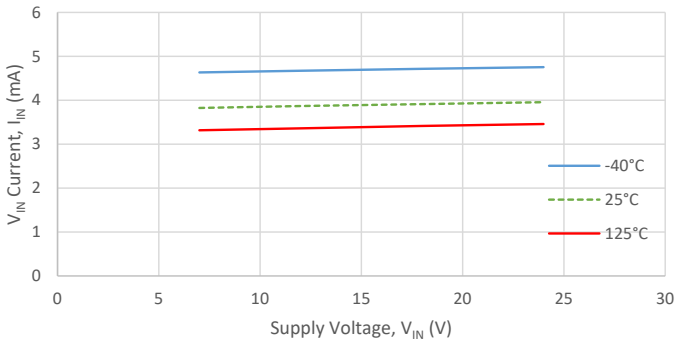
Output On Voltage ($V_{OUT(SAT)}$ v. V_{IN})



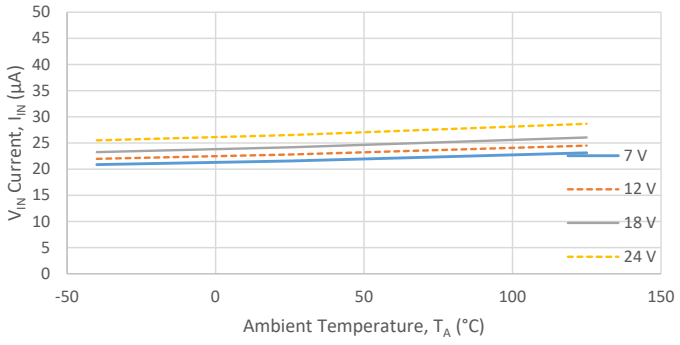
V_{IN} Active Current ($I_{IN(ACT)}$ v. T_A)



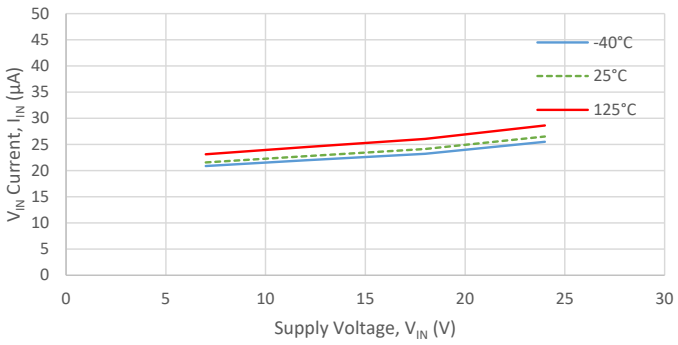
V_{IN} Active Current ($I_{IN(ACT)}$ v. V_{IN})



V_{IN} Average Current (I_{INAVG} v. T_A)



V_{IN} Average Current (I_{INAVG} v. V_{IN})



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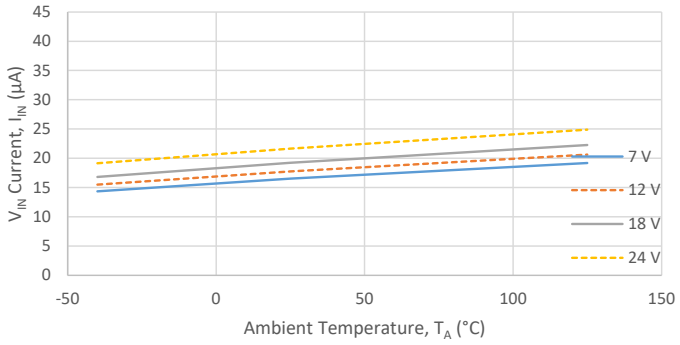
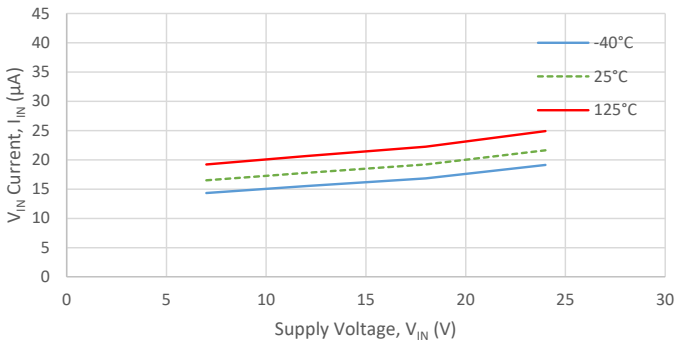
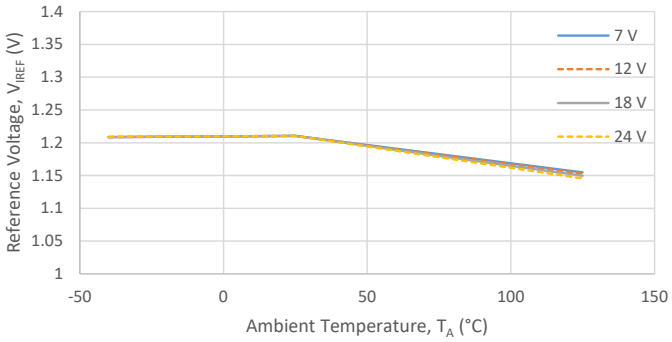
V_{IN} Quiescent Current (I_{INQ} v. T_A)



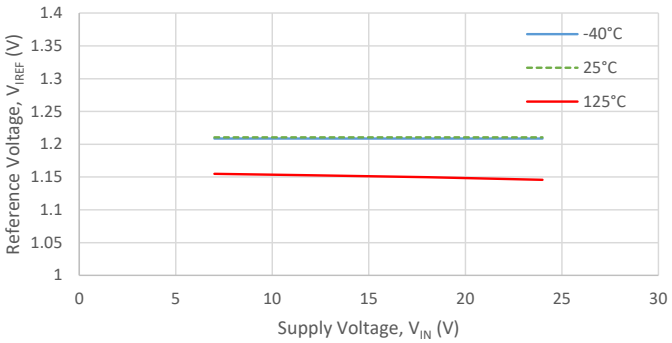
V_{IN} Quiescent Current (I_{INQ} v. V_{IN})



Reference Voltage (V_{IREF} v. T_A)

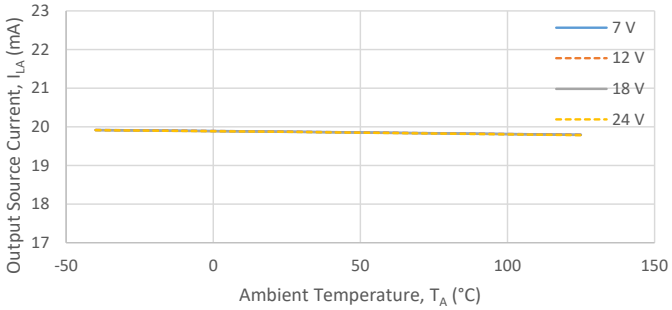


Reference Voltage (V_{IREF} v. V_{IN})



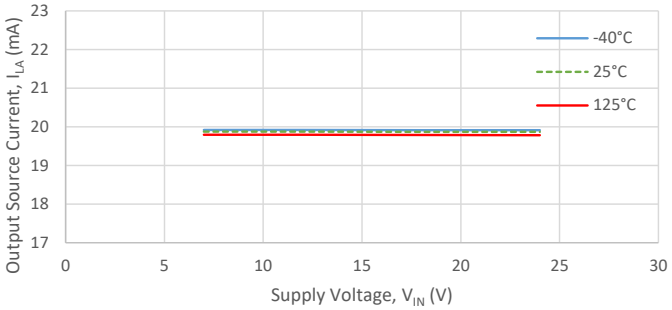
Output Source Current (I_{LA} v. T_A)

I_{REF} = 0.267 mA



Output Source Current (I_{LA} v. V_{IN})

I_{REF} = 0.267 mA



For Output Source Current and Reference Current Ratio, the Thermal Monitor Activation is disabled during test.

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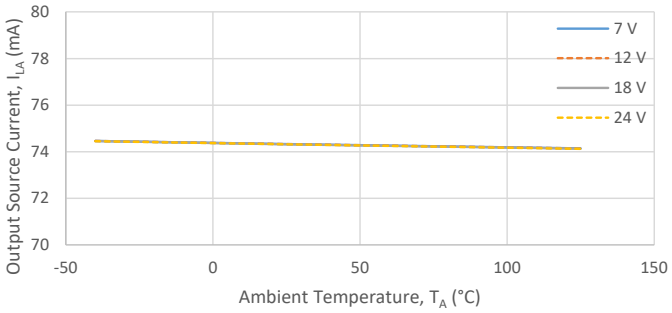
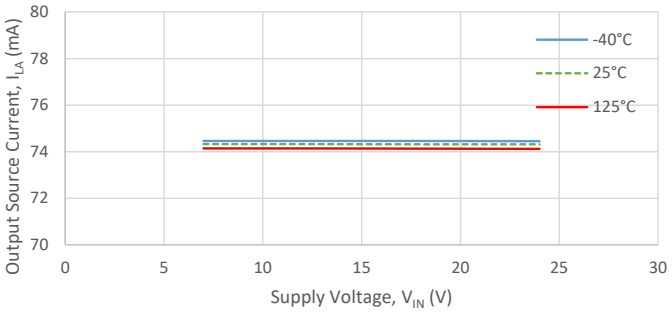
Output Source Current (I_{LA} v. T_A)

I_{REF} = 1.0 mA



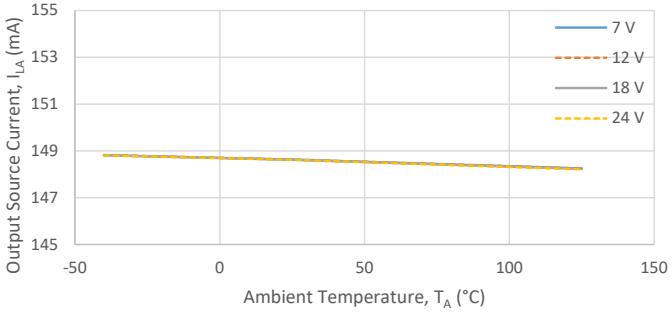
Output Source Current (I_{LA} v. V_{IN})

I_{REF} = 1.0 mA



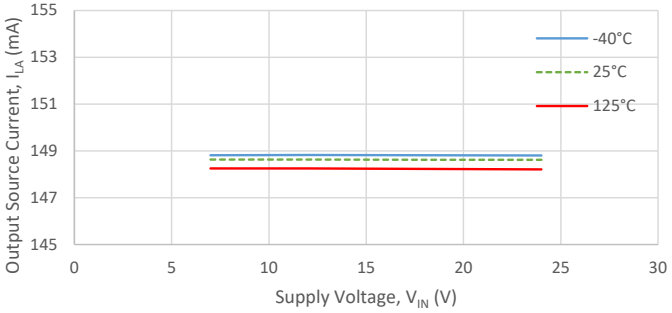
Output Source Current (I_{LA} v. T_A)

I_{REF} = 2.0 mA



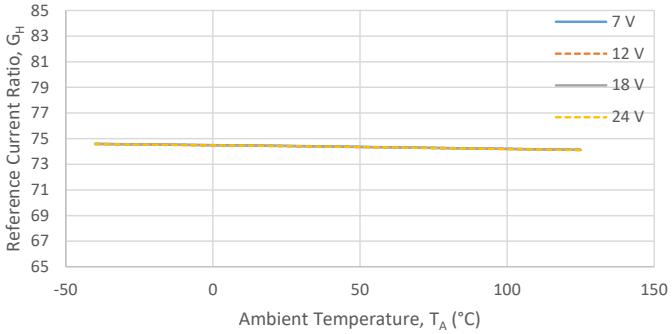
Output Source Current (I_{LA} v. V_{IN})

I_{REF} = 2.0 mA



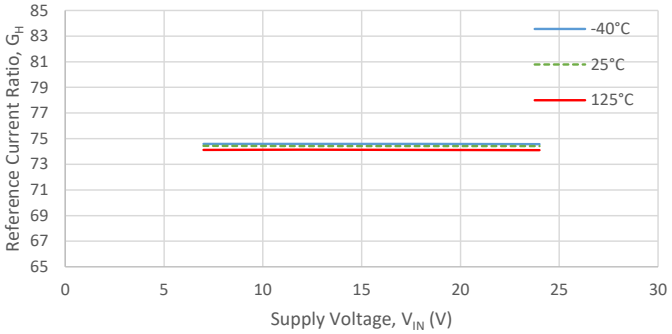
Reference Current Ratio (G_H v. T_A)

I_{REF} = 0.267 mA



Reference Current Ratio (G_H v. V_{IN})

I_{REF} = 0.267 mA



For Output Source Current and Reference Current Ratio, the Thermal Monitor Activation is disabled during test.

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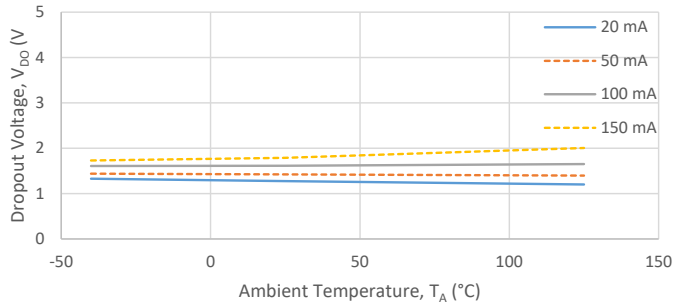
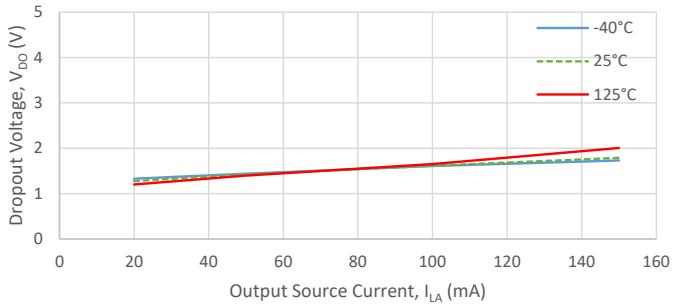
Dropout Voltage (V_{DO} v. T_A)

V_{IN} = 7 V

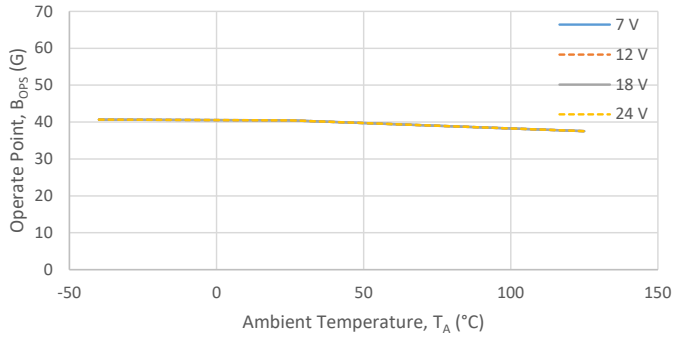


Dropout Voltage (V_{DO} v. I_{LA})

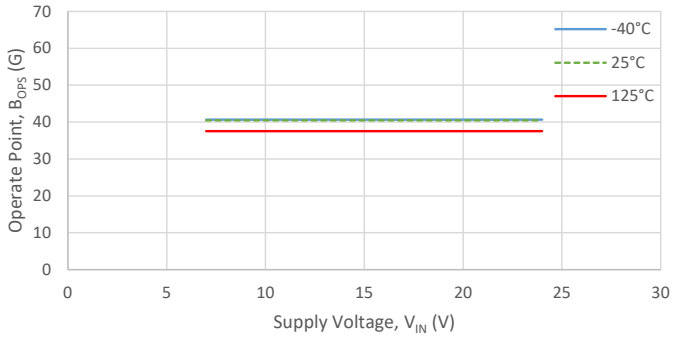
V_{IN} = 7 V



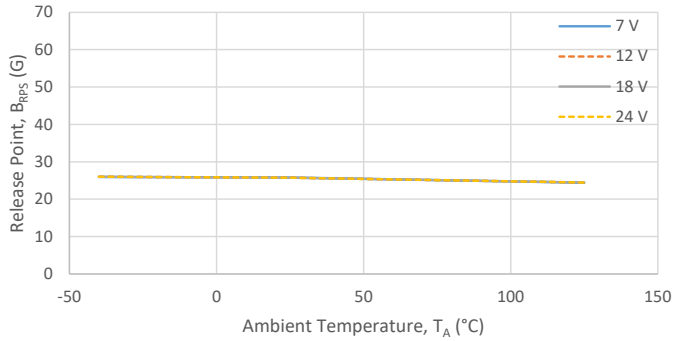
Operate Point, South (B_{OPS} v. T_A)



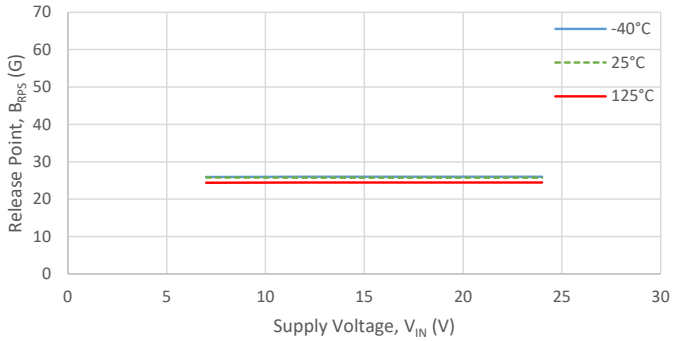
Operate Point, South (B_{OPS} v. V_{IN})



Release Point, South (B_{RPS} v. T_A)



Release Point, South (B_{RPS} v. V_{IN})



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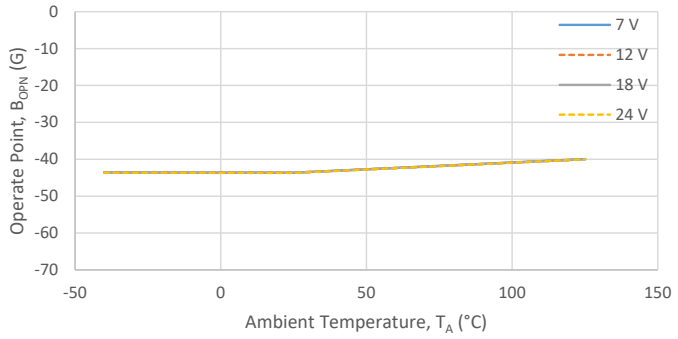
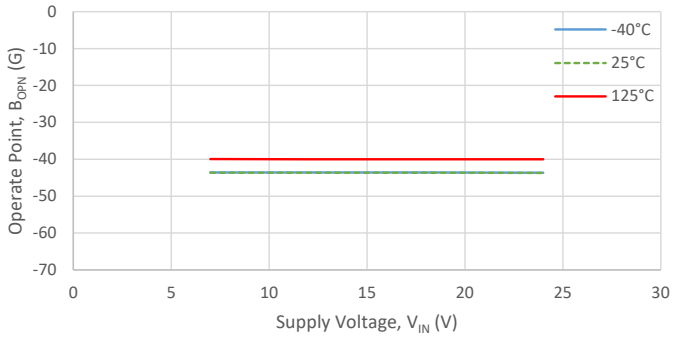
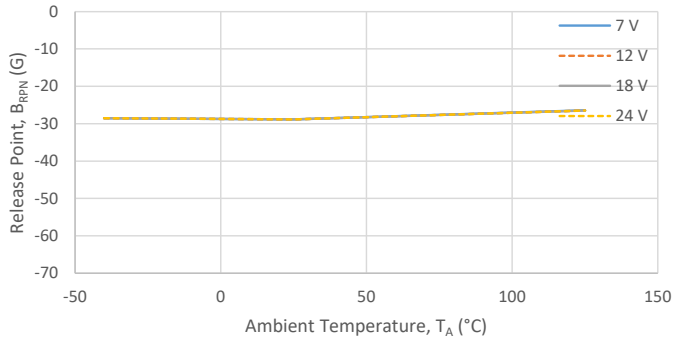
Operate Point, North (B_{OPN} v. T_A)



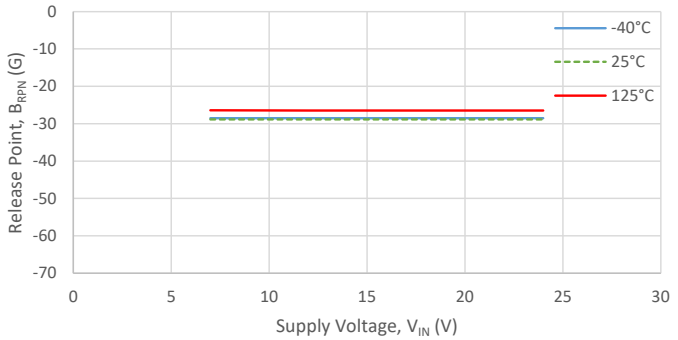
Operate Point, North (B_{OPN} v. V_{IN})



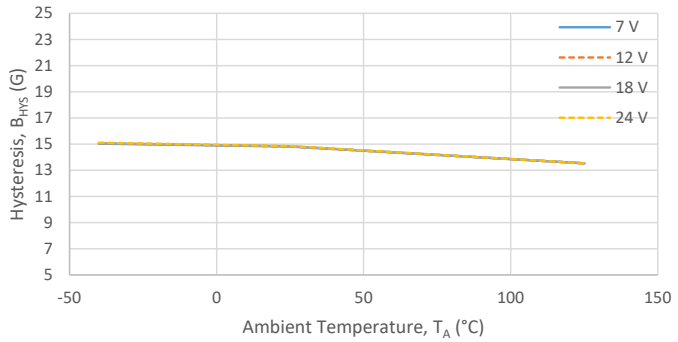
Release Point, North (B_{RPN} v. T_A)



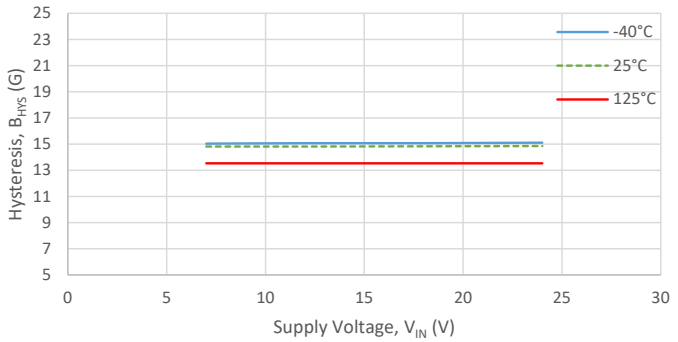
Release Point, North (B_{RPN} v. V_{IN})



Hysteresis (B_{HYS} v. T_A)



Hysteresis (B_{HYS} v. V_{IN})



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FUNCTIONAL DESCRIPTION

Overview

The APS13568 is an integrated Hall-effect switch with a linear current regulator which is designed to provide drive current and protection for a string of series connected high-brightness LEDs in automotive applications. It provides a single programmable current output sourcing up to 150 mA, with low dropout voltage.

The APS13568 is designed for illumination applications where the LED activity is controlled by the integrated Hall-effect switch, external logic, or by a PWM input signal such as from an MCU (microcontroller).

Current regulation is maintained and the LEDs are protected during a short to ground at any point in the LED string. A short to ground on the output terminal will disable the output until the short is removed. Integrated thermal management reduces the regulated current level at high internal junction temperatures to limit power dissipation.

Omnipolar Operation

The integrated Hall-effect switch in the APS13568 is an omnipolar switch. The output switches when a magnetic field perpendicular to the Hall sensor exceeds the operate point threshold, B_{OPx} ($B > B_{OPS}$ or $B < B_{OPN}$). When magnetic field is reduced below the release point, B_{RPx} ($B < B_{RPS}$ or $B > B_{RPN}$), the device output goes to the other state. The output transistor is capable of sinking current up to the short-circuit current limit, I_{OM}, which ranges from 30 to 60 mA. The difference in the magnetic operate and release points is the hysteresis, B_{HYS}, of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Removal of the magnetic field results in an output state consistent with $B < B_{RPx}$. Since the output state polarity relative to the magnetic thresholds is user-selectable via the POL pin, reference Table 1 to determine the expected output state.

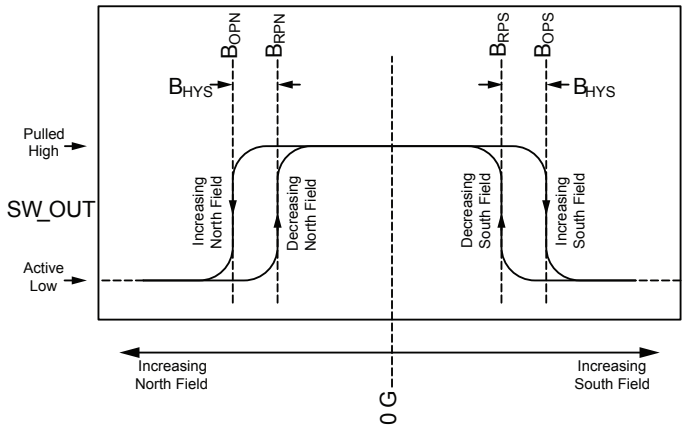

Figure 3: Hall Switch Output ($\overline{SO}$) State versus Magnetic Field (POL = float)

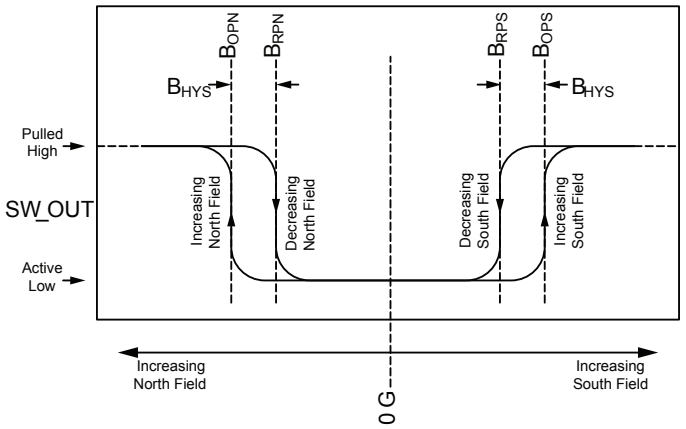

Figure 4: Hall Switch Output ($\overline{SO}$) State versus Magnetic Field (POL = GND)

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Pin Functions

VIN

Supply to the micro-power control circuit and current regulator. A ceramic bypass capacitor, typically 100 nF, should be connected as close as possible to this pin and GND. See Figure 1 typical application circuit.

$\overline{SO}$

Active-low open-drain output of the Hall-effect switch (requires pull-up resistor, R_{PU}). The output polarity of $\overline{SO}$ depends on the configuration of the POL pin. See Figure 3 and Figure 4 and Table 1. Drives low when $B_{FIELD} > |B_{OP}|$ when POL = float, or pulled high through a pull-up resistor on $\overline{SO}$ when POL = GND.

POL

Inverts $\overline{SO}$ polarity, as shown in Table 1. See Figure 3 and Figure 4.

Table 1: $\overline{SO}$ State Truth Table (POL)

POL	B_{FIELD}	$\overline{SO}$ State
GND	$\|B\| > \|B_{OP}\|$	High
	$\|B\| < \|B_{RP}\|$	Low
Float	$\|B\| > \|B_{OP}\|$	Low
	$\|B\| < \|B_{RP}\|$	High

POL should only be tied to ground or floated to achieve the desired output polarity. The LED driver is only enabled when the $\overline{EN}$ pin is pulled low. If $\overline{SO}$ is tied to $\overline{EN}$, changing the $\overline{SO}$ polarity changes the behavior between LED *off* (POL = GND) and LED *on* (POL = Float) with a magnet present.

$\overline{EN}$

Active-low logic input to enable/disable the LED driver.

Table 2: LED Driver State Truth Table ($\overline{EN}$)

$\overline{EN}$ State	LED Driver State
Low	LED Driver Enabled; Device is in Active Mode
High	LED Driver Disabled; Device operates in Micropower Mode

This provides direct on/off action and can be used for PWM control when the fade function is disabled. See FADE pin description below. Tie to $\overline{SO}$ for standalone APS13568 operation.

FADE

A capacitor between this pin and GND controls the turn-on and turn-off times of the LED current. To disable the fade feature, omit C_{FADE} and float the FADE pin.

IREF

A 1.2 V reference used to set the LED current drive. Connect resistor R_{IREF} to GND to set the reference current. See Equation 1.

LA

Current source output connected to the anode of the first LED in the string.

GND

Ground reference connection. This pin should be connected directly to the negative supply.

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PAD

Isolated pad for thermal dissipation only. It may be left floating, but it is recommended to connect this pad to ground.

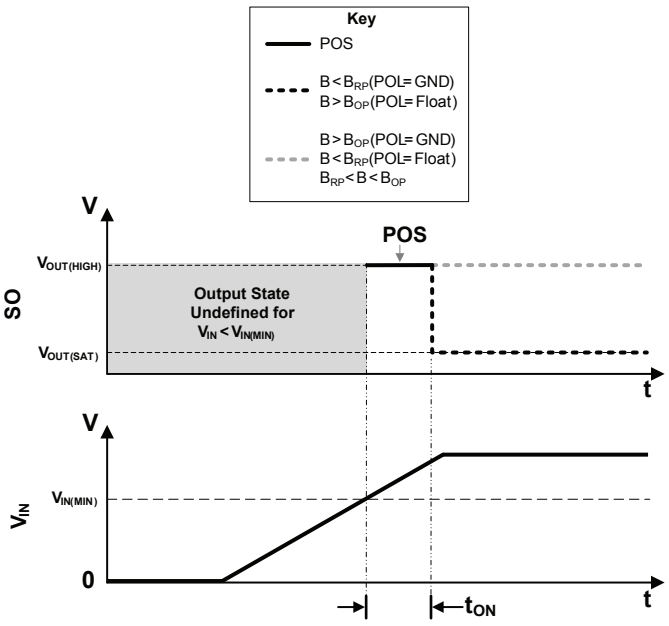

Figure 5: Power-On Timing

Power-On Behavior

Device power-on occurs once t_{ON} has elapsed. During the time prior to t_{ON}, and after $V_{IN} > V_{IN(min)}$, the output state is high, regardless of the POL configuration. After t_{ON} has elapsed, the output will correspond with the applied magnetic field for $B > B_{OP}$ or $B < B_{RP}$. See Figure 5 for an example.

Powering-on the device in the hysteresis range (less than B_{OPx} and greater than B_{RPx}) causes the output state to be high. The correct state is attained after the first excursion beyond B_{OPx} or B_{RPx}.

LED Current Level

The LED current is controlled by a linear current regulator between the VIN pin and the LA output. The basic equation that determines the nominal output current at this pin is:

Given that the LED driver is enabled (see Table 1),

$$I_{LA} = \frac{V_{REF} \times G_H}{R_{IREF}} \quad (1)$$

where I_{LA} is in A and R_{IREF} is in Ω; $V_{REF} \times G_H$ is 90.

Note: the output current may be reduced from the set level by the thermal monitor circuit.

Conversely, the reference resistor may be calculated from:

$$R_{IREF} = \frac{V_{REF} \times G_H}{I_{LA}} \quad (2)$$

where I_{LA} is in A, R_{IREF} is in Ω, V_{REF} = 1.2 V, and G_H = 75.

For example, where the required current is 75 mA, the resistor value will be:

$$R_{IREF} = \frac{1.2\ V \times 75}{0.075\ A} = 1.2\ k\Omega \quad (3)$$

It is important to note that because the APS13568 is a linear current regulator, the maximum regulated current is limited by the power dissipation and thermal management in the application. All current calculations assume an adequate heat sink and/or airflow for the power dissipated. The application section below provides further detail on thermal management and the associated limitations.

Fade-In/Fade-Out

Fade timing is controlled by external capacitor, C_{FADE}, on the FADE pin. A larger capacitor will result in a longer fade time. The 10%-90% fade time is approximated by the equation:

$$t_{FADE} = C_{FADE} \times 0.8 \times 10^6 \quad (4)$$

where t_{FADE} is in seconds and C_{FADE} is in farads.

Fade-in is triggered when the LED driver is enabled and fade-out is triggered when the LED driver is disabled (see Table 1).

To disable the fade feature, omit C_{FADE} and float the FADE pin.

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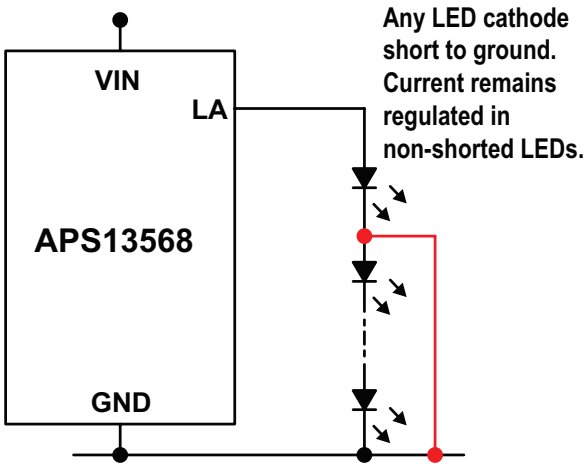

Figure 6: Any Cathode Short to Ground

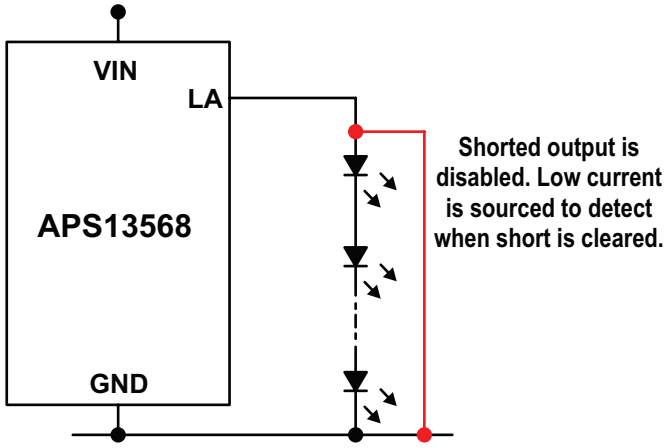

Figure 7: Output Short to Ground

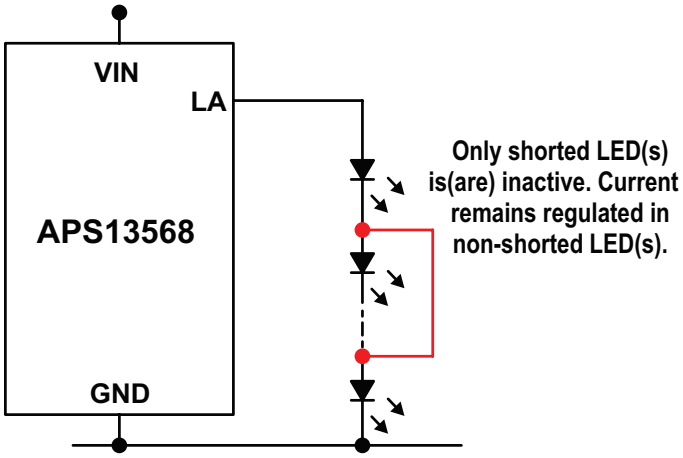

Figure 8: Shorted LED(s)

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Dimming Frequency and Duty Cycle

Dimming of the LED can be controlled by applying a pulse-width-modulated (PWM) signal to the $\overline{EN}$ pin (see Table 2). The duty cycle of the PWM directly correlates to the duty cycle of the LED current, provided that the fade function is disabled (see Fade pin description above). This controls the relative LED on-time versus off-time and changes the perceived brightness of the LED.

The $\overline{EN}$ pin is rated for the full range of V_{IN} and therefore when tied directly to the $\overline{SO}$ pin, V_{IN} can be used as the pull-up supply for $\overline{SO}$.

When using the PWM capabilities, the PWM input voltage (V_{PWM}) applied to the $\overline{EN}$ pin should be in the range of 0 to 5.25 V. The $\overline{EN}$ input has typical TTL switching thresholds, but exceeding 5.25 V may cause pulse-width (duty-cycle) distortion. The PWM input frequency (f_{PWM}) can be as high as 1 kHz.

The combination of the external response time (t_{EXT_ON}) and I_{LA} current slew time (t_{FADE}) may not provide sufficient time for the desired/user-set LA on and off current levels to be reached when $\overline{EN}$ is pulsed with short on/off times. See Figure 9 and Figure 10.

This only affects the proportionality between the input PWM duty cycle on $\overline{EN}$ and LA duty cycle (and therefore average LA current) at higher PWM carrier frequencies in conjunction with very low or very high duty cycle (see Figure 11).

Figure 11 shows that with 100 Hz PWM frequency, all duty cycles from 0% to 100% are capable of producing an output current equal to the user-set I_{LA} level. However, at 1 kHz PWM frequency, duty cycles from 95% to 100% produce an output which does not reach the user-set I_{LA} current. The user's PWM algorithm can adjust the duty cycle range accordingly.

For example, with a PWM frequency of 1 kHz and duty cycle of 1% or 99%, the $\overline{EN}$ on time is 1% × 1 kHz = 10 µs. The external response time (t_{EXT_ON}) and I_{LA} current slew time (t_{FADE}) is 50 µs (typ) + 10 µs (typ).

Safety Features

The circuit includes several features to ensure safe operation and to protect the LEDs and the APS13568:

- The current regulator between VIN and LA output provide a natural current limit due to the regulation.
- The LA output includes a short-to-ground detector that will disable the output to limit the dissipation.
- The thermal monitor reduces the regulated current as the temperature rises.
- Thermal shutdown completely disables the outputs under extreme overtemperature conditions.

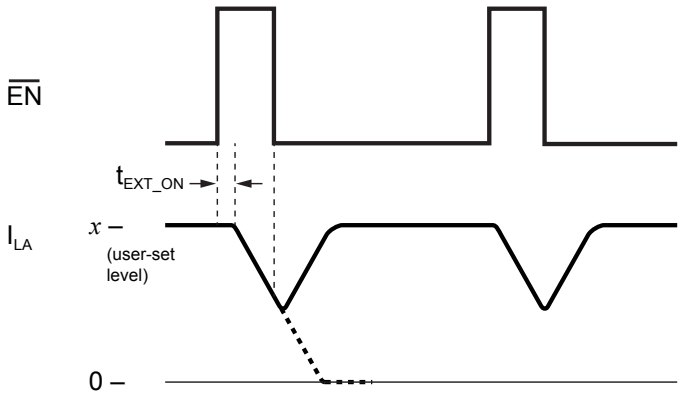

Figure 9: Low PWM Duty Cycle

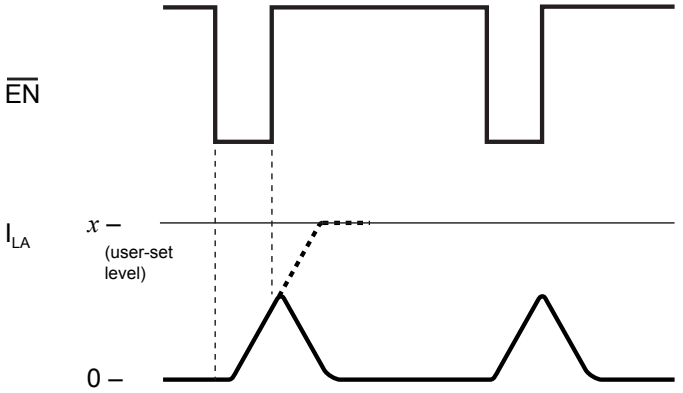

Figure 10: High PWM Duty Cycle

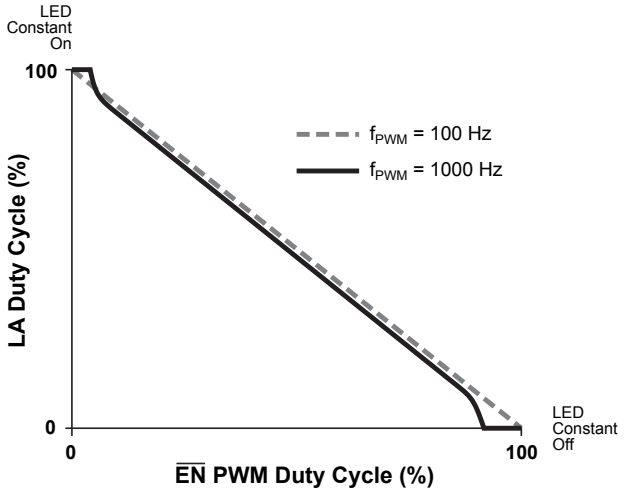

Figure 11: LA Duty Cycle vs. $\overline{EN}$ PWM Duty Cycle

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SHORT-CIRCUIT DETECTION

A short to ground on an LED cathode as in Figure 6 will not result in a short-to-ground fault condition. The current through the remaining LEDs will remain in regulation and the LEDs will be protected. If the LA output is pulled below the short detect voltage as in Figure 7, it will disable the driver output. A small current will be sourced from the disabled output to monitor the short and detect when it is removed. When the voltage at LA rises above the short detect voltage, the driver will be re-enabled. A shorted LED or LEDs in a multi-LED string, as in Figure 8, will not result in a short fault condition. The current through the remaining LEDs will remain in regulation and the LEDs will be protected. Thermal protection will still operate normally in all described LED short-circuit conditions. Short-circuit detection is shut off to minimize power consumption when the LED driver is disabled.

Temperature Monitor and Thermal Protection

The temperature monitor function included in the APS13568 reduces the LED current as the silicon junction temperature increases (see Figure 12). As the junction temperature of the APS13568 increases, the regulated current level is reduced, reducing the dissipated power in the APS13568 and in the LEDs. The current is reduced from the 100% level at typically 3.25%/°C until the point at which the current drops to 25% of the full value, defined at T_{JL}. Above this temperature, the current will continue to reduce at a lower rate until the temperature reaches the over-temperature shutdown threshold temperature, T_{JF}.

If the chip temperature exceeds the overtemperature limit T_{JF}, the driver will be disabled. The temperature will continue to be monitored and the regulator will be re-activated when the temperature drops below the threshold provided by the specified hysteresis. Note that it is possible for the APS13568 to transition rapidly between thermal shutdown and normal operation. This can happen if the thermal mass attached to the exposed thermal pad is small and T_{JM} is increased to close to the shutdown temperature. The period of oscillation will depend on T_{JM}, the dissipated power, the thermal mass of any heatsink present, and the ambient temperature.

By mounting the APS13568 in close proximity and on the same thermal substrate as the LEDs, this feature can also be used to limit the dissipation of the LEDs.

Micropower Operation

The built-in micropower control periodically activates the Hall switch circuitry for a short period of time (t_{AWAKE}), and deactivates it for the remainder of the period (t_{PERIOD}). The short duration awake state allows for sensor stabilization prior to sampling the Hall switch and latching the state on the $\overline{SO}$ output. If the $\overline{SO}$ output state is off (high), it is kept high during the sleep period; updates to the output from the off-state only occur at the end of the Active (t_{AWAKE}) pulse. If the output state is on (low), the Hall switch circuitry will remain awake until the output switches back off. The IC's supply current is not affected by the output state, provided the LED driver is disabled. The micropower control operates independently of the LED driver state. If $\overline{EN}$ is forced low by an external circuit, the device will also remain in the awake mode.

At power-on, the APS13568 will sample a t_{AWAKE} cycle before the first t_{SLEEP} cycle.

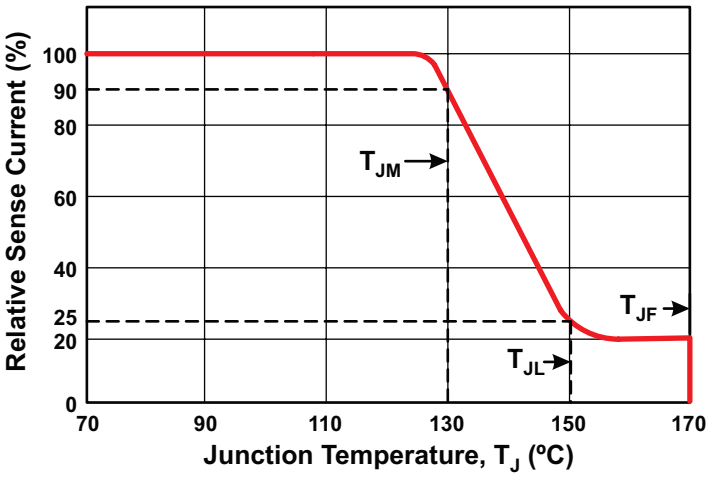

Figure 12: Temperature Monitor Current Reduction

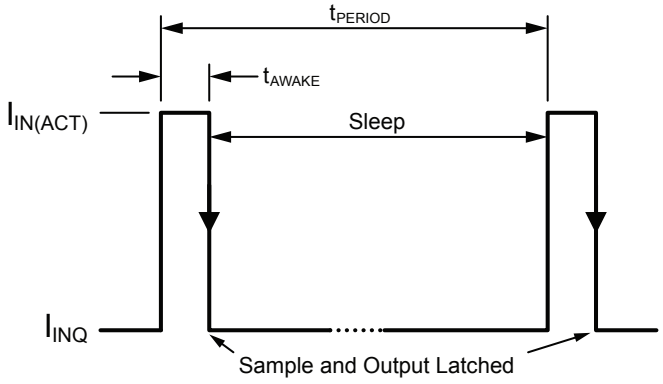

Figure 13: Micropower Timing Diagram

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APPLICATION INFORMATION

Power Dissipation

The most critical design consideration when using a linear regulator such as the APS13568 is the power produced internally as heat and the rate at which that heat can be dissipated.

There are three sources of power dissipation in the APS13568:

- The quiescent power to run the control circuits
- The power in the reference circuit
- The power due to the regulator voltage drop

QUIESCENT POWER

The quiescent power is the product of the quiescent current (I_{INQ}) and the supply voltage (V_{IN}), and it is not related to the regulated current. The quiescent power (P_Q) is therefore defined as:

$$P_Q = V_{IN} \times I_{INQ} \quad (5)$$

REFERENCE POWER

The reference circuit draws the reference current from the supply and passes it through the reference resistor to ground. The reference circuit power is the product of the reference current and the difference between the supply voltage and the reference voltage, typically 1.2 V. The reference power (P_{REF}) is therefore defined as:

$$P_{REF} = \frac{(V_{IN} - V_{REF}) \times V_{REF}}{R_{IREF}} \quad (6)$$

REGULATOR POWER

In most application circuits, the largest dissipation will be produced by the output current regulator. The power dissipated the current regulator is simply the product of the output current and the voltage drop across the regulator. The regulator power the output is defined as:

$$P_{REG} = (V_{IN} - V_{LED}) \times I_{LED} \quad (7)$$

Note that the voltage drop across the regulator (V_{REG}) is always greater than the specified minimum dropout voltage (V_{DO}). The output current is regulated by making this voltage large enough to provide the voltage drop from the supply voltage to the total forward voltage of all LEDs in series (V_{LED}). The total power dissipated in the APS13568 is the sum of the quiescent power, the reference power, and the power in the regulator:

$$P_D = P_Q + P_{REG} - P_{REF} \quad (8)$$

The power that is dissipated in the LEDs is:

$$P_{LED} = V_{LED} \times I_{LED} \quad (9)$$

where V_{LED} is the voltage across all LEDs in the string.

From these equations (and as illustrated in Figure 12), it can be seen that, if the power in the APS13568 is not limited, then it will increase as the supply voltage increases while the power in the LEDs will remain constant.

Dissipation Limits

The thermal shutdown feature limits the power that can be dissipated by the APS13568.

THERMAL SHUTDOWN

If the thermal resistance from the APS13568 to the ambient environment is high, then the silicon temperature will rise to the thermal shutdown threshold and the LED current will be disabled. After the current is disabled the power dissipated will drop and the temperature will fall. When the temperature falls by the hysteresis of the thermal shutdown circuit, the driver will be re-enabled and the temperature will start to rise again. This cycle will repeat continuously until the ambient temperature drops or the APS13568 is switched off. The period of this thermal shutdown cycle will depend on several electrical, mechanical, and thermal parameters.

Supply Voltage Limits

In many applications, especially in automotive systems, the available supply voltage can vary over a two-to-one range, or greater when double battery or load dump conditions are taken into consideration. In such systems, it is necessary to design the application circuit such that the system meets the required performance targets over a specified voltage range.

To determine this range when using the APS13568, there are two limiting conditions:

- For maximum supply voltage, the limiting factor is the power that can be dissipated from the regulator without exceeding the

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temperature at which the thermal foldback starts to reduce the output current below an acceptable level.

- For minimum supply voltage, the limiting factor is the maximum dropout voltage of the regulator, where the difference between the load voltage and the supply is insufficient for the regulator to maintain control over the output current.

Minimum Supply Limit: Regulator Saturation Voltage

The supply voltage (V_{IN}) is always the sum of the voltage drop across the high-side regulator (V_{REG}) and the forward voltage of the LEDs in the string (V_{LED}).

V_{LED} is constant for a given current and does not vary with supply voltage. Therefore, V_{REG} provides the variable difference between V_{LED} and V_{IN}. V_{REG} has a minimum value below which the regulator can no longer be guaranteed to maintain the output current within the specified accuracy. This level is defined as the regulator dropout voltage (V_{DO}).

The minimum supply voltage, below which the LED current does not meet the specified accuracy, is therefore determined by the sum of the minimum dropout voltage (V_{DO}) and the forward voltage of the LEDs in the string (V_{LED}). The supply voltage must always be greater than this value and the minimum specified supply voltage, that is:

$$V_{IN} > V_{DO} + V_{LED} \text{ and } V_{IN} > V_{IN(MIN)} \quad (10)$$

As an example, consider a string of two white LEDs, running at 150 mA, with each LED forward voltage at 3.15 V. The minimum supply voltage will be approximately:

$$V_{IN(MIN)} = 0.8 + (2 \times 3.15) = 7.1 \text{ V} \quad (11)$$

Maximum Supply Limit: Thermal Limitation

As described above, when the silicon temperature reaches the thermal shutdown threshold the thermal protection feature causes the output current to be disabled. The maximum supply voltage is therefore defined as the voltage above which the LED current drops below the acceptable minimum.

This can be estimated by determining the maximum power that can be dissipated before the internal (junction) temperature of the APS13568 reaches the thermal shutdown threshold.

The maximum power dissipation is defined as:

$$P_{D(MAX)} = \frac{\Delta T_{(MAX)}}{R_{\theta JA}} \quad (12)$$

where $\Delta T_{(MAX)}$ is the difference between the thermal protection activation temperature of the APS13568 and the maximum ambient temperature T_A(max), and $R_{\theta JA}$ is the thermal resistance from the internal junctions in the silicon to the ambient environment.

Thermal Dissipation

The amount of heat that can pass from the silicon of the APS13568 to the surrounding ambient environment depends on the thermal resistance of the structures connected to the APS13568. The thermal resistance ($R_{\theta JA}$) is a measure of the temperature rise created by power dissipation and is usually measured in degrees Celsius per watt (°C/W).

The temperature rise (ΔT) is calculated from the power dissipated (P_D) and the thermal resistance ($R_{\theta JA}$) as:

$$\Delta T = P_D \times R_{\theta JA} \quad (13)$$

A thermal resistance from silicon to ambient ($R_{\theta JA}$) of approximately 35°C/W can be achieved by using a high thermal conductivity, multilayer printed circuit board as specified in the JEDEC standards JESD51-7 for JEDEC Package MS-012 BA (including thermal vias as called out in JESD51-5). Additional improvements may be achieved by optimizing the PCB design.

Optimizing Thermal Layout

The features of the printed circuit board, including heat conduction and adjacent thermal sources such as other components, have a significant effect on the thermal performance of the device. To optimize thermal performance, the following should be taken into account:

- Maximizing the forward voltage of the LEDs relative to the V_{IN} of the APS13568 will greatly reduce the power dissipated in the APS13568 by reducing the voltage drop across the APS13568.
- The APS13568 exposed thermal pad should be connected to as much copper area as is available. This copper area may be left floating or connected to ground if desired.
- Copper thickness should be as high as possible (for example, 2 oz. or greater for higher power applications).
- The greater the quantity of thermal vias, the better the

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dissipation. If the expense of vias is a concern, studies have shown that concentrating the vias directly under the device in a tight pattern, as shown in Figure 14, has the greatest effect.

- Additional exposed copper area on the opposite side of the board should be connected by means of thermal vias. The copper should cover as much area as possible.
- Other thermal sources should be placed as far away from the device as possible.

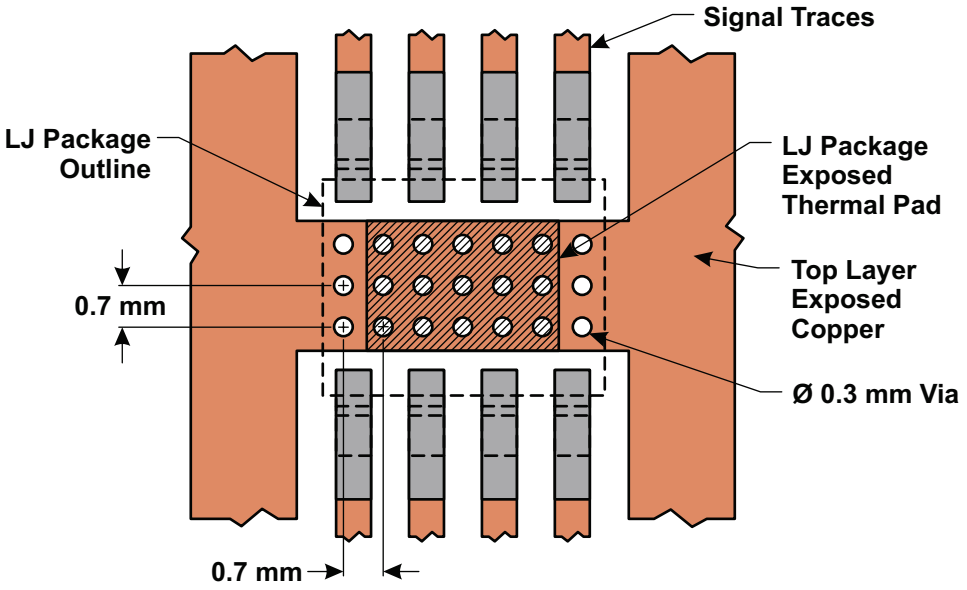

Figure 14: Suggested PCB Layout for Thermal Optimization

(Maximum available bottom-layer copper recommended)

Extensive applications information for Hall effect devices is available in:

- *Hall-Effect IC Applications Guide* (AN27701)
- *Soldering Methods for Allegro's Products — SMD and Through-Hole* (AN26009)
- *Guidelines for Designing Subassemblies Using Hall-Effect Devices* (AN27703.1)
- *Handling, Storage and Shelf Life of Semiconductor Devices* (AN296126)
- *Chemical Exposure of Devices* (AN295047)
- *Allegro Hall-Effect Sensor ICs* (AN296065)
- *Integrating Hall-Effect Magnetic Sensing Technology into Modern Household Appliances* (AN295046)
- *Omnipolar Switch Hall-Effect IC Basics* (AN296070)

All are provided on the Allegro website, www.allegromicro.com.

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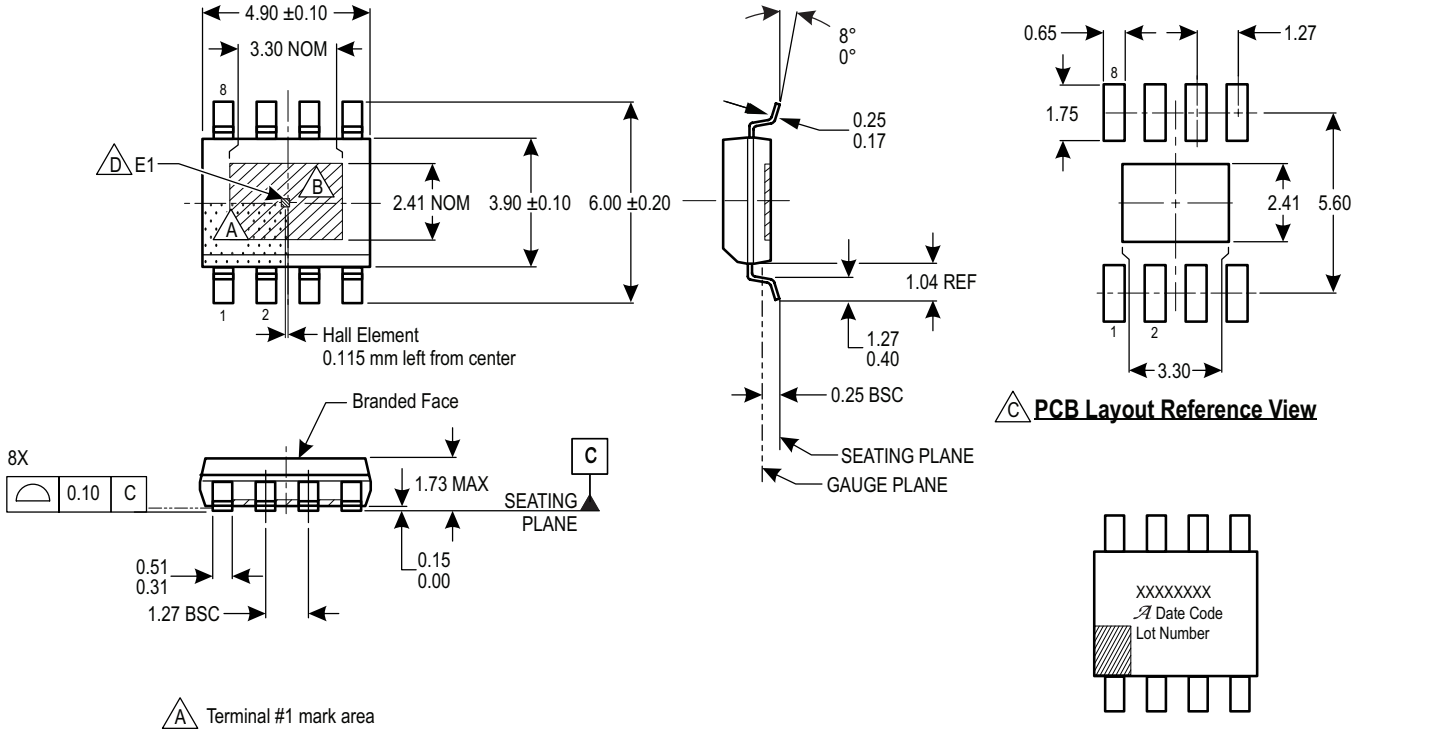
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000380, Rev. 2 and JEDEC MS-012BA)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-9AM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Hall element (E1) centered in package (not to scale).

E Branding scale and appearance at supplier discretion.

E Standard Branding Reference View

Lines 1, 2 = 8 characters.
Line 3 = 6 characters.

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of
Assembly Lot Number

Figure 15: Package LJ, 8-Pin SOICN with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	March 13, 2017	Initial release
1	February 11, 2019	Minor editorial updates
2	February 13, 2020	Minor editorial updates
3	February 10, 2022	Updated package drawing (page 21)

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