A4481

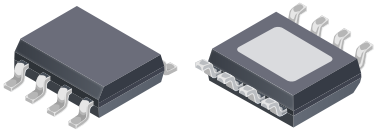
5 V_{OUT}, 50 mA Automotive Linear Regulator with 50 V Load Dump and Short-to-Battery Protection

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- 5.25 to 40 V_{IN} operating range, 50 V load dump rating
- 5 V ±1% internal LDO regulator
- Foldback short-circuit protection
- Short-to-battery protection (to 32 V, independent of V_{IN}) for harness faults
- Power OK (POK) flag
- High-voltage logic level enable input (ENB) for microprocessor control or connection directly to battery
- Pin-to-pin and pin-to-ground tolerant at every pin

Package:

8-pin SOIC with exposed thermal pad (suffix LJ)



Not to scale

DESCRIPTION

The A4481 is a single low-dropout linear regulator with complete control, diagnostics, and protection features that address many requirements of automotive applications. It regulates input voltages from 5.25 to 40 V, down to 5 V ±1% output voltage and is able to supply up to 50 mA of load current.

Diagnostic output from the A4481 includes Power OK (POK) output to alert the microprocessor that a fault has occurred.

Protection features include input undervoltage lockout (UVLO), foldback overcurrent protection, output undervoltage and overvoltage protections (UV/OVP), and thermal shutdown (TSD). In addition, the output is protected from a short-to-battery event up to 32 V.

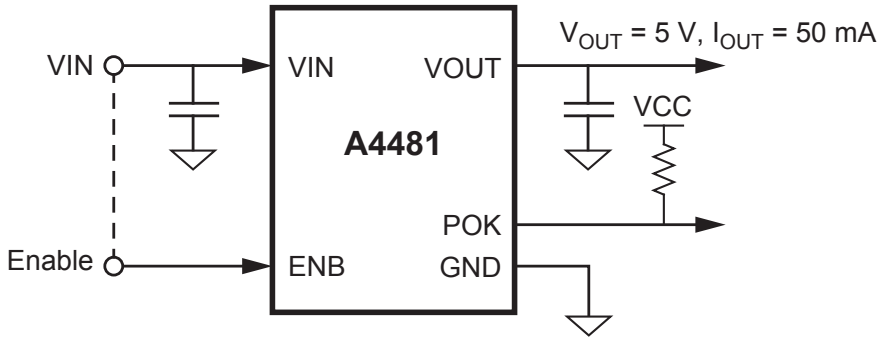
The A4481 device is available in an 8-pin SOIC package with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte-tin leadframe plating.

APPLICATIONS

Power supplies for:

- Microcontrollers
- Transceivers (CAN, LIN, etc.)
- Sensors

Typical Application Circuit



SELECTION GUIDE

Part Number	Temperature Range (°C)	Package	Packing*
A4481KLJTR-T	–40 to 150	8-pin eSOIC with exposed thermal pad	3000 pieces per 7-in. reel

*Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Notes	Rating	Unit
VIN, ENB Pins	V_{IN}, V_{ENB}		–0.3 to 50	V
VOUT Pin	V_{OUT}	Independent of VIN	–0.3 to 32	V
All other pins			–0.3 to 7	V
Junction Temperature Range	T_J(max)		–40 to 165	°C
Storage Temperature Range	T_{stg}		–40 to 150	°C

*Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

THERMAL CHARACTERISTICS:* May require derating at maximum conditions; see application section for optimization

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	eSOIC-8 (LJ) package	35	°C/W

*Additional thermal information available on the Allegro website.

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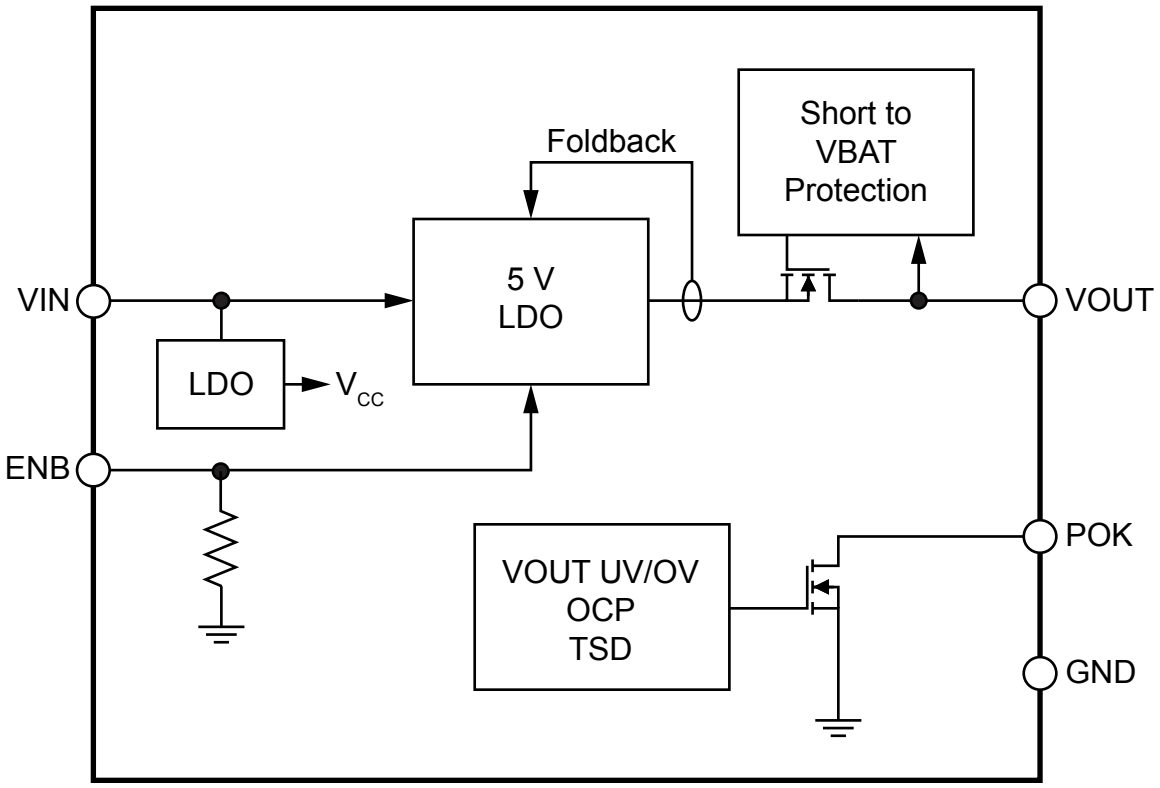
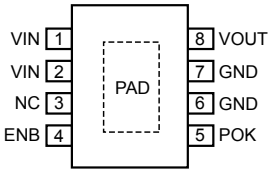
Functional Block Diagram



Pinout Diagram



Terminal List Table

Number	Name	Function
1	VIN	Input voltage pin
2	VIN	Input voltage pin
3	NC	No connect
4	ENB	Logic enable input from a microcontroller or DSP
5	POK	Open-drain regulator fault detection output
6	GND	Ground
7	GND	Ground
8	VOUT	5 V regulator output

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ELECTRICAL CHARACTERISTICS[1]: Valid at 5.25 V ≤ V_{INx} ≤ 40 V, −40°C ≤ T_A = T_J ≤ 150°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
INPUT VOLTAGE						
Operating Input Voltage	V_{IN}	ENB high	5.25	5.35	40	V
VIN UVLO Start Voltage	$V_{IN(START)}$	V_{IN} rising, ENB high	4.75	–	5.2	V
VIN UVLO Stop Voltage	$V_{IN(STOP)}$	V_{IN} falling, ENB high	4.55	–	5	V
VIN UVLO Hysteresis	$V_{IN(HYS)}$	$V_{IN(START)} – V_{IN(STOP)}$	–	0.2	–	V
INPUT CURRENT						
Input Quiescent Current[1]	I_Q	V_{IN} = 5.25 V, ENB high	–	3.4	–	mA
Input Sleep Supply Current[1]	$I_{Q(SLEEP)}$	V_{IN} = 5.25 V, ENB low	–	1	10	µA
5 V LINEAR REGULATOR						
Accuracy	V_{OUT}	I_{OUT} = 25 mA, V_{IN} = 5.25 V	4.95	5	5.05	V
Load Regulation		5 mA < I_{OUT} < 50 mA, V_{IN} = 5.25 V	–1	–	+1	%
Output Capacitance Range[2]	C_{OUT}		3	4.7	10	µF
Startup Time[2]	t_{START}	C_{OUT} ≤ 4.7 µF, Load = 100 Ω ±5% (50 mA)	0.7	1.5	2.3	ms
LOGIN ENABLE (ENB) INPUT						
ENB Threshold	$V_{ENB(H)}$	V_{ENB} rising	–	–	2	V
	$V_{ENB(L)}$	V_{ENB} falling	0.8	–	–	V
ENB Resistance	R_{ENB}		–	100	–	kΩ
ENB Filter/Deglitch Time	$t_{d(EN,FILT)}$		10	15	25	µs
OVERCURRENT PROTECTION (OCP)						
Current Limit[1]	I_{LIM}	V_{OUT} = 5 V	−55	−80	−140	mA
Foldback Current[1]	I_{FBK}	V_{OUT} = 0 V	−13	−23	−35	mA
THERMAL PROTECTION (TSD)						
Thermal Shutdown Threshold[2]	T_{TSD}	T_J rising	165	–	–	°C
Thermal Shutdown Hysteresis[2]	T_{HYS}		–	15	–	°C
VOUT OV/UV PROTECTIONS						
VOUT OV Thresholds	$V_{OV(H)}$	V_{OUT} rising	5.15	5.33	5.5	V
	$V_{OV(L)}$	V_{OUT} falling	–	5.3	–	V
VOUT OV Hysteresis	$V_{OV(HYS)}$	$V_{OV(H)} – V_{OV(L)}$	15	30	50	mV
VOUT UV Thresholds	$V_{UV(H)}$	V_{OUT} rising	–	4.71	–	V
	$V_{UV(L)}$	V_{OUT} falling	4.5	4.68	4.85	V
VOUT UV Hysteresis	$V_{UV(HYS)}$	$V_{UV(H)} – V_{UV(L)}$	15	30	50	mV
VOUT Output Disconnect Threshold	V_{DISC}	V_{OUT} rising	–	7.2	–	V
POK OUTPUTS						
POK Output Low Voltage	$V_{POK(L)}$	ENB high, V_{IN} ≥ 5.25 V, I_{POK} = 4 mA	–	150	400	mV
POK Leakage Current[1]	$I_{POK(LKG)}$	V_{POK} = 3.3 V	–	–	2	µA
OV and UV Filter/Deglitch Times[2]	$t_{d(FILT)}$	Applies to undervoltage of the VOUT voltages	10	15	20	µs

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.

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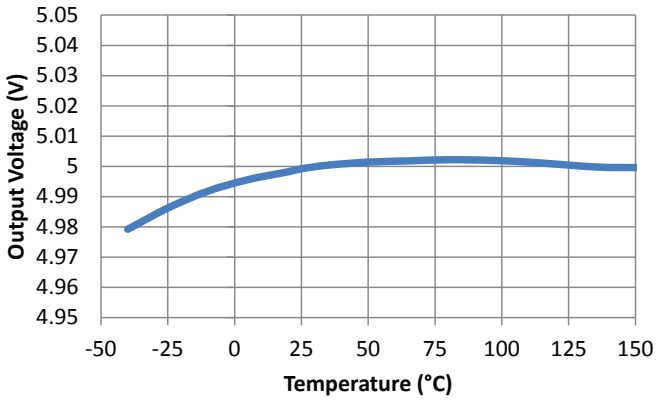
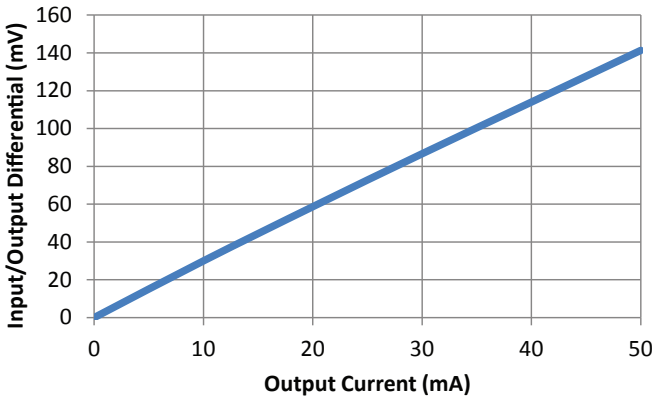
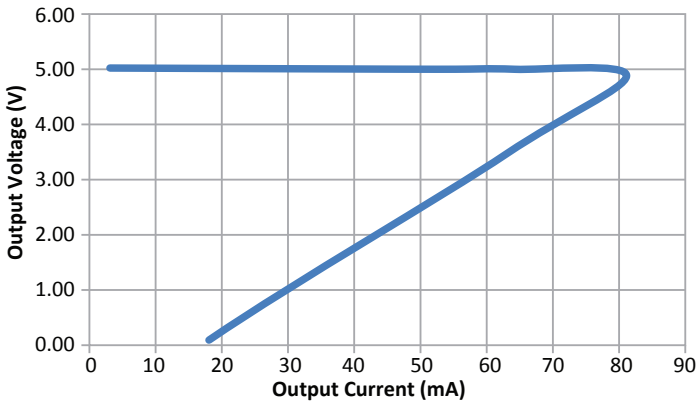
TYPICAL PERFORMANCE CHARACTERISTICS



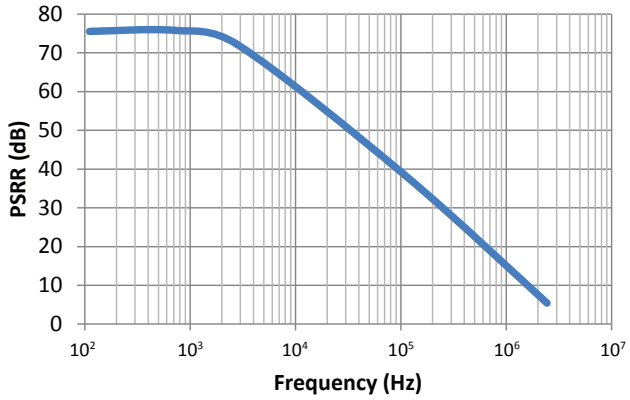
Output Voltage vs. Temperature



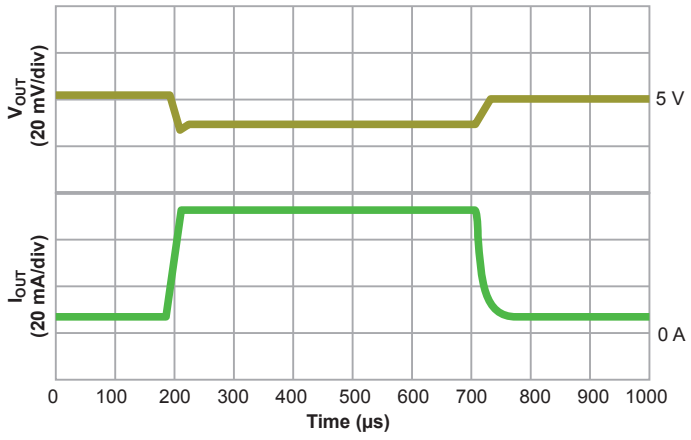
Dropout Voltage vs. Output Current



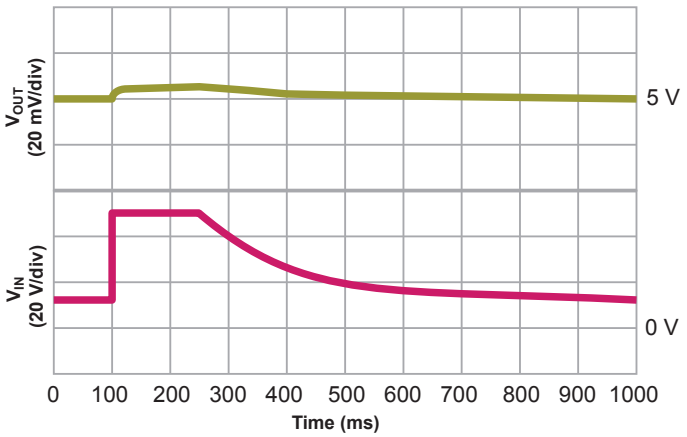
Foldback Current Limit



Ripple Rejection



Load Transient Response
(V_{IN} = 12 V, I_{OUT} = 5 mA to 50 mA, C_{OUT} = 4.7 µF)



Load Dump Characteristics
(V_{IN} = 12 to 50 V, I_{OUT} = 50 mA, C_{OUT} = 4.7 µF)

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FUNCTIONAL DESCRIPTION

Enable (ENB) Input

The A4481 has an enable (ENB) logic level input pin. To get the A4481 to operate, the ENB pin must be a logic high (>2 V). The ENB pin is rated to 50 V, allowing the ENB pin to be connected directly to VIN if there is no suitable logic signal available to wake up the A4481. When ENB transitions low, the A4481 waits approximately 15 µs before shutting down. This delay provides plenty of filtering to prevent the A4481 from prematurely shutting down because of any small glitch coupling onto the PCB trace or ENB pin.

Power OK (POK) Output

The Power OK (POK) output is an open-drain output, so an external pull-up resistor must be connected. An internal comparator monitors the voltage at the VOUT pin and controls the open-drain device at the POK pin. POK is high when the voltage at the VOUT pin is within 10% of the final regulation voltage. The POK output is pulled low if: (1) the ENB pin transitions low, (2) UVLO occurs, (3) TSD occurs, or (4) UV/OVP occurs.

The following timing diagram shows the basic operation and fault handling of the A4481:

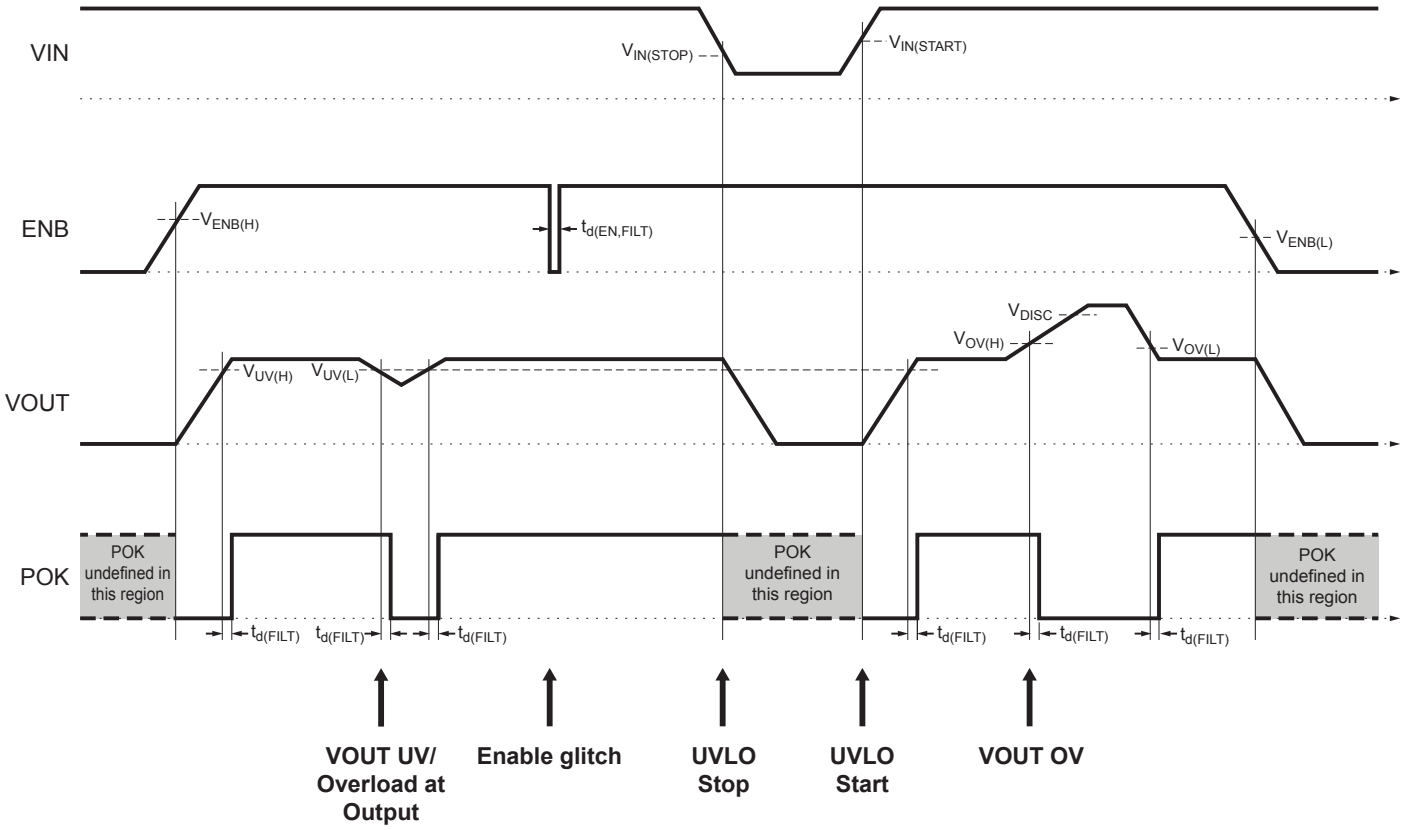

Figure 1: Timing Diagram (not to scale)

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APPLICATION INFORMATION

Capacitor Selection

Output Capacitor (C_{OUT}): The A4481 is designed to be stable with all types of output capacitors, but it must meet the minimum and maximum capacitance requirement of 3 µF and 10 µF at the intended operating temperature and working voltage. For a ceramic capacitor, X5R or X7R dielectrics with 10 V or higher voltage rating are recommended. However, if the part needs to survive short-to-battery events (e.g. to supply off-board sensors), then 50 to 100 V voltage-rated capacitors are recommended.

Input Capacitor (C_{IN}): A 2.2 µF or larger capacitor is recommended for an input bypass capacitor. Similarly, choose a capacitor that offers plenty of safety margins for known input voltage applications.

Thermal Considerations

The A4481 remains fully operational to 40 V. However, owing to power dissipation characteristics of the package, full output current cannot be ensured for all combinations of ambient temperature and input voltage. The maximum allowable power dissipation in the IC is as follows:

$$P_{MAX} = \frac{(T_{J(MAX)} - T_A)}{R_{\theta JA}}$$

where $T_{J(MAX)}$ = maximum junction temperature, T_A = ambient air temperature, and $R_{\theta JA}$ thermal = resistance from junction to ambient. (35°C/W for the 8-pin eSOIC).

The power dissipated by the IC can be calculated according to the following equation:

$$P_{DISS} = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

where V_{IN} = input voltage, V_{OUT} = output voltage, I_{OUT} = output current, and I_Q = input quiescent current (3.4 mA typical).

Figure 2 shows current de-rating plot at selected input voltages based on the above calculations.

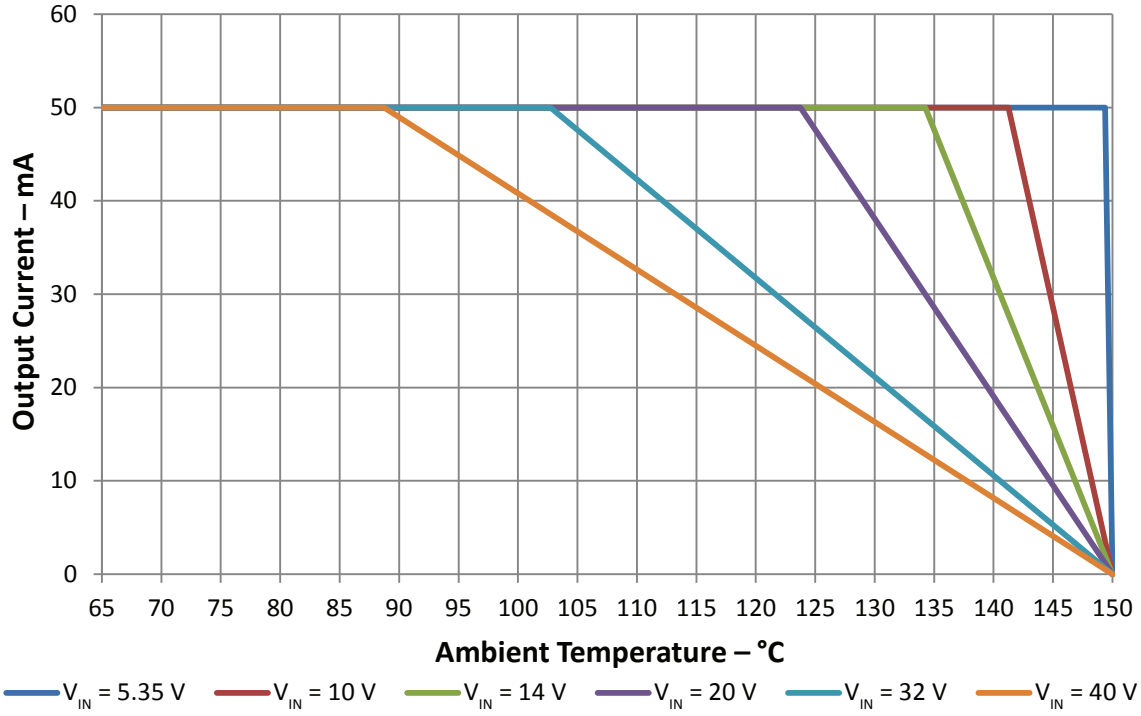

Figure 2: Output Current De-Rating vs. Input Voltage

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PCB LAYOUT GUIDELINES

Place the input and output capacitors as close as possible and on the same side of the PCB and IC.

Place thermal vias directly under the device in a tight pattern, as shown in Figure 4, to improve dissipation.

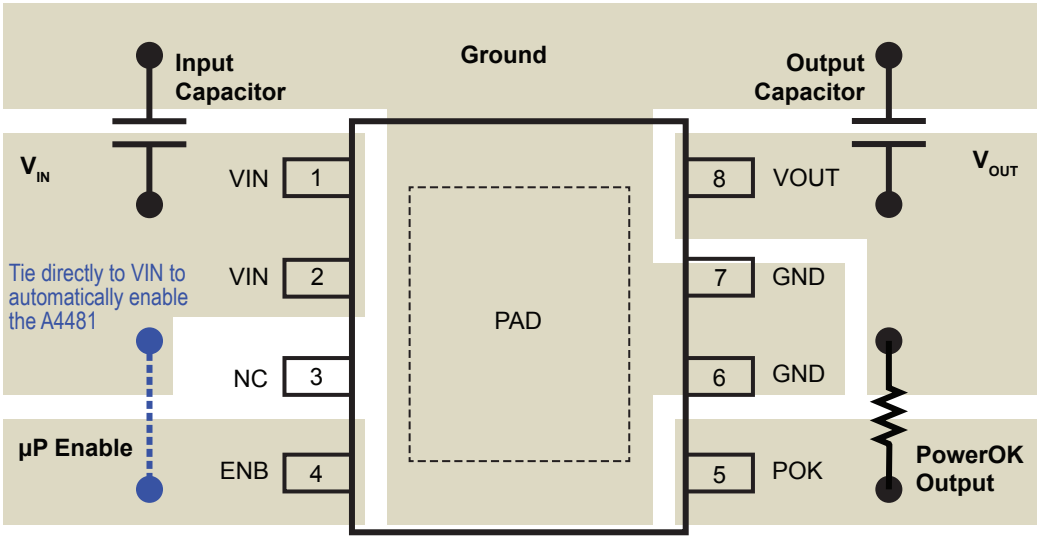

Figure 3: A4481 Layout Example

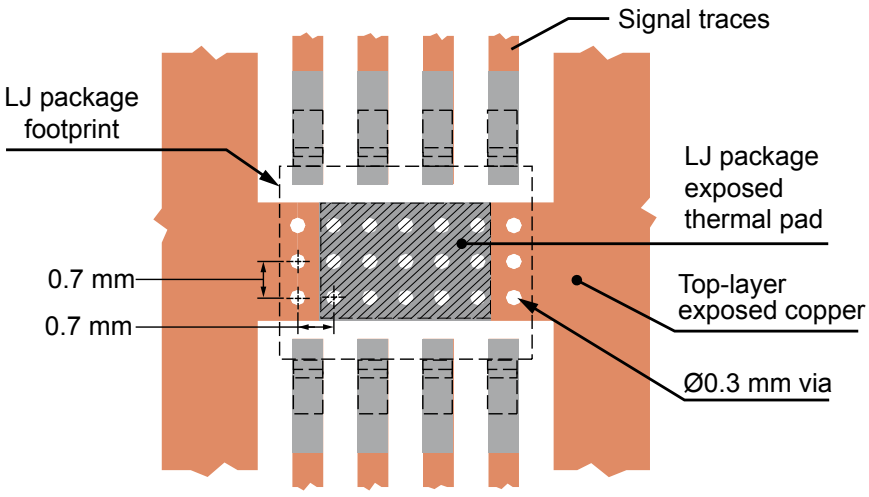

Figure 4: Suggested PCB layout for thermal optimization (maximum available bottom-layer copper recommended)

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000380, Rev. 2 and JEDEC MS-012BA)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

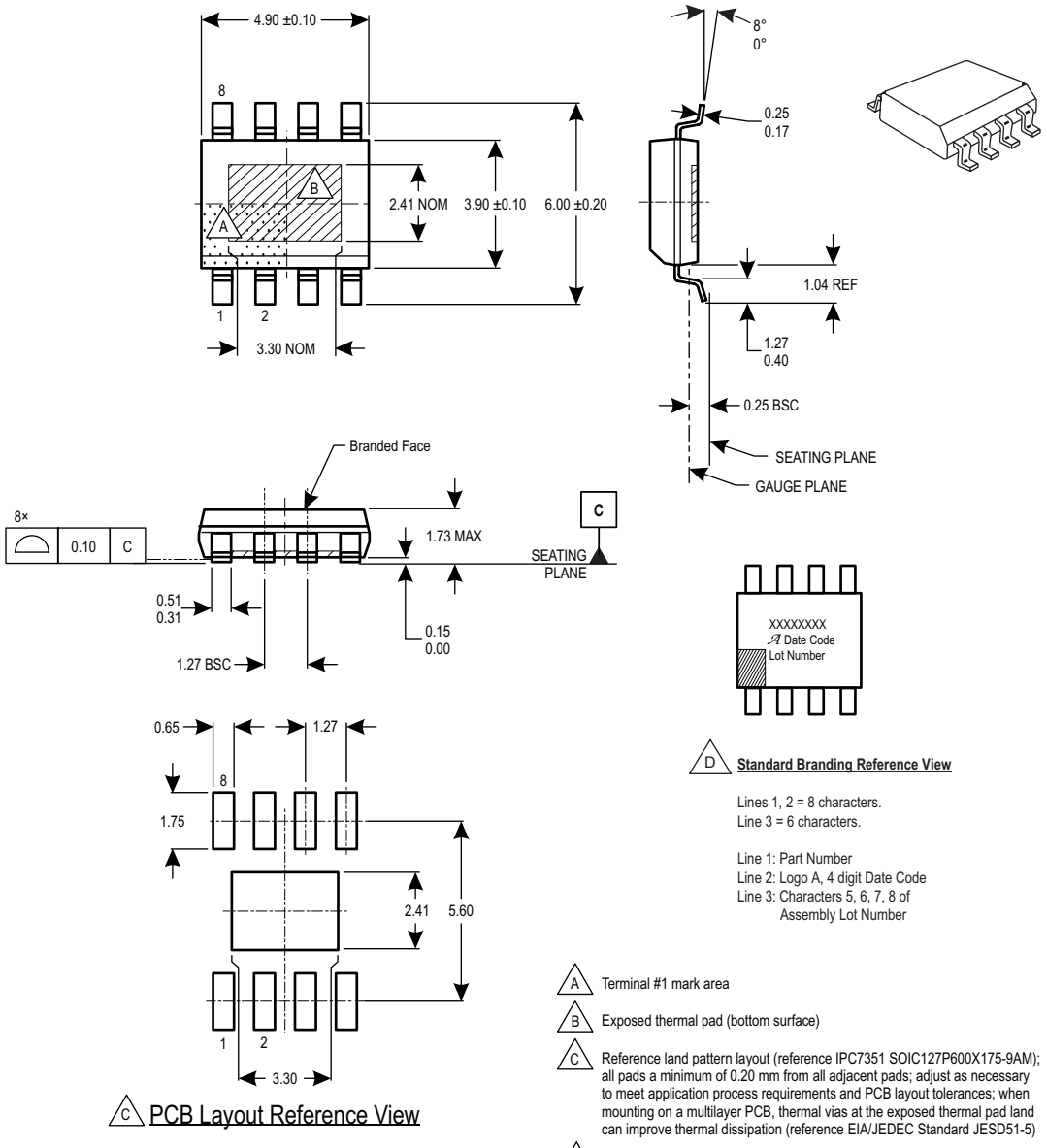

Figure 5: Package LJ, 8-Pin eSOIC

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Revision History

Number	Date	Description
–	October 9, 2015	Initial Release
1	August 31, 2016	Updated Foldback Current values (page 4) and Power OK (POK) Output section (page 6).
2	December 20, 2019	Minor editorial updates
3	January 6, 2022	Updated package drawing (page 9)

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