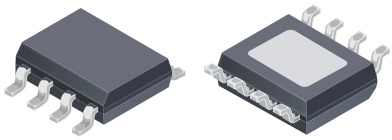
A4945 and A4949

Three Phase Sensorless Sinusoidal Fan Driver

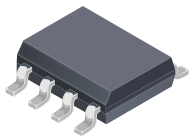
FEATURES AND BENEFITS

- 180° sinusoidal drive for low audible noise
- High efficiency control algorithm
- Sensorless operation
- Analog Speed input (A4945)
- PWM Speed input (A4949)
- Wide supply voltage range
- FG speed output
- Lock detection
- Overcurrent protection
- Soft start
- Short circuit protection

PACKAGES:



8-pin SOICN
with exposed thermal pad
(LJ package)



8-pin SOICN
(L package)

Not to scale

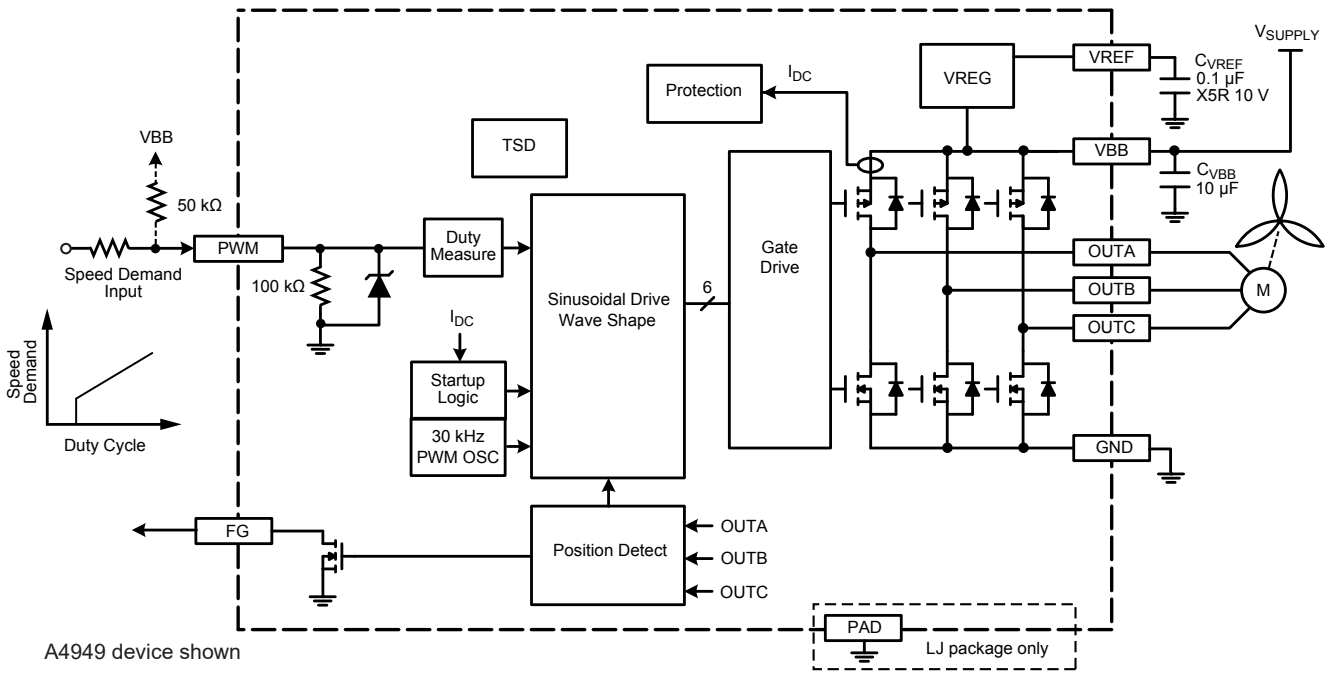
DESCRIPTION

The A4945 and A4949 three phase motor drivers incorporate sinusoidal drive to minimize audible noise and vibration for medium power fans.

A Speed input is provided to control motor speed. This allows system cost savings by eliminating an external variable power supply. Alternatively, power supply modulation down to 4 V can be used to adjust motor speed.

The A4945 and A4949 are supplied in an 8-pin SOICN with exposed power pad (suffix LJ), and an 8-pin SOICN (suffix L) for wave solder applications. Both packages are lead (Pb) free with 100% matte-tin leadframe plating.

Functional Block Diagram



SELECTION GUIDE

Part Number	Speed Input	Operating Ambient Temperature Range T_A, (°C)	Package		Packing
A4945GLJTR-T [1][5]	Analog	–40 to 105	8-pin SOICN	Exposed thermal pad	3000 pieces per 13-in. reel
A4945GLTR-T [1][5]			8-pin SOICN	–	
~~A4945KLJTR-T~~ [1][2]		–40 to 125	8-pin SOICN	Exposed thermal pad	
A4949GLJTR-T [1]	PWM	–40 to 105	8-pin SOICN	Exposed thermal pad	
A4949GLJTR-6-T [3][4]					
A4949GLTR-T [1]			8-pin SOICN	–	
~~A4949KLJTR-T~~ [1][2]		–40 to 125	8-pin SOICN	Exposed thermal pad	
~~A4949KLJTR-6-T~~ [2][3][4]					

[1] Startup Current Ramp: Slow ramp – device takes a 50 mA current step every 128 ms. BEMF Hysteresis at Startup: 100 mV. See Figure 4.
[2] The A4945KLJTR-T, A4949KLJTR-T, and A4949KLJTR-6-T part variants have been discontinued. Samples are no longer available.
Date of status change: December 28, 2019. For existing customer transition, and for new customers or new applications, refer to A5947KLPTR-T.
[3] Contact Allegro sales for availability of this package option.
[4] Startup Current Ramp: Fast ramp – device takes a 50 mA current step every 31 ms. BEMF Hysteresis at Startup: 40 mV. See Figure 4.
[5] Part variants A4945GLTR-T and A4945GLJTR-T are no longer in production. This device should not be purchased for new design applications. Samples are no longer available. Status change date: September 30, 2024.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		18	V
Input Logic Voltage Range	V_{IN}	PWM and VSP pins	–0.3 to 6	V
Logic Output	V_{FG}	FG pin	14	V
Logic Output Current	I_{FG}	FG pin	10	mA
Load Output Current	I_{OUT}	Internally limited	I_{OCL}(max)	A
Operating Ambient Temperature	T_A	G temperature range	–40 to 105	°C
		K temperature range	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	L package, single-sided PCB with copper limited to mounting lands	140	°C/W
		LJ package, 2-sided PCB with 0.8 in^2 copper each side	62	°C/W

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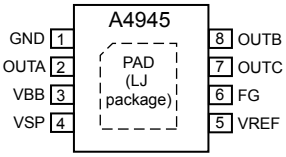
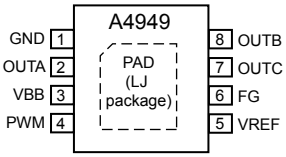
Pinout Diagrams

L and LJ packages





Terminal List Table

Number	Name	Function
1	GND	Ground
2	OUTA	Motor terminal
3	VBB	Input supply
4	VSP	Speed (analog) logic input (A4945)
	PWM	Speed (PWM) logic input (A4949)
5	VREF	Analog output
6	FG	Speed output signal
7	OUTC	Motor terminal
8	OUTB	Motor terminal
–	PAD	Exposed thermal pad (LJ package)

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ELECTRICAL CHARACTERISTICS: Unless otherwise specified,
G version*: Valid at T_A = 25°C, V_{BB} = 4 to 18 V
K version*: Valid at T_A = –40°C to 125°C, V_{BB} = 4 to 18 V

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
VBB Supply Current	I_{BB}	V_{IN} = 3 V	–	10	15	mA
Total Driver $R_{DS(on)}$ (Sink + Source)	$R_{DS(on)}$	I_{OUT} = 1 A, T_J = 25°C, V_{BB} = 12 V	–	1.1	1.4	Ω
		I_{OUT} = 1 A, T_J = 25°C, V_{BB} = 4 V	–	1.5	1.8	Ω
Reference Voltage (VREF pin)	V_{REF}	I_{FG} = 5 mA	3.2	3.3	3.4	V
Output Saturation Voltage (FG Pin)	$V_{FG(sat)}$	I_{FG} = 5 mA	–	–	0.3	V
FG Output Leakage	$I_{FG(LKG)}$	V_{FG} = 14 V	–	–	1	µA
Motor PWM Frequency	f_{OUTPWM}		28	30	32	kHz
INPUT LOGIC (A4945 VSP Pin or A4949 PWM Pin)						
Input Current	I_{IN}	V_{IN} = 3 V (R_{IN} = 100 kΩ pulldown)	21	33	45	µA
Logic Input (Low Level)	V_{IL}		0	–	0.8	V
Logic Input (High Level)	V_{IH}		2	–	5.5	V
Logic Input Hysteresis	V_{IHYS}		200	300	600	mV
Input Pulldown Resistance	R_{IN}		–	100	–	kΩ
A4945 SPEED INPUT (VSP Pin)						
VSP On-Threshold Level	V_{ON}		0.45	0.9	1.2	V
VSP On-Time	t_{ON}	C_{VREF} = 1 µF	100	–	–	µs
VSP Disable Threshold	V_{THOFF}		194	228	264	mV
VSP Accuracy	ERR_{VSP}		–	±6	–	LSB
VSP Maximum Level	$V_{SP(MAX)}$		2.95	3	3.05	V
A4949 SPEED INPUT (PWM Pin)						
PWM On Threshold	D_{ON}		9.5	10	10.5	%
PWM Off Threshold	D_{OFF}		7	7.5	8	%
PWM Input Frequency Range	f_{PWM}		0.1	–	100	kHz
PROTECTION						
VBB Undervoltage Lockout (UVLO)	V_{BBUVLO}	V_{BB} rising	–	3.85	3.98	V
VBB UVLO Hysteresis	$V_{BBUVHYS}$		150	300	450	mV
Lock Protection	t_{OFF}		7	8	9	s
Overcurrent Limiting (OCL)	I_{OCL}		1.4	1.6	1.8	A
Thermal Shutdown Temperature (TSD)	T_{JTSD}	Temperature rising	150	165	180	°C
Thermal Shutdown Hysteresis	$T_{JTSDHYS}$	Recovery = T_{JTSD} – $T_{JTSDHYS}$	–	20	–	°C

*Specified limits are tested at a single temperature and assured across the operating temperature range by design and characterization.

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FUNCTIONAL DESCRIPTION

The A4945/A4949 targets fan applications, meeting application design objectives of low audible noise, minimal vibration, and high efficiency. The Allegro proprietary control algorithm results in a sinusoidal current waveform that adapts to a variety of motor characteristics, in order to dynamically optimize efficiency across a wide range of speeds. The A4945/A4949 trapezoidal startup method does not require any external components and automatically switches to sinusoidal operation as the motor is accelerating up to operating speed.

Speed Control

The speed of the fan can be controlled by: voltage mode (control of power supply amplitude), variable duty cycle PWM input (A4949 only), or via an adjustable analog input (A4945 only). Use of the PWM or analog input allows overall system cost savings by eliminating the requirement for an external variable power supply. Voltage mode operation allows the IC to fit into legacy systems, achieving operation down to 4 V.

The Speed input, analog voltage for the A4945 or PWM duty cycle for the A4949, is measured and converted to a 9-bit number. This 9-bit speed demand value is applied to an internal PWM generator function to create the modulation profile. The modulation profile is applied to the three motor outputs, with a 120-degree phase relationship, to create the sinusoidal current waveform as shown in Figure 1.

A BEMF detection window is opened on the phase A modulation profile in order to measure the rotor position, so as to define the modulation timing. The control system maintains the window at a small level in order to minimize the disturbance and to approximate the ideal sinusoidal current waveform as much as possible.

A4945 – VSP Pin Analog Input. An internal A-to-D convertor translates the input voltage to a demand value to control speed of the fan (Figure 2). The motor drive will be disabled if the VSP pin voltage is lower than V_{THOFF}. Upon startup, V_{IN} must exceed V_{THON} for t_{ON}. The t_{ON} delay is required to allow internal reference supply and analog circuits to properly power-up. After this short delay, V_{SP} can be adjusted below V_{THOFF} to allow full scale operation (7.5% to 100%).

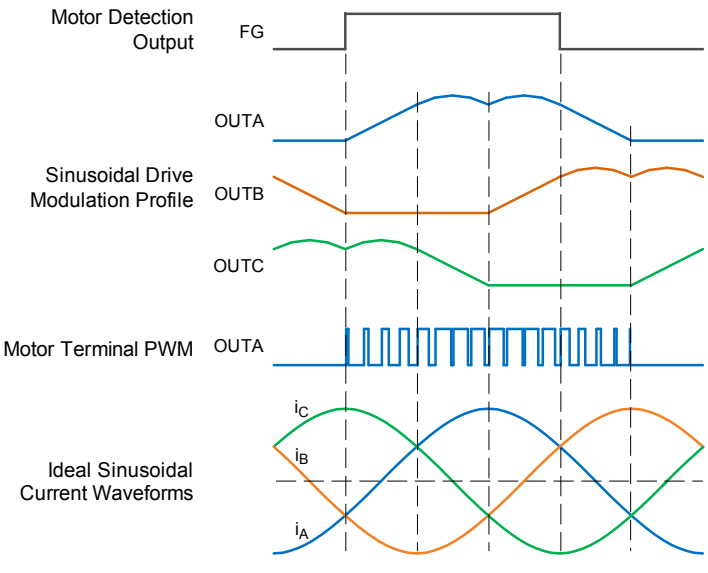

Figure 1: Sinusoidal PWM Output Generation

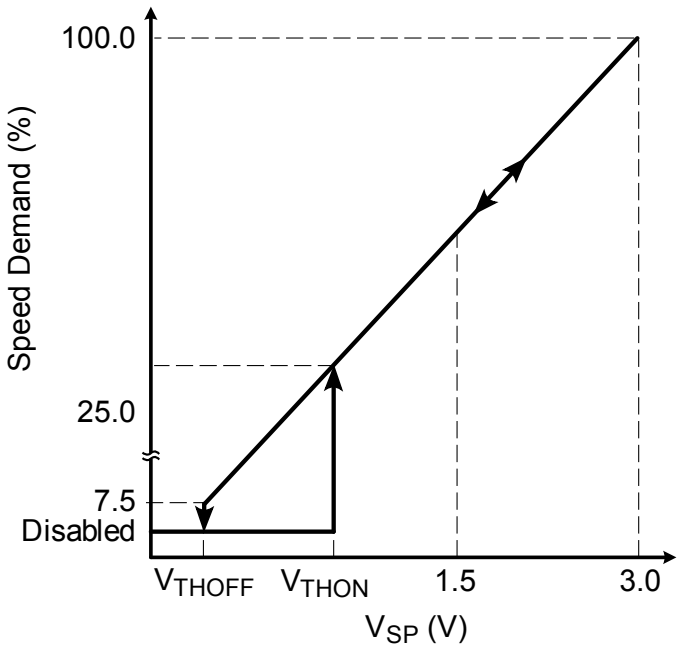

Figure 2: A4945 Analog Speed Input Characteristic

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A4949 – PWM Pin Duty Cycle Input. A duty cycle measurement circuit converts the applied duty cycle to a demand value (9-bit resolution) to control speed of the fan. The motor drive will be enabled if the duty cycle is greater than D_{ON} (10% (typ)) (Figure 3). The PWM input is filtered to prevent spurious noise from turning the IC on or off unexpectedly.

There is an internal pulldown resistor (100 kΩ) on the PWM pin that turns the motor off if the input signal is disconnected. If 100% speed demand is required, such as for an open PWM condition, connect a 50 kΩ pullup resistor to the VBB pin.

Power Supply Modulation. Speed can be controlled simply by varying the power supply voltage. To allow this function, insert a 50 kΩ pullup resistor from the VSP pin (A4945) or the PWM pin (A4949) to the VBB pin. Motor driving will be enabled and disabled at the VBB undervoltage lockout rising and falling thresholds.

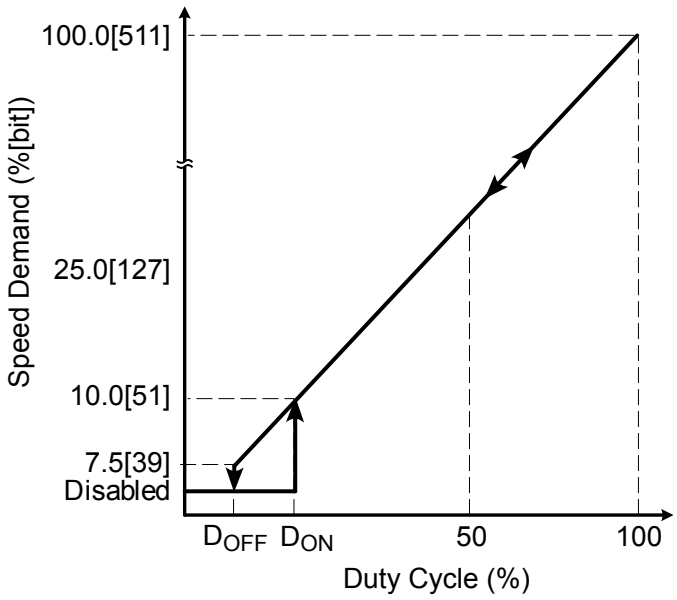

Figure 3: A4949 PWM Speed Input Characteristic

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Soft Start

A soft start feature is integrated, both to minimize demand on the power supply at startup, and to smoothly initiate motor rotation and ramp up to speed. Soft start ramps both the speed demand (duty cycle) and current limit as shown in Figure 4.

Protection

Protection features include: lock detection with restart, overcurrent limit, motor output short circuit detection, supply undervoltage monitor, and thermal shutdown.

Lock Detect Speed is monitored to determine if the rotor is locked. If a lock condition is detected, the IC will be disabled for t_{OFF} before an auto-restart is attempted.

FG Open drain output provides speed information to the system. FG changes state one period per electrical revolution of the motor (as shown in Figure 1).

Current Limit Load current is monitored on the high-side MOSFET. If the current has reached I_{OCL}, the source drivers will turn off for the remaining time of the PWM cycle.

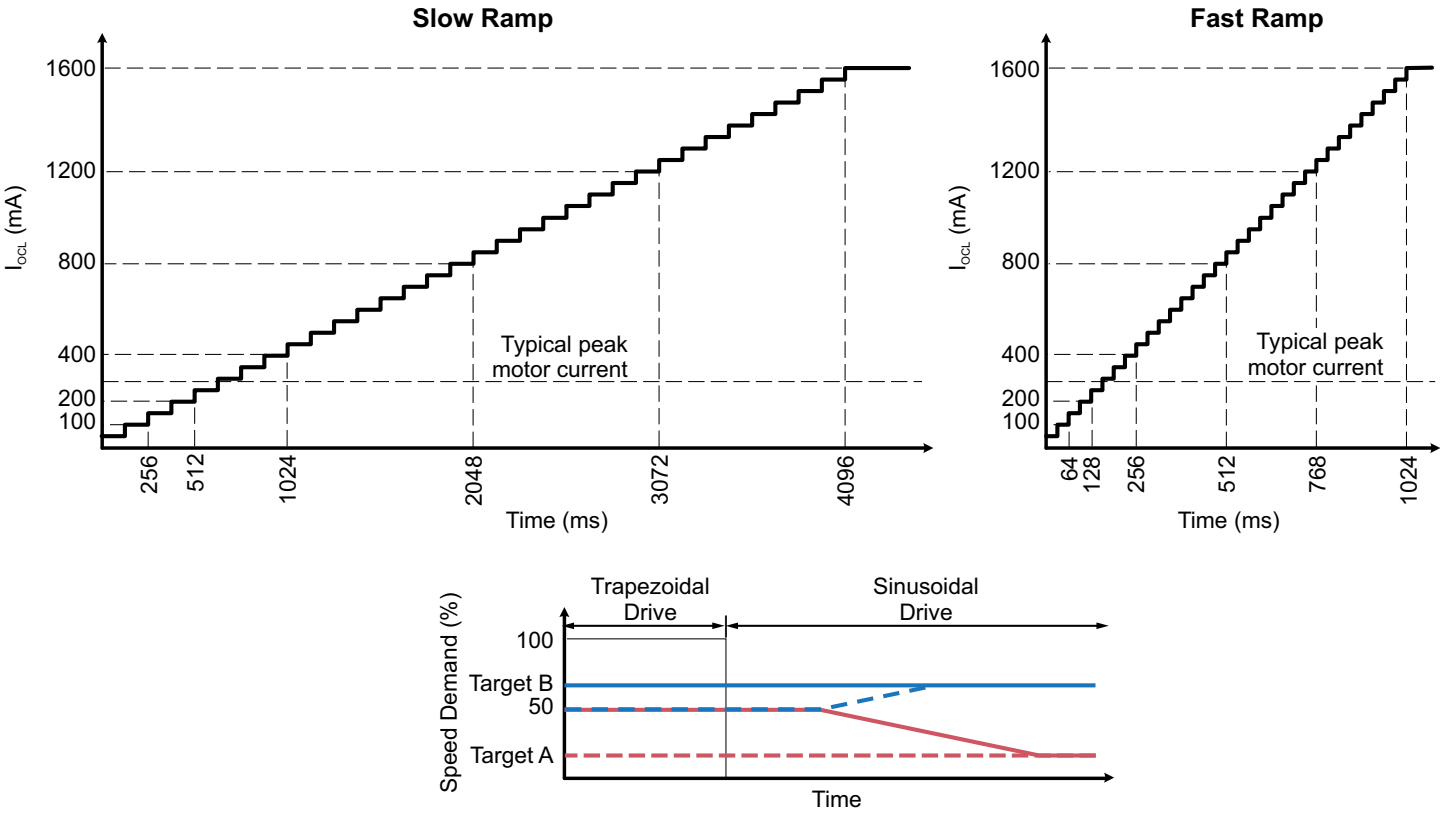

Figure 4: A4945 and A4949 Startup

1. Target A represents situation where the external duty cycle applied is less than 50% at startup. A minimum level of 50% demand is applied internally to ensure the motor will accelerate in reasonable time. 500 ms after the IC has switched from trapezoidal mode to sinusoidal mode, demand ramps down at a rate of 410 ms for every 10% demand.
2. Target B represents the external duty cycle applied at greater than 50% at startup. In this case, the internally applied duty cycle stays constant.
3. Drive mode switches from trapezoidal mode to sinusoidal mode after the motor approaches startup target speed (50% or greater). The time required to switch-over depends on motor characteristics and the demand applied at startup.

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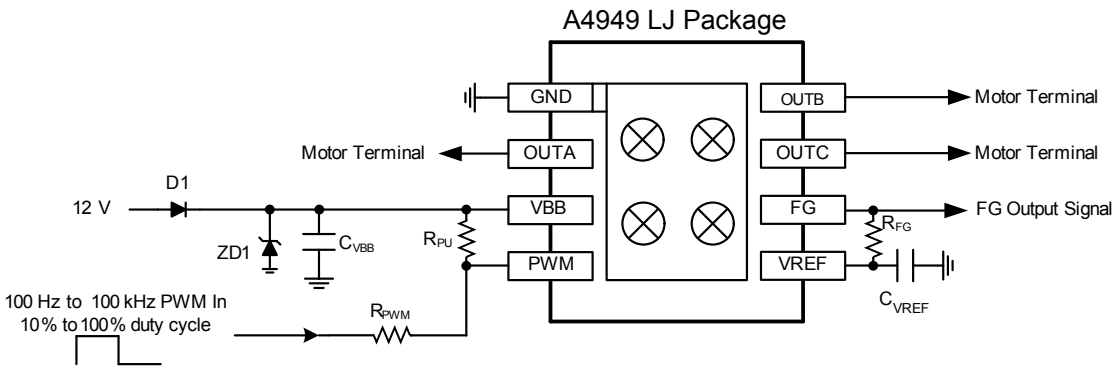
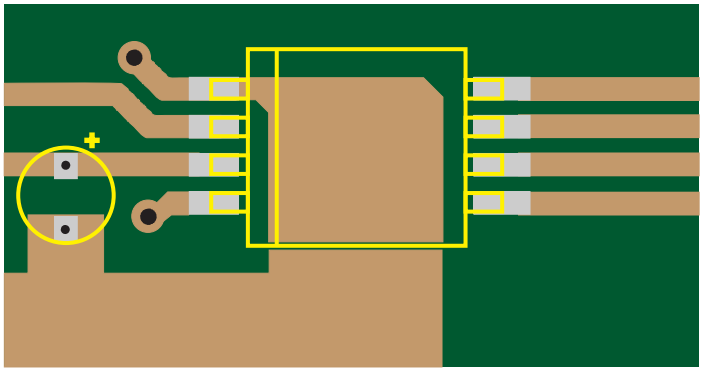
APPLICATION INFORMATION



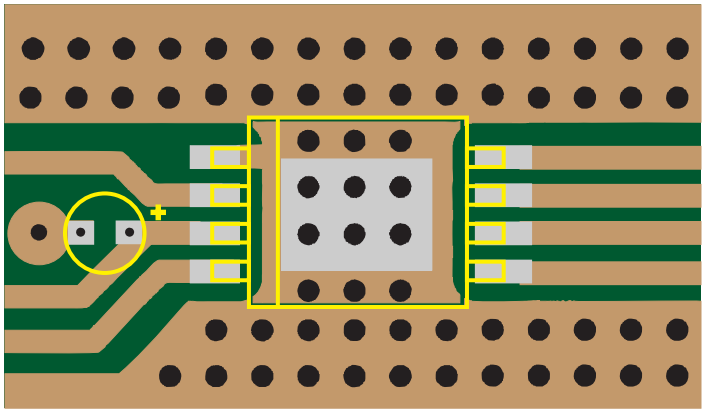
Typical Application Circuit

Name	Suggested Value	Comment
C_{VREF}	0.1 µF/X5R/10 V	Required – ceramic capacitor
C_{VBB}	4.7 to 47 µF	Power supply stabilization; electrolytic or ceramic can be used
R_{FG}	20 kΩ	Optional – Pullup resistor for speed feedback
D1	Not installed	May be required to isolate motor from system or for reverse polarity protection
ZD1	Not Installed	Optional – TVS to limit maximum V_{BB} due to transients resulting from motor generation or power line. Suggested to clamp below 18 V (example: Fairchild SMBJ14A). Typically required if blocking diode D1 is used.
R_{PWM}	1 kΩ	Optional – If the PWM or VSP pin is wired to a connector, R_{PWM} will isolate the IC pin from noise or overvoltage transients.
R_{PU}	50 kΩ	Optional – If the application requires maximum speed when a PWM pin open circuit occurs, then this pullup resistor to VBB is required. Do not pullup to V_{REF}.

Layout Notes:
1. Add thermal vias to exposed pad area. Connect to ground planes on top and bottom of PCB.
2. Place C_{VREF} and C_{VBB} as close as possible to the IC.



L Package Board



LJ Package Board Via Layout for Thermal Dissipation

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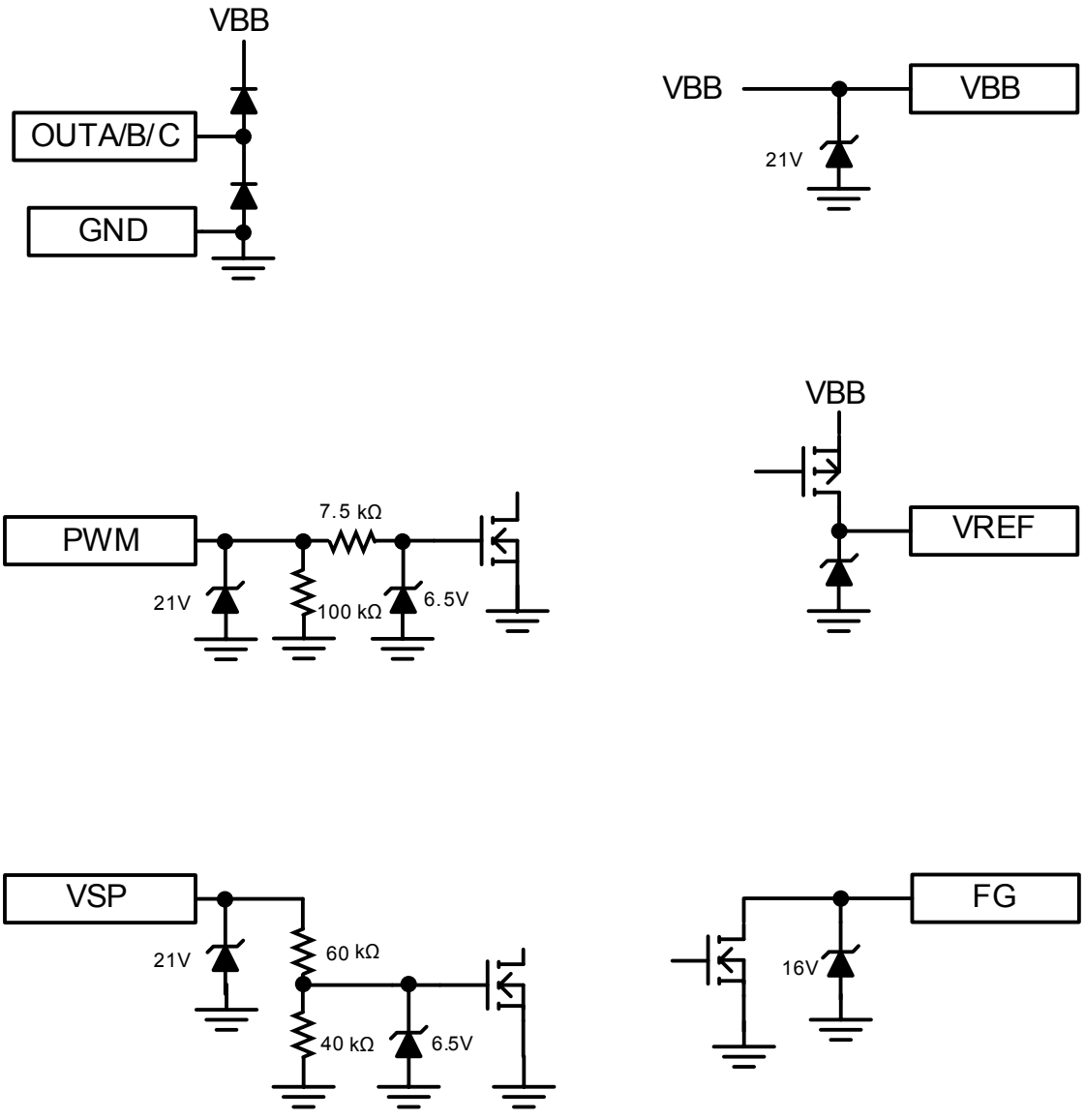
INPUT/OUTPUT PIN STRUCTURES



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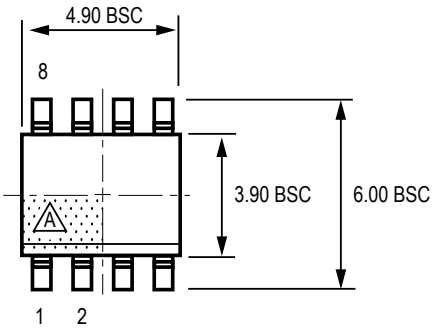
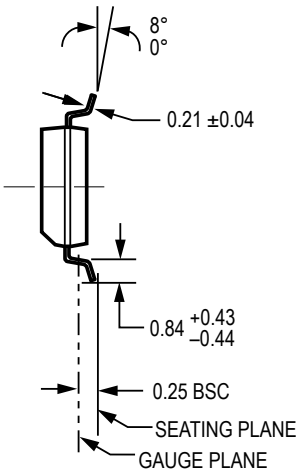
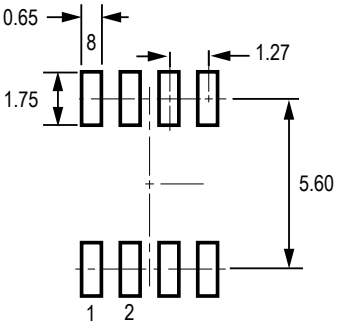
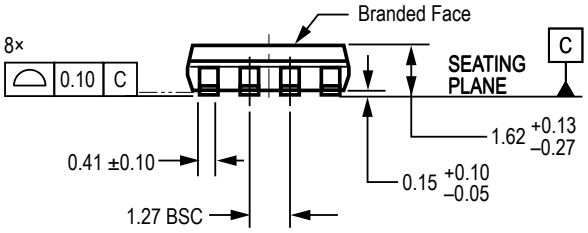
Package L, 8-Pin SOICN







B PCB Layout Reference View

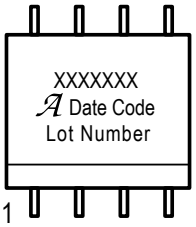


For Reference Only; not for tooling use
(reference Allegro DWG-0000385, Rev. 2 or JEDEC MS-012AA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area.

B Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances.

C Branding scale and appearance at supplier discretion.



C Standard Branding Reference View

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot number

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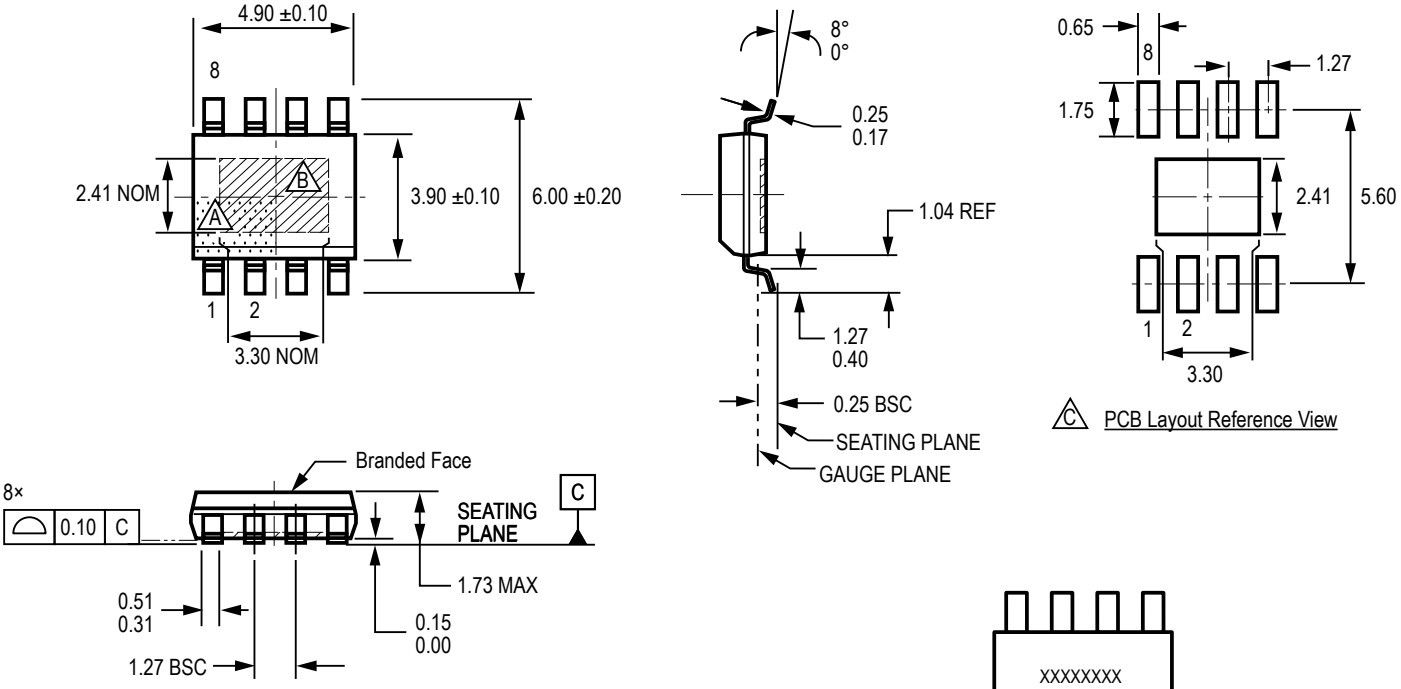
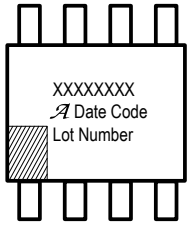
Package LJ, 8-Pin SOICN with Exposed Thermal Pad





For Reference Only; not for tooling use
(reference Allegro DWG-0000380, Rev. 2 and JEDEC MS-012BA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area.

B Exposed thermal pad (bottom surface).

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-9AM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

D Branding scale and appearance at supplier discretion.

D **Standard Branding Reference View**

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

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Revision History

Number	Date	Description
1	May 6, 2014	Added -6 variant
2	January 30, 2015	Added KLJ-6-T variant
3	July 25, 2018	Minor editorial updates
4	February 1, 2019	Updated K temperature variant product status to Pre-End-of-Life
5	August 1, 2019	Updated K temperature variant product status to Last Time Buy
6	September 29, 2020	Updated K temperature variant product status to Discontinued
7	October 9, 2022	Updated package drawings (pages 10-11)
8	March 19, 2024	Part variants A4945GLJTR-T and A4945GLTR-T status changed to Last-Time Buy (page 2).
9	September 13, 2024	Part variants A4945GLJTR-T and A4945GLTR-T status changed to Discontinued (page 2).

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