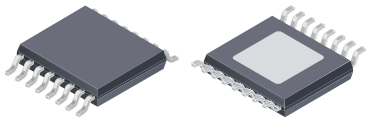
A8583

Wide Input Voltage, 2.4 MHz, 3.5 A Asynchronous Buck Regulator

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Wide operating voltage range: 4.7 to 36 V
- UVLO stop threshold is at 3.8 V (typ)
- Supports 40 V input for surge and load dump testing
- Capable of at least 3.5 A steady-state output current
- Adjustable output voltage as low as 0.8 V
- Internal 70 mΩ high-side switching MOSFET
- Adjustable switching frequency, f_{SW}: 0.25 to 2.4 MHz
- Synchronization to external clock: $1.2 \times f_{SW}$ to $1.5 \times f_{SW}$
- Sleep mode supply current less than 3 µA
- Soft start time externally set via the SS pin
- Very low no-load current, typically 3.5 mA
- Pre-bias startup compatible
- Power OK (POK) output
- Pulse-by-pulse current limiting (OCP)
- Hiccup mode short-circuit protection (HIC)
- Overtemperature protection (TSD)
- Overvoltage protection (OVP)
- Missing asynchronous diode (D1) protection
- Open-circuit and adjacent pin short-circuit tolerant
- Short-to-ground tolerant at every pin
- Externally adjustable compensation
- Stable with ceramic output capacitors

PACKAGE: 16-pin TSSOP (suffix LP)



Not to scale

DESCRIPTION

The A8583 is an adjustable frequency, high output current, PWM regulator that integrates a low resistance, high-side, N-channel MOSFET. The A8583 incorporates current-mode control to provide simple compensation, excellent loop stability, and fast transient response. The A8583 utilizes external compensation to accommodate a wide range of power components to optimize transient response without sacrificing stability.

The A8583 regulates input voltages from 4.7 to 36 V, down to output voltages as low as 0.8 V and is able to supply at least 3.5 A of load current. The A8583 features include an externally adjustable switching frequency, an externally set soft start time to minimize inrush currents, an EN/SYNC input to either enable VOUT and/or synchronize the PWM switching frequency, and a Power OK (POK) output to indicate when VOUT is within regulation. The A8583 only turns-on the lower FET to charge the boot capacitor when needed, not every PWM cycle. This improves light load efficiency and provides no-load currents

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APPLICATIONS:

- GPS/infotainment
- Automobile audio
- Home audio
- Network and telecom

Typical Application

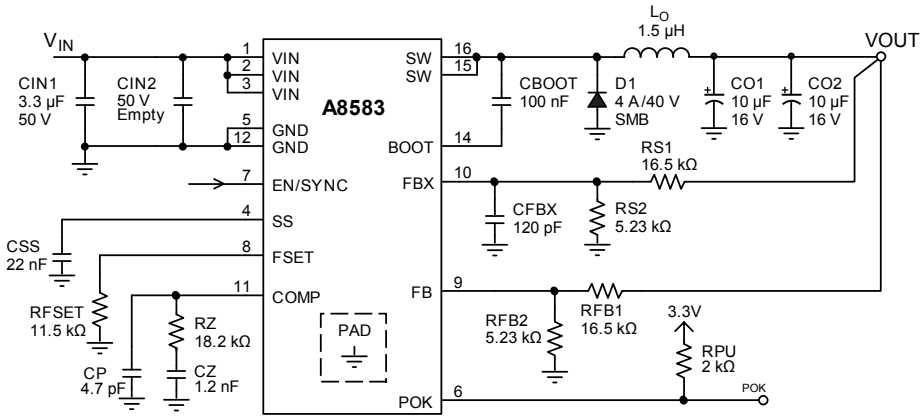

Figure 1. Application schematic, at V_{IN} 5 to 16 V, 3.3 V_{OUT} , at 2 MHz

DESCRIPTION (continued)

as low as 3.5 mA at 2 MHz. The Sleep mode current of the A8583 control circuitry is less than 3 µA.

Protection features include VIN undervoltage lockout (UVLO), pulse-by-pulse overcurrent protection (OCP), hiccup mode short-circuit protection (HIC), overvoltage protection (OVP), and thermal shutdown (TSD). In addition, the A8583 provides unique missing diode (D1) protection, open-circuit, adjacent pin short-circuit, and short-to-ground protection at every pin to satisfy the most demanding applications.

The A8583 device is available in a 16-pin TSSOP package with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte tin leadframe plating.

SELECTION GUIDE

Part Number	Packing
A8583KLPTR-T	4000 pieces per 13-in. reel

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
VIN Pin to GND	V_{IN}		–0.3 to 40	V
SW Pin to GND [2]	V_{SW}	Continuous	–0.3 to V_{IN} + 0.3	V
		Single pulse, t_W < 50 ns	–1.0 to V_{IN} + 5.0	V
BOOT Pin Above SW Pin	V_{BOOT}		V_{SW} – 0.3 to V_{SW} + 7.0	V
SS Pin	V_{SS}		–0.3 to V_{IN} + 0.3	V
All Other Pins	V_I		–0.3 to 5.5	V
Operating Ambient Temperature	T_A	K temperature range for automotive	–40 to 125	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum–rated conditions for extended periods may affect device reliability.

[2] SW has internal clamp diodes to GND and VIN. Applications that forward bias these diodes should take care not to exceed the IC package power dissipation limits.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	34	ºC/W

*Additional thermal information available on the Allegro website

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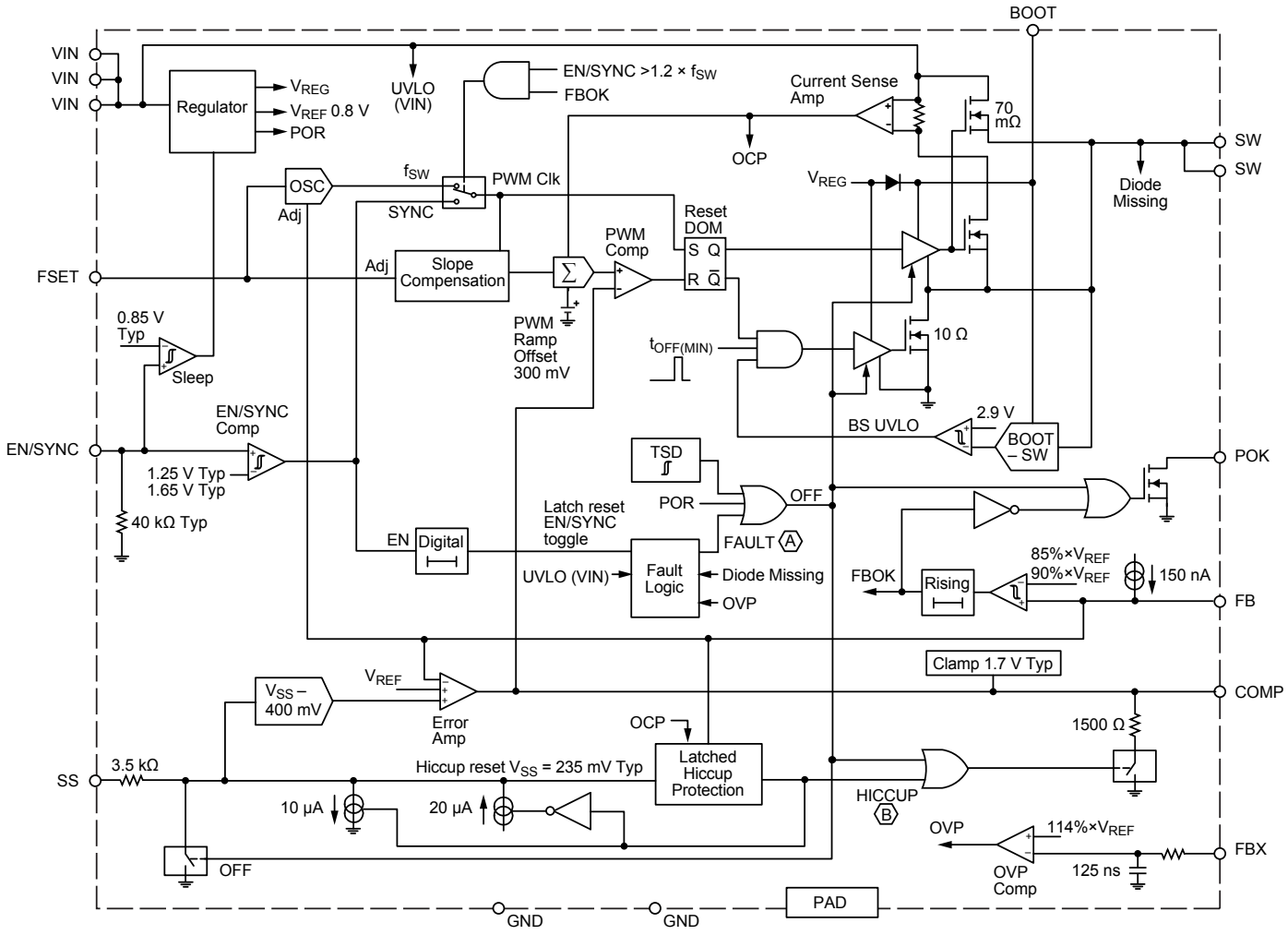
FUNCTIONAL BLOCK DIAGRAM



A FAULT = 1, if:
EN = 0, or
UVLO = 1, or
OVP = 1, or
Diode Missing = 1

B HICCUP = 1, if Hiccup protection enabled (V_{FB} < 625 mV) and a net count of > 7 OCP events occur

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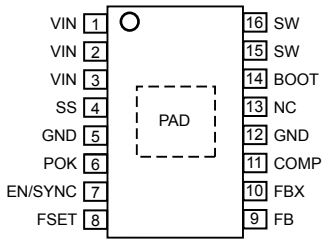
Pinout Diagram



Terminal List Table

Number	Name	Description
1, 2, 3	VIN	Power input for the control circuits and the drain of the internal high-side N-channel MOSFET. Connect this pin to a power supply of 4.7 to 36 V. A high quality ceramic capacitor should be placed very close to this pin.
4	SS	Soft-start pin. Connect a capacitor, CSS, from this pin to GND to set the soft-start time. This capacitor also determines the hiccup period during an overcurrent event.
5, 12	GND	Ground.
6	POK	Power OK output signal. This pin is an open drain output that transitions from low impedance to high impedance when the output is within the final regulation voltage.
7	EN/SYNC	Enable and synchronization input. This pin is a logic input that turns the converter on or off. Set this pin to logic high to turn the converter on or set this pin to logic low to turn the converter off. This pin also functions as a synchronization input to allow the PWM frequency to be set by an external clock.
8	FSET	Frequency setting pin. A resistor, RFSET, from this pin to GND sets the PWM switching frequency. See figure 10 and/or equation 2 to determine the value of RFSET.
9	FB	Feedback (negative) input to the Error amplifier. Connect a resistive divider from the converter output node, VOUT, to this pin to program the output voltage.
10	FBX	Remote sense input for the overvoltage protection (OVP) comparator. Connect a resistive divider from the converter output node, VOUT, to this pin to set the OVP trip threshold. If OVP protection is not required, this pin should be grounded.
11	COMP	Output of the error amplifier and compensation node for the current-mode control loop. Connect a series RC network from this pin to GND for loop compensation. See the Design and Component Selection section of this datasheet for further details.
13	NC	No connect.
14	BOOT	High-side gate drive boost input. This pin supplies the drive for the high-side N-channel MOSFET. Connect a 100 nF ceramic capacitor from BOOT to SW.
15, 16	SW	The source of the internal high-side N-channel MOSFET. The external free-wheeling diode (D1) and output inductor (L_O) should be connected to this pin. Both D1 and L_O should be placed close to this pin and connected with relatively wide traces.
–	PAD	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 6 vias, directly in the pad.

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ELECTRICAL CHARACTERISTICS [1]: Valid at V_{IN} = 12 V, T_A = 25°C , • indicates specifications guaranteed through –40°C ≤ T_J ≤ 125°C; unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ. [2]	Max.	Unit
INPUT VOLTAGE SPECIFICATIONS							
Operating Input Voltage Range	V_{IN}		•	4.7	–	36	V
UVLO Start Threshold	$V_{INSTART}$	V_{IN} rising		–	4.2	4.6	V
UVLO Stop Threshold	V_{INSTOP}	V_{IN} falling		–	3.8	4.2	V
UVLO Hysteresis	$V_{UVLOHYS}$			280	400	520	mV
INPUT CURRENTS							
Input Quiescent Current	I_Q	$V_{EN/SYNC}$ = 5 V, V_{FB} = 1.5 V, no PWM switching	•	–	3.0	5.0	mA
Input Sleep Supply Current [3]	I_{QSLEEP}	V_{IN} = 16 V, $V_{EN/SYNC}$ ≤ 0.4 V, T_A = T_J between –40°C and 85°C		–	–	3.0	µA
		V_{IN} = 16 V, $V_{EN/SYNC}$ ≤ 0.4 V, T_A = T_J = 125°C		–	5	15	µA
REFERENCE VOLTAGE							
Feedback Voltage	V_{FB}	4.7 V < V_{IN} < 36 V, V_{FB} = V_{COMP}	•	792	800	808	mV
ERROR AMPLIFIER							
Feedback Input Bias Current	I_{FB}	V_{COMP} = 1.5 V, V_{FB} regulated so that I_{COMP} = 0 A	•	–	–150	–300	nA
Open Loop Voltage Gain	A_{VOL}			–	56	–	dB
Transconductance	g_m	I_{COMP} = 0 µA, V_{SS} > 700 mV	•	550	750	1000	µA/V
		0 V < V_{SS} < 700 mV		–	225	–	µA/V
Source Current	$I_{EA(SRC)}$	V_{FB} < 0.8 V, V_{COMP} = 1.5 V		–	–50	–	µA
Sink Current	$I_{EA(SINK)}$	V_{FB} > 0.8 V, V_{COMP} = 1.5 V		–	+50	–	µA
Maximum Output Voltage	$V_{EAVO(max)}$			1.3	1.7	2.1	V
COMP Pull-Down Resistance	R_{COMP}	FAULT = 1		–	1500	–	Ω
PULSE WIDTH MODULATION (PWM)							
PWM Ramp Offset	$V_{PWMOFFSET}$	V_{COMP} for 0% duty cycle		–	300	–	mV
Minimum Controllable On-Time	$t_{ON(MIN)}$		•	–	65	100	ns
Minimum Switch Off-Time	$t_{OFF(MIN)}$		•	–	65	130	ns
COMP to SW Current Gain	g_{mPOWER}		•	–	5.0	–	A/V
Slope Compensation	S_E	f_{SW} = 250 kHz		–	0.33	–	A/µs
		f_{SW} = 2.0 MHz		–	2.6	–	A/µs
MOSFET PARAMETERS							
Hi-Side MOSFET On Resistance	$R_{DS(on)HS}$	I_{DS} = 400 mA, V_{BOOT} – V_{SW} = 6 V		–	70	–	mΩ
High-Side MOSFET Leakage Current [3]	I_{LEAK}	V_{IN} = 16 V, $V_{EN/SYNC}$ ≤ 0.4 V, V_{SW} = 0 V T_A = T_J between –40°C and 85°C		–	–	10	µA
		V_{IN} = 16 V, $V_{EN/SYNC}$ ≤ 0.4 V, V_{SW} = 0 V, T_A = T_J = 125°C		–	50	150	µA
Low-Side MOSFET On Resistance	$R_{DS(on)LS}$	I_{DS} = 10 mA, (V_{BOOT} – V_{SW}) < 4 V		–	10	12	Ω

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ELECTRICAL CHARACTERISTICS [1] (continued): Valid at V_{IN} = 12 V, T_A = 25°C , • indicates specifications guaranteed through –40°C ≤ T_J ≤ 125°C; unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ. [2]	Max.	Unit
OSCILLATOR FREQUENCY							
Oscillator Frequency	f_{SW}	R_{FSET} = 9.09 kΩ	•	2.20	2.45	2.70	MHz
		R_{FSET} = 24.9 kΩ	•	0.90	1.00	1.10	MHz
		R_{FSET} = 105 kΩ		–	0.250	–	MHz
SYNCHRONIZATION TIMING							
Synchronization Frequency Range	f_{SW_MULT}			1.2 × f_{SW}	–	1.5 × f_{SW}	MHz
Synchronized PWM Frequency	f_{SW_SYNC}			–	–	2.9	MHz
Synchronization Input Duty Cycle	D_{SYNC}			–	–	80	%
Synchronization Input Pulse Width	t_{WSYNC}			200	–	–	ns
Synchronization Input Edge Rise Time	t_{rSYNC}			–	10	15	ns
Synchronization Input Edge Fall Time	t_{fSYNC}			–	10	15	ns
ENABLE/SYNCHRONIZATION INPUT							
EN/SYNC High Threshold	V_{ENIH}	$V_{EN/SYNC}$ rising	•	–	1.65	1.80	V
EN/SYNC Low Threshold	V_{ENIL}	$V_{EN/SYNC}$ falling	•	–	1.25	–	V
EN/SYNC Low Threshold (Sleep)	$V_{ENILSLEEP}$	$V_{EN/SYNC}$ falling	•	0.40	0.85	–	V
EN/SYNC Hysteresis	V_{ENHYS}	$V_{ENIH} – V_{ENIL}$		–	400	–	mV
EN/SYNC Digital Delay	t_{SLEEP}	$V_{EN/SYNC}$ transitioning high or low cycles		–	32	–	PWM cycles
EN/SYNC Input Resistance	$R_{EN/SYNC}$		•	20	40	–	kΩ
OVERCURRENT PROTECTION (OCP) AND HICCUP MODE							
Pulse-by-Pulse Current Limit	I_{LIM}	Duty cycle = 5%, EN/SYNC = High (no sync)	•	4.90	5.65	6.45	A
		Duty cycle = 90%, EN/SYNC = High (no sync)	•	4.00	4.75	5.50	A
Hiccup Disable Threshold	V_{HICDIS}	V_{FB} rising		–	750	–	mV
Hiccup Enable Threshold	V_{HICEN}	V_{FB} falling		–	625	–	mV
OCP / HICCUP Count Limit	OCP_{LIMIT}	Hiccup enabled, OCP pulses		–	7	–	counts
OVERVOLTAGE PROTECTION (OVP)							
OVP Comparator Threshold	$V_{OVPTRIP}$	V_{FBX} rising, as a percentage of V_{REF}	•	112	114	116	%
FBX Time Constant (Filtering) [4]	τ_{FBX}			–	125	–	ns
Soft Start (SS)							
SS COMP Release Voltage	$V_{SSRELEASE}$	V_{SS} rising due to I_{SSSU}		255	330	–	mV
SS Fault/Hiccup Reset Voltage	$V_{SSRESET}$	V_{SS} falling due to I_{SSHIC}		–	235	310	mV
SS Maximum Charge Voltage	V_{SSCHRG}			–	3.1	–	V
SS Startup (Source) Current	I_{SSSU}	V_{SS} = 1 V, HICCUP = FAULT = 0	•	−10	–20	−30	µA
SS Hiccup (Sink) Current	I_{SSHIC}	V_{SS} = 0.5 V, HICCUP = 1	•	5	10	20	µA

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ELECTRICAL CHARACTERISTICS [1] (continued): Valid at V_{IN} = 12 V, T_A = 25°C , • indicates specifications guaranteed through –40°C ≤ T_J ≤ 125°C; unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ. [2]	Max.	Unit
SOFT START (SS) (continued)							
SS Input Resistance	R_{SS}	FAULT = 1		–	3.5	–	kΩ
SS to VOUT Delay Time	$t_{SSDELAY}$	C_{SS} = 22 nF		–	363	–	µs
VOUT Soft Start Ramp Time	t_{SS}	C_{SS} = 22 nF		–	880	–	µs
SS Switching Frequency	f_{SS}	V_{FB} = 0 V		–	f_{SW} / 3	–	MHz
		V_{FB} ≥ 600 mV		–	f_{SW}	–	MHz
POWER OK (POK) OUTPUT							
POK Output Voltage	V_{POK}	I_{POK} = 4 mA	•	–	–	0.4	V
POK Leakage	$I_{POKLEAK}$	V_{POK} = 5 V		–	–	1	µA
POK Comparator Threshold	$V_{POKTHRESH}$	V_{FB} rising, as a percentage of V_{REF}	•	87	90	93	%
POK Hysteresis	V_{POKHYS}	V_{FB} falling, as a percentage of V_{REF}		2	5	6	%
POK Digital Delay	t_{dPOK}	V_{FB} rising only		–	7	–	PWM cycles
THERMAL PROTECTION (TSD)							
Thermal Shutdown Threshold [4]	T_{TSD}	Temperature rising		150	165	–	°C
Thermal Shutdown Hysteresis [4]	T_{TSDHYS}			–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

[2] Typical specifications are at T_A = 25ºC.

[3] For T_A = T_J between –40°C and 85°C, ensured by design and characterization, not production tested.

[4] Ensured by design and characterization, not production tested.

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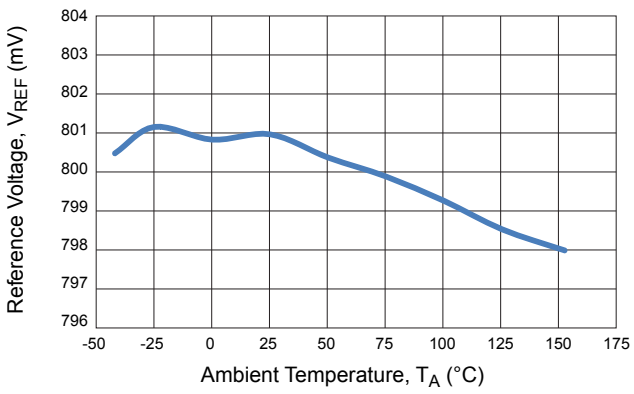
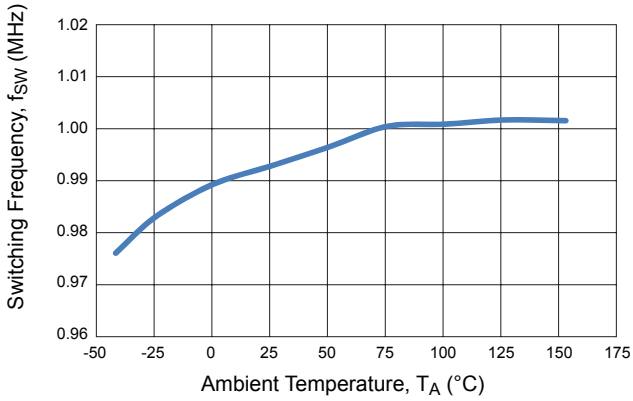
TYPICAL CHARACTERISTIC PERFORMANCE

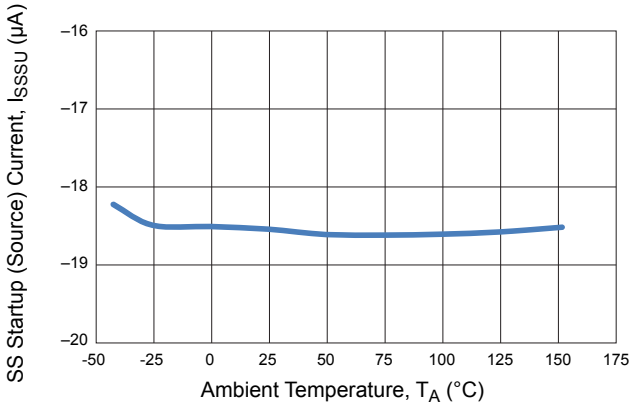
Reference Voltage versus Temperature



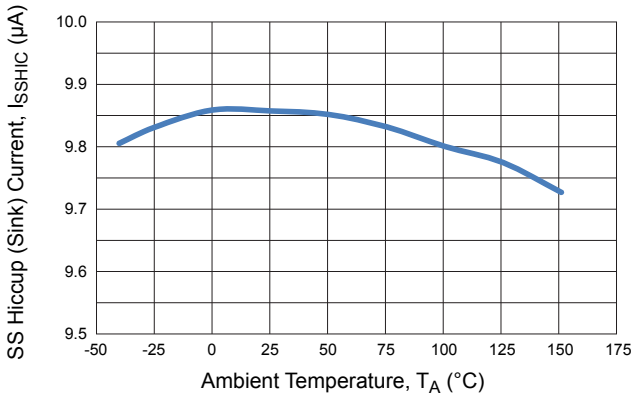
Switching Frequency versus Temperature



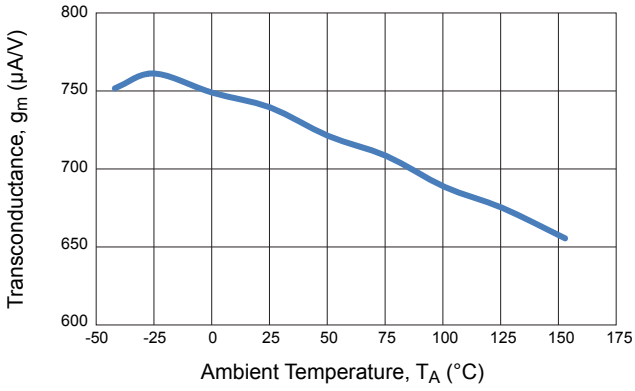
Soft Start (Source) Current versus Temperature



Soft Start Hiccup (Sink) Current versus Temperature

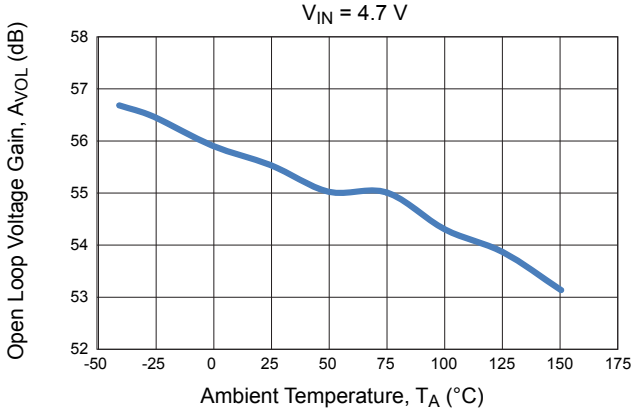


Error Amplifier Transconductance versus Temperature



Error Amplifier Voltage Gain versus Temperature

V_{IN} = 4.7 V



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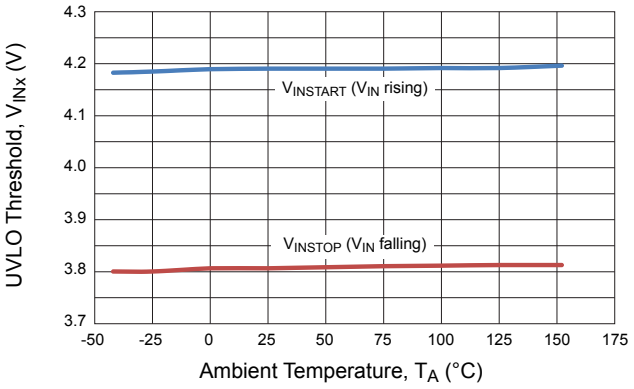
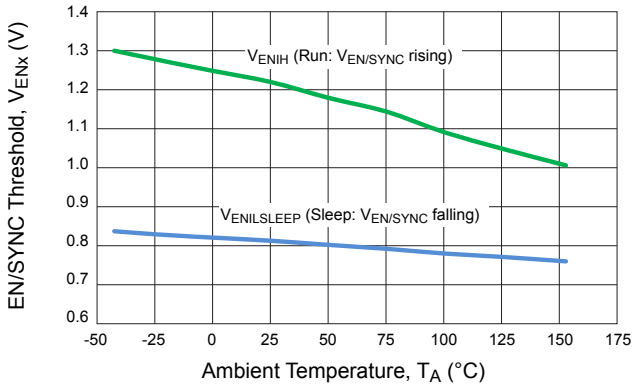
UVLO Threshold Voltage versus Temperature

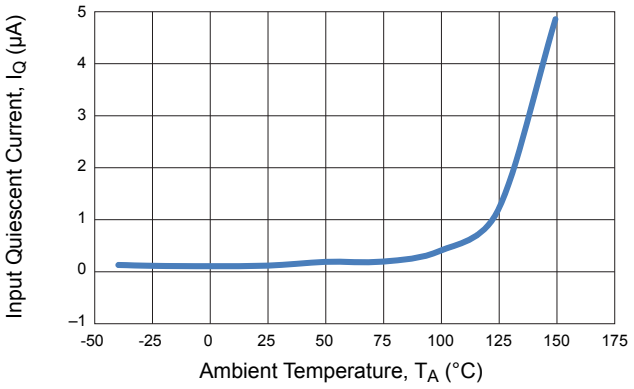


Enable Threshold Voltage versus Temperature



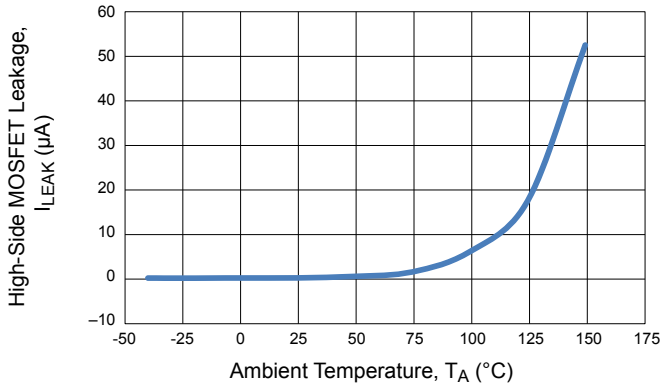
Sleep Input Current versus Temperature

V_{IN} = 16 V, EN/SYNC = Low

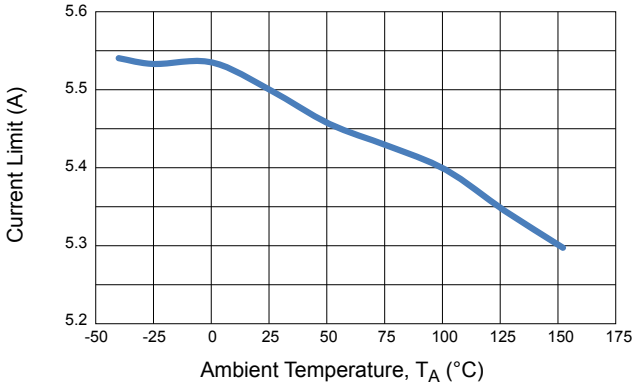


SW Leakage Output Current versus Temperature

V_{IN} = 16 V, EN/SYNC = Low



Switch Overcurrent Limit versus Temperature



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FUNCTIONAL DESCRIPTION

Overview

The A8583 is an asynchronous PWM regulator that incorporates all the control and protection circuitry necessary to satisfy a wide range of applications. The A8583 employs current mode control to provide fast transient response, simple compensation, and excellent stability. The features of the A8583 include a precision reference, an adjustable switching frequency, a transconductance error amplifier, an enable/synchronization input, an integrated high-side N-channel MOSFET, adjustable soft-start time, pre-bias startup, low current Sleep mode, and a Power OK (POK) output. The protection features of the A8583 include undervoltage lockout (UVLO), pulse-by-pulse over current protection (OCP), hiccup mode short-circuit protection (HIC), overvoltage protection (OVP), and thermal shutdown (TSD). In addition, the A8583 provides open-circuit, adjacent pin short-circuit, and pin-to-ground short circuit protection.

Reference Voltage

The A8583 incorporates an internal reference that allows output voltages as low as 0.8 V. The accuracy of the internal reference is ±1% through the operating temperature range. The output voltage of the regulator is adjusted by connecting a resistor divider (RFB1 and RFB2 in figure 1) from VOUT to the FB pin of the A8583.

Oscillator/Switching Frequency

The PWM switching frequency of the A8583 is adjustable from 250 kHz to 2.4 MHz and has an accuracy of ±12% through the operating temperature range. Connecting a resistor from the FSET pin to GND, as shown in figure 1, sets the switching frequency. An FSET resistor with 1% tolerance is recommended. A graph of switching frequency versus FSET resistor value is shown in the Design and Component Selection section of this data sheet.

Transconductance Error Amplifier

The primary function of the transconductance error amplifier is to regulate the converter output voltage. The error amplifier is shown in figure 2. It is shown as a 3-terminal input device with two positive and one negative inputs. The negative input is simply connected to the FB pin and is used to sense the feedback voltage for regulation. The two positive inputs are used for soft start and regulation. The error amplifier performs an “analog OR” selection between the two positive inputs. The error amplifier regulates to either the soft start pin voltage (minus 400 mV) or the A8583 internal reference, whichever is lower. To stabilize the regulator, a series RC compensation network (RZ and CZ) must be connected from the error amplifier output (COMP pin) to GND as shown in figure 1. In some applications, an additional, low value capacitor (CP) may be connected in parallel with the RC compensation network to reduce the loop gain at higher frequencies. However, if the CP capacitor is too large, the phase margin of the converter may be reduced. If the regulator is disabled or a fault occurs, the COMP pin is immediately pulled to GND via approximately 1500 Ω, and PWM switching is inhibited.

Slope Compensation

The A8583 incorporates internal slope compensation to allow PWM duty cycles above 50% for a wide range of input/output voltages, switching frequencies, and inductor values. As shown in the Functional Block diagram, the slope compensation signal is added to the sum of the current sense and PWM ramp offset. The amount of slope compensation is scaled directly with the switching frequency.

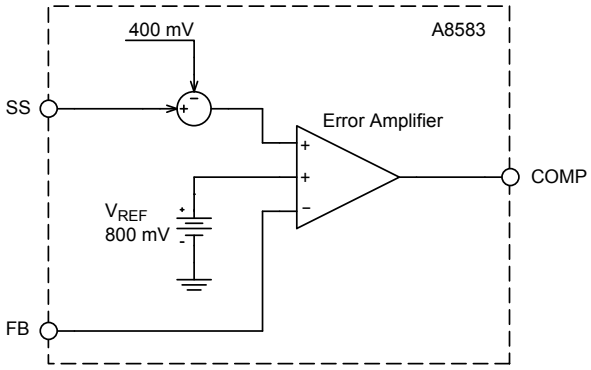

Figure 2. The A8583 transconductance error amplifier

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Sleep Mode

If the voltage at the EN/SYNC pin is pulled below 400 mV ($V_{ENILSLEEP}$) the A8583 will enter a Sleep mode where the internal control circuits will be shut off and draw less than 3 µA from V_{IN}. However, the total current drawn by the VIN pin will be the sum of the current drawn by the control circuitry (<3 µA) plus any leakage due to the high-side MOSFET (<10 µA at 25°C).

Enable/Synchronization (EN/SYNC) Input

The enable/synchronization (EN/SYNC) input provides three functions:

- A control input that commands the Sleep mode of the A8583. When EN/SYNC is very low ($V_{EN/SYNC} < V_{ENILSLEEP}$), most of the internal circuits are de-biased to provide the Sleep mode current of less than 3 µA.
- A simple logic input. If EN/SYNC is a logic low ($V_{EN/SYNC} < V_{ENIL}$), then the A8583 and VOUT will be off. If EN/SYNC is a logic high ($V_{EN/SYNC} > V_{ENIH}$), the A8583 will turn on and, provided there are no fault conditions, soft start will be initiated and VOUT will ramp to its final voltage in a time set by the soft start capacitor (CSS). (The operating modes of the A8583 based on EN/SYNC voltage are summarized in figure 3.)
- A synchronization input that accepts an external clock to turn on the A8583 and (after soft starting) will scale the PWM switching frequency from 1.2X to 1.5X above the base frequency set by the FSET resistor.

Note that, when used as a synchronization input, soft start is at the base frequency set by the FSET resistor. Synchronization to the external clock occurs after soft start is completed (when $V_{FB} > V_{POKTHRESH}$). When being used as a synchronization input, the applied clock pulses must satisfy the pulse width, duty-cycle, and rise/fall time requirements shown in the Electrical Characteristics table in this data sheet.

To automatically enable the A8583, the EN/SYNC input pin may be connected to a voltage rail, such as V_{IN}, via a resistor and a Zener diode as shown in figure 4.

There is a short delay between when EN/SYNC transitions low and when PWM switching stops. This is necessary because the enable circuitry must distinguish between a constant logic level and synchronization pulses at the lowest switching frequency. The nominal delay from when EN/SYNC transitions low and PWM switching stopping is 32 PWM clock cycles. The shut-

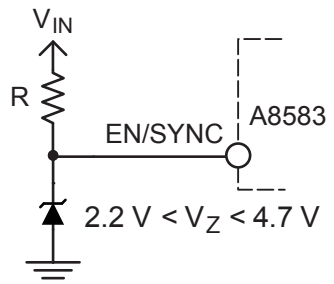

Figure 4. Automatically enabling the A8583 from VIN or some other power rail

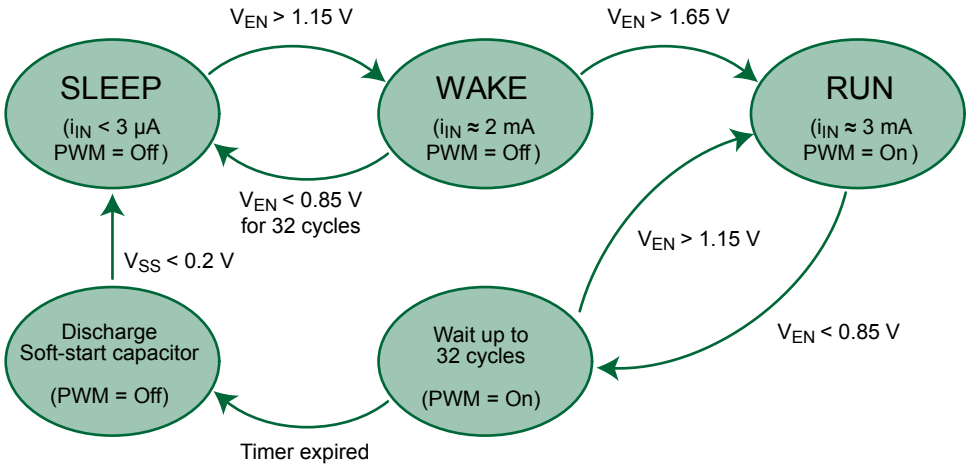

Figure 3. EN/SYNC voltage and A8583 operating modes

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down transition delay from switching to Sleep mode is shown in figure 5.

Power MOSFETs

The A8583 includes a low $R_{DS(on)}$, high-side N-channel MOSFET capable of delivering up to 3.5 A of current at high duty cycles. The A8583 also includes a 10 Ω, low-side MOSFET to ensure the boot capacitor (CBOOT) is always charged.

Unlike other typical asynchronous regulators, the A8583 only turns on the lower MOSFET when the boot capacitor must be charged. This minimizes negative currents in the output inductor and improves the light load efficiency. When the EN/SYNC input is low or a fault occurs, the A8583 is disabled and the regulator output stage is tri-stated by turning off both the upper and lower MOSFETs.

Pulse Width Modulation (PWM)

A high-speed PWM comparator, capable of pulse widths less than 100 ns, is included in the A8583. The inverting input of the comparator is connected to the output of the error amplifier. The noninverting input is connected to the sum of the current sense signal, the slope compensation, and a PWM Ramp Offset ($V_{PWMOFFSET}$, nominally 300 mV). At the beginning of each PWM cycle, the CLK signal sets the PWM flip-flop and the upper MOSFET is turned on. When the summation of the DC offset, the slope compensation, and the current sense signal rises above the error amplifier voltage, the comparator will reset the PWM flip-flop and the upper MOSFET will be turned off. If the output voltage of the error amplifier drops below the PWM Ramp Offset ($V_{PWMOFFSET}$) then zero PWM duty-cycle (pulse skipping) operation is achieved.

Current Sense Amplifier

A high-bandwidth current sense amplifier monitors the current in the upper MOSFET. The PWM comparator, the pulse-by-pulse current limiter, and the hiccup mode up/down counter require the current signal.

Soft Start (Startup) and Inrush Current Control

Inrush currents to the converter are controlled by the soft start function of the A8583. When the A8583 is enabled and all faults are cleared, the soft start (SS) pin will source approximately 20 µA (I_{SSSU}) and the voltage on the soft start capacitor (CSS) will ramp upward from 0 V. When the voltage on the soft start pin exceeds the Soft Start COMP Release Voltage threshold ($V_{SSRELEASE}$, 330 mV typical, measured at the soft start pin) the output of the error amplifier is released, and shortly thereafter the upper and lower MOSFETs will begin switching. As shown in figure 6, there is a short delay ($t_{SSDELAY}$) to initiate PWM switching, between when the EN/SYNC pin transitions high and when the soft start voltage reaches 330 mV.

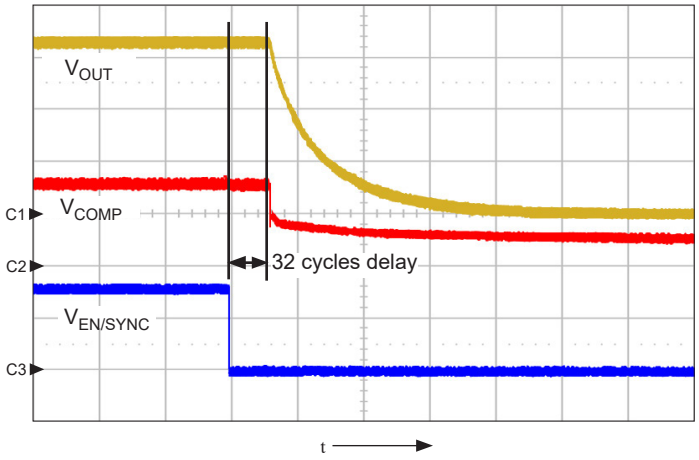

Figure 5. PWM switching stops and sleep mode begins approximately 32 cycles after EN/SYNC transitions low; shows V_{OUT} (ch1, 1 V/div.), V_{COMP} (ch2, 1 V/div.), $V_{EN/SYNC}$ (ch3, 2 V/div.), t = 50 µs/div.

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When the A8583 begins PWM switching, the error amplifier regulates the voltage at the FB pin to the soft start pin voltage minus the Soft Start PWM Threshold voltage (V_{SSPWM}). When PWM switching starts, the voltage at the soft start pin rises from 330 mV to 1.13 V (a difference of 800 mV), the voltage at the FB pin rises from 0 V to 800 mV, and the regulator output voltage rises from 0 V to the required set-point determined by the feedback resistor divider (RFB1 and RFB2).

When the voltage at the soft start pin reaches approximately 1.13 V, the error amplifier will "switch over" and begin regulating to the A8583 internal reference, 800 mV. The voltage at the soft start pin will continue to rise to about 3.3 V. The soft start functionality is shown in figure 6.

If the A8583 is disabled or a fault occurs, the internal fault latch is set, and the soft start pin is pulled to GND via approximately 3.5 kΩ. The A8583 will clear the internal fault latch when the voltage at the soft start pin decays to approximately 235 mV ($V_{SSRESET}$).

If the A8583 enters hiccup mode, the capacitor on the soft start pin is discharged by a 10 µA current sink (I_{SSHIC}). Therefore, the soft start pin capacitor value (CSS) controls the time between soft start attempts. Hiccup mode operation is discussed in more detail in the Output Short Circuit (Hiccup Mode) Protection section of this data sheet. During startup, the PWM switching frequency is scaled linearly from f_{SW} / 3 to f_{SW} as the voltage at the FB pin ramps from 0 V to 600 mV. This is done to minimize the peak current in the output inductor when the input voltage is high and the output of the regulator is either shorted, or soft starting a relatively high output capacitance.

Pre-Biased Startup

If the output capacitors are pre-biased to some voltage, the A8583 will modify the normal startup routine to prevent discharging the output capacitors. Normally, the COMP pin is released and PWM switching starts when the voltage at the soft start pin reaches 330 mV. In the case with pre-bias at the output, the pre-bias voltage will be sensed at the FB pin. The A8583 will not start switching until the voltage at the soft-start pin increases to approximately V_{FB} + 330 mV. At this soft start pin voltage, the error amplifier output is released, the voltage at the COMP pin rises, PWM switching starts, and V_{OUT} will ramp upward starting from the pre-bias level. Figure 7 shows startup when the output voltage is pre-biased to 2.0 V.

Power OK (POK) Output

The Power OK (POK) output is an open drain output, so an external pull-up resistor must be connected. An internal comparator monitors the voltage at the FB pin and controls the open drain device at the POK pin. POK remains low until the voltage at the FB pin is within 10% of the final regulation voltage. The POK output is pulled low if: (1) the EN/SYNC pin transitions low for more than 32 PWM cycles, (2) UVLO occurs, (3) TSD occurs, or (4) OVP occurs.

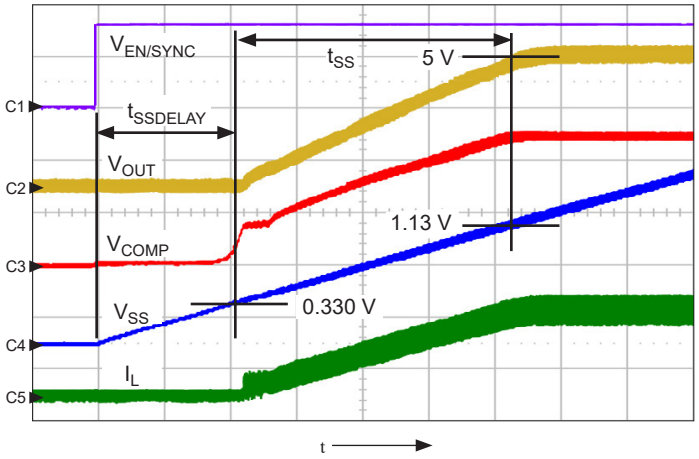

Figure 6. Startup to V_{OUT} = 5 V, 2.0 A, with C_{SS} = 22 nF; shows $V_{EN/SYNC}$ (ch1, 2 V/div.), V_{OUT} (ch2, 2 V/div.), V_{COMP} (ch3, 500 mV/div.), V_{SS} (ch4, 500 mV/div.), I_L (ch5, 2 A/div.), t = 200 µs/div.

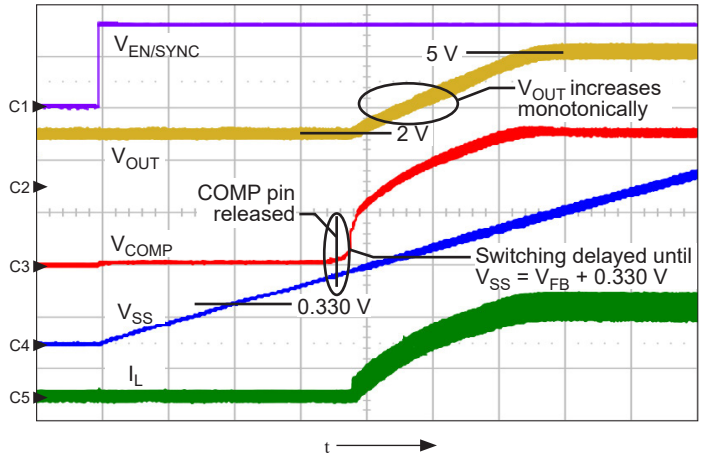

Figure 7. Startup to V_{OUT} = 5 V, with V_{OUT} pre-biased to 2 V; shows $V_{EN/SYNC}$ (ch1, 2 V/div.), V_{OUT} (ch2, 2 V/div.), V_{COMP} (ch3, 500 mV/div.), V_{SS} (ch4, 500 mV/div.), I_L (ch5, 2 A/div.), t = 200 µs/div.

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If the A8583 is running and EN/SYNC transitions low, then after 32 PWM cycles, POK will transition low and remain low only as long as the internal rail is able to enhance the open drain output device. After the internal rail collapses, POK will return to the high impedance state. The POK comparator incorporates hysteresis to prevent chattering due to voltage ripple at the FB pin.

Protection Features

Undervoltage Lockout (UVLO)

An Undervoltage Lockout (UVLO) comparator monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the lockout threshold ($V_{INSTART}$). The UVLO comparator incorporates enough hysteresis ($V_{UVLOHYS}$) to prevent on/off cycling of the regulator due to IR drops in the V_{IN} path during heavy loading or during startup.

Thermal Shutdown (TSD)

The A8583 protects itself from over-heating, with an internal thermal monitoring circuit. If the junction temperature exceeds the upper thermal shutdown threshold (T_{TSD}, nominally 165°C) the voltages at the soft start and COMP pins will be pulled to GND and both the upper and lower MOSFETs will be shut off. The A8583 will stop PWM switching and stay in WAKE state (see figure 3). It will automatically restart when the junction temperature decreases more than the thermal shutdown hysteresis (T_{TSDHYS}, nominally 20°C).

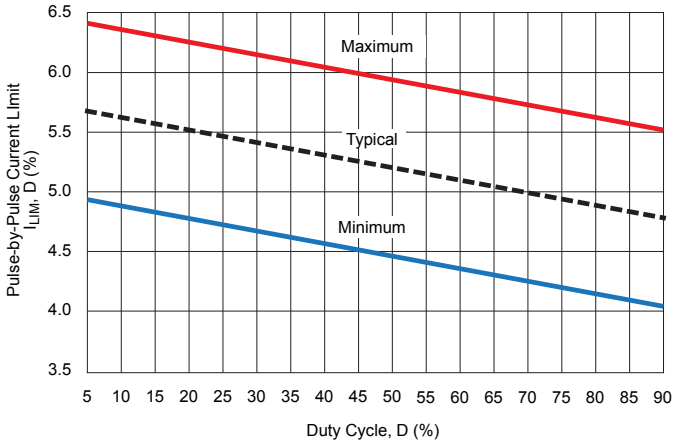

Figure 8. Pulse-by-pulse current limit versus duty cycle

Overvoltage Protection (OVP)

The A8583 provides a remote sense input pin (FBX) to protect the system from an overvoltage condition. An overvoltage condition will occur if the FB pin is inadvertently grounded, the series feedback resistor (RFB1 in figure 1) is missing, the FB pin is not soldered, the FB trace is broken, or the COMP pin is shorted to a voltage higher than approximately 1.6 V. When an overvoltage condition is detected: (1) the fault is latched, (2) PWM switching stops, and (3) POK, SS, and COMP are pulled low. An OVP fault may be cleared by either toggling the EN/SYNC input or cycling power to the VIN pin.

The FBX pin should be connected to VOUT using a feedback resistor divider as shown in figure 1. To prevent nuisance trips, it is recommended that a capacitor (CFBX) be included from FBX to ground to place a pole at approximately 2X to 5X the system crossover frequency, f_C (see the Compensation Components section of this data sheet). For optimal protection, the trace that connects the FBX resistor divider should be separate from the trace that connects the FB resistor divider. If the OVP function is not required, the FBX pin can be grounded to essentially disable the OVP comparator.

Usually, the FBX resistor divider will be identical to the FB resistor divider and the OVP threshold will be equal to $V_{OVPTRIP}$ shown in the Electrical Characteristics table (nominally 114% of V_{REF}). However, if nuisance trips occur during transient situations, the OVP trip threshold can be scaled slightly higher by using a resistor divider that provides less voltage at the FBX pin. Reducing the signal at the FBX pin essentially desensitizes the OVP circuit, so care should be taken not to increase the OVP trip threshold beyond a reasonable amount.

Table 1. Pulse-by-Pulse Current Limit versus Duty Cycle

D (%)	I_{LIM} (A)		
	Min.	Typ.	Max.
5	4.89	5.64	6.45
20	4.75	5.48	6.23
40	4.52	5.27	6.02
60	4.31	5.06	5.81
80	4.10	4.85	5.60
90	4.00	4.75	5.50

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Pulse-by-Pulse Overcurrent Protection (OCP)

The A8583 monitors the current in the upper MOSFET and if the current exceeds the pulse-by-pulse overcurrent threshold (I_{LIM}) then the upper MOSFET is turned off. Normal PWM operation resumes on the next clock pulse from the oscillator. The A8583 includes leading edge blanking to prevent falsely triggering the pulse-by-pulse current limit when the upper MOSFET is turned on. Pulse-by-pulse current limiting is always active.

The A8583 is conservatively rated to deliver 3.5 A for most applications. However, the exact current it can support is heavily dependent on duty cycle, ambient temperature, thermal resistance of the PCB, airflow, component selection, and nearby heat sources. The A8583 is designed to deliver more current at lower duty cycles and slightly less current at higher duty cycles. For example, the pulse-by-pulse limit at 20% duty cycle is ≥ 4.75 A but at 80% duty cycle the pulse limit is ≥ 4.10 A. Use table 1 and figure 8 to determine the real current limit, given the duty cycle required for each application. Take care to do a careful thermal solution or thermal shutdown will occur.

Output Short Circuit (Hiccup Mode) Protection

Hiccup mode protects the A8583 when the load is either too high or when the output of the converter is shorted to ground. When the voltage at the FB pin is below the Hiccup Enable Threshold (V_{HICEN}, nominally 625 mV), Hiccup mode protection is enabled. When the voltage at the FB pin is above the Hiccup Disable Threshold (V_{HICDIS}, nominally 750 mV), Hiccup mode protection is disabled.

Hiccup Mode overcurrent protection monitors the number of overcurrent events using an up/down counter: an overcurrent pulse increases the count by one, and a PWM cycle without an overcurrent pulse decreases the count by one. If the total count reaches more than 7 (while Hiccup mode is enabled) then the Hiccup latch is set and PWM switching is stopped. The Hiccup signal causes the COMP pin to be pulled low with a relatively low resistance (1500 Ω). Hiccup mode also enables a current sink connected to the soft start pin (nominally 10 µA) so, when Hiccup first occurs, the voltage at the soft start pin ramps downward. Hiccup mode operation is shown in figure 9.

When the voltage at the soft start pin decays to a low level ($V_{SSRESET}$, 235 mV typical), the Hiccup latch is cleared and the 10 µA soft start pin current sink is turned off. The soft start pin will resume charging the soft start capacitor with 20 µA and the voltage at the soft start pin will ramp upward. When the voltage at the soft start pin exceeds the COMP release threshold ($V_{SSRELEASE}$, 330 mV typical), the low resistance pull-down at the COMP pin will be turned off and the Error amplifier will force the voltage at the COMP pin to ramp up quickly, and PWM switching will begin. If the short circuit at the converter output remains, another Hiccup cycle will occur. Hiccups will repeat until the short circuit is removed or the converter is disabled. If the short circuit is removed, the A8583 will soft start normally and the output voltage will be ramped to the required level as shown in figure 9.

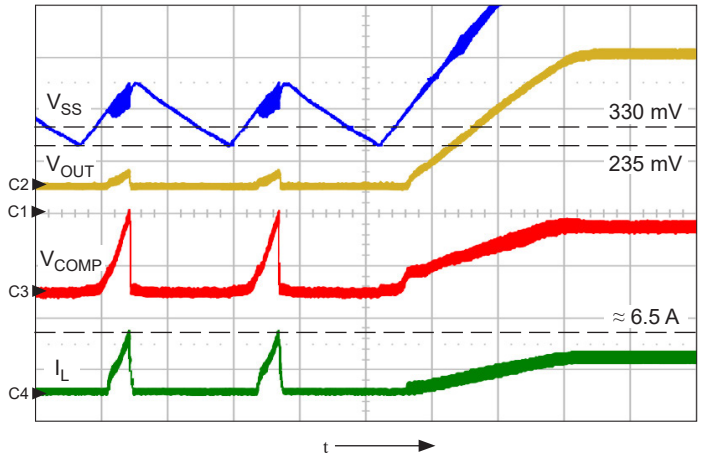

Figure 9. Hiccup mode operation and recovery ; shows V_{SS} (ch1, 200 mV/div.), V_{OUT} (ch2, 2 V/div.), V_{COMP} (ch3, 1 V/div.), I_L (ch4, 5 A/div.), t = 500 µs/div.

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APPLICATION INFORMATION

Design and Component Selection

Setting the Output Voltage (VOUT, RFB1, RFB2)

The output voltage of the A8583 is determined by connecting a resistor divider from the output node (VOUT) to the FB pin, as shown in figure 10. There are trade-offs when choosing the value of the feedback resisters. If the series combination (RFB1 + RFB2) is relatively low, the light load efficiency of the regulator will be reduced. So, to maximize the efficiency, it is best to choose high values for the resistors. On the other hand, if the parallel combination (RFB1 // RFB2) is too high, then the regulator may be susceptible to noise coupling into the FB pin. In general, the feedback resisters must satisfy the ratio shown in equation 1 to produce a required output voltage.

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT}}{0.8\ V} - 1 \quad (1)$$

Table 2 shows the most common output voltages and recommended feedback resistor values, assuming less than 0.2% efficiency loss at light load of 100 mA and a parallel combination of 4 kΩ presented to the FB pin. For optimal system accuracy, it is recommended that the feedback resistors have ≤1% tolerances.

PWM Switching Frequency (RFSET)

The PWM switching frequency is set by connecting a resistor from the FSET pin to ground. Figure 11 is a graph showing the relationship between the typical switching frequency (y axis) and the FSET resistor, $1/R_{FSET}$ (x axis). For a given switching frequency (f_{SW}), the FSET resistor can be calculated using equation 2, where f_{SW} is in kHz and R_{FSET} is in kΩ.

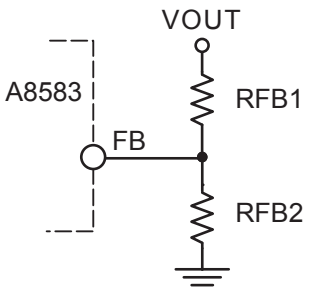

Figure 10. Connecting the feedback divider

$$R_{FSET} = \frac{26730}{f_{SW}} - 1.8 \quad (2)$$

When the PWM switching frequency is chosen, the designer should be aware of the minimum controllable PWM on-time, $t_{ON(MIN)}$ of the A8583. If the system required on-time is less than the A8583 minimum controllable on-time, then switch node jitter will occur, and the output voltage will have increased ripple or oscillations. The PWM switching frequency should be calculated using equation 3, where V_{OUT} is the output voltage, $t_{ON(MIN)}$ is the minimum controllable on-time of the A8583 (worst case of

Table 2. Recommended Feedback Resistor Values

V_{OUT} (V)	RFB1 VOUT to FB pin (kΩ)	RFB2 FB pin to GND (kΩ)
1.2	6.04	12.1
1.5	7.50	8.45
1.8	9.09	7.15
2.5	12.4	5.76
3.3	16.5	5.23
5.0	24.9	4.75
7.0	34.8	4.53
8.0	40.2	4.42
9.6	47.5	4.32

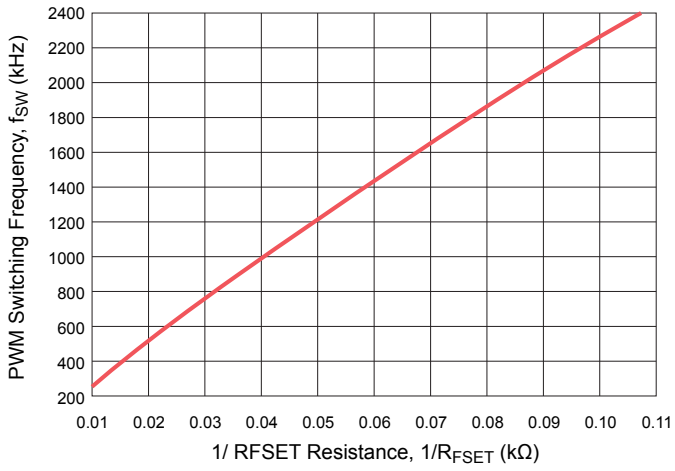

Figure 11. PWM switching frequency versus $1/R_{FSET}$

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100 ns), and $V_{IN(MAX)}$ is the maximum required operational input voltage to the A8583 (not the peak surge voltage).

$$f_{SW} < \frac{V_{OUT}}{t_{ON(MIN)} \times V_{IN(MAX)}} \quad (3)$$

If the A8583 synchronization function is employed, the base switching frequency should be chosen such that jitter will not result at the maximum synchronized switching frequency according to equation 3, that is, $1.5 \times f_{SW} < f_{SW}$ calculated by equation 2.

Output Inductor (L_O)

The value of the output inductor (L_O) is usually calculated to set a particular peak-to-peak ripple current in the inductor. However, the inductor physical size and cost will be directly proportional to the peak current or saturation specification. There are tradeoffs among: peak-to-peak ripple current, system efficiency, transient response, and cost. If the peak-to-peak inductor ripple is chosen to be relatively high, then the inductor value will be low, the system efficiency will be reduced, the transient response will be fast, the inductor physical size will be small, and the cost reduced. If the peak-to-peak inductor ripple is chosen to be relatively low, then the inductor value will be high, the system efficiency will be higher, the transient response will be slow, the inductor physical size will be larger, and the cost will be increased.

Equation 4 can be used to estimate the inductor value, given a particular peak-to-peak ripple current (ΔI_L), input voltage (V_{IN}), output voltage (V_{OUT}), and switching frequency (f_{SW}). The reference designs in this data sheet use a peak-to-peak ripple current of 25% of the 3.5 A, DC rating of the A8583, or 0.875 A_{PP}.

$$L_O \geq \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

If the preceding equation yields an inductor value that is not a standard value, the next higher available value should be used.

After choosing a standard inductor value, equation 5 should be used to make sure the A8583 slope compensation is adequate. In this equation $V_{IN(MIN)}$ is the minimum required input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, and V_f is the forward voltage of the asynchronous Schottky diode.

$$L_O \geq 0.77 \times \frac{V_{OUT} + V_f}{f_{SW}} \left(1 - \frac{0.18 \times (V_{IN(MIN)} + V_f)}{V_{OUT} + V_f}\right) \quad (5)$$

Ideally, the rated saturation current of the inductor should be higher than the maximum current capability of the A8583 at the expected duty cycle. Unfortunately, this usually results in a physically larger, more costly inductor. At a minimum, the saturation current of the inductor should support the DC rating of the A8583 (3.5 A), plus ½ of the inductor peak-to-peak ripple current (usually 0.875 A_{PP}), the capacitive startup current (I_{CO}), and some margin for component, frequency, and voltage tolerances. For example, an inductor with a 4.5 A rating allows 3.5 A of load current, 0.4375 A_{PEAK} of ripple current, 0.25 A of capacitive startup current (I_{CO}), along with a 20% frequency decrease, a 20% inductance decrease, and a 10% input voltage increase (at 5.0 V_{OUT}, 12 V_{IN}, 2 MHz).

After an inductor is chosen, it should be tested during output short circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator are not damaged when the output is shorted to GND at maximum input voltage and the highest expected ambient temperature

Output Capacitors (COUT)

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage and they store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{OUT}) is a function of the output capacitor parameters: ESR_{CO}, ESL_{CO}, and C_O, as follows:

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{ESL} + \Delta V_{CO} \quad (6)$$

It is commonly known that, for a constant load on the regulator, the current in the output inductor is equal to the DC output current plus ΔI_L. Therefore, using Kirchhoff's current law, it can be shown that the current in the output capacitors is equal to the ripple current in the output inductor, or $I_C = \Delta I_L$. Knowing this, we can determine the first term in equation 6:

$$\Delta V_{ESR} = \Delta I_L \times ESR_{CO} \quad (7)$$

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To calculate the second term in equation 6, ΔV_{ESL}, we must determine the slope of the output inductor current, di/dt, which is $(V_{IN} - V_{OUT}) / L_O$:

$$\Delta V_{ESL} = L_O \frac{di}{dt} = ESL_{CO} \times \frac{V_{IN} - V_{OUT}}{L_O} \quad (8)$$

To calculate the third term in equation 6, we must understand that, over a single PWM cycle, the amount of charge into the output capacitors must equal the amount of charge out of the capacitors, or the capacitor output voltages would drift. What this means is the output inductor current (ΔI_L) flows in and out of the output capacitor and is centered at 0 A, as shown in figure 12. For any capacitor, the voltage is:

$$\Delta V_{CO} \geq \frac{1}{C_{OUT}} \int i \times dt$$

In this case, the integral term can be graphically calculated by examining the 2 areas, A1 and A2, shown in figure 12:

$$A1 = \frac{1}{2} \times \frac{\Delta I_L}{2} \times \frac{DT_S}{2} = \frac{\Delta I_L DT_S}{8}$$

$$A2 = \frac{1}{2} \times \frac{\Delta I_L}{2} \times \frac{(1-D)T_S}{2} = \frac{\Delta I_L T_S}{8} - \frac{\Delta I_L DT_S}{8}$$

$$\int i \times dt = A1 + A2 = \frac{\Delta I_L T_S}{8}$$

Substituting this into the equation for ΔV_{CO} results in:

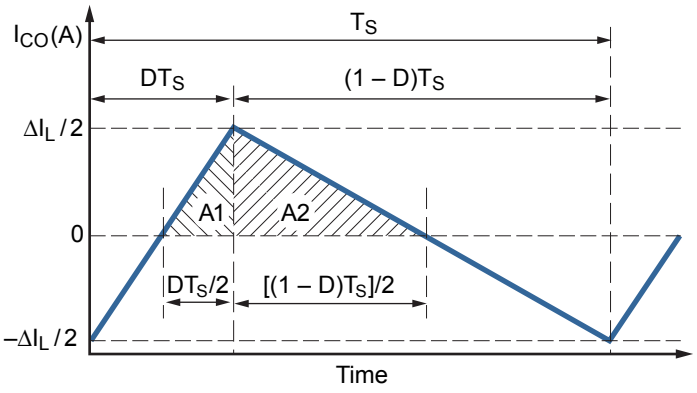

Figure 12. Output capacitor current waveform

$$\Delta V_{CO} = \frac{\Delta I_L T_S}{8 C_{OUT}} = \frac{\Delta I_L}{8 f_{SW} C_{OUT}} \quad (9)$$

Combining equations 7, 8, and 9 results in an expression for the total output voltage ripple:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO} + \frac{\Delta I_L}{8 f_{SW} C_{OUT}} \quad (10)$$

The type of output capacitors will determine which terms of equation 10 are dominant.

For ceramic output capacitors the ESR and ESL are extremely low, so the output voltage ripple will be dominated by the third term of equation 10:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 f_{SW} C_{OUT}} \quad (10a)$$

To reduce the voltage ripple of a design using ceramic output capacitors, simply: increase the total capacitance, reduce the inductor current ripple (that is, increase the inductor value), or increase the switching frequency.

For electrolytic output capacitors the value of capacitance will be relatively high, so the third term in equation 10 will be minimized and the output voltage ripple will be determined primarily by the first two terms of equation 10:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO} \quad (10b)$$

To reduce the voltage ripple of a design using electrolytic output capacitors, simply: decrease the equivalent ESR and ESL by using a high(er) quality capacitor, and/or add more capacitors in parallel, or reduce the inductor current ripple (that is, increase the inductor value). The ESR of some electrolytic capacitors can be quite high, so Allegro recommends choosing a quality capacitor that clearly documents the ESR or the total impedance in the data sheet. Also, the ESR of electrolytic capacitors usually increases significantly at cold ambient, which increases the output voltage ripple and, in many cases, reduces the stability of the system.

To reduce the output voltage ripple and save PCB area, a design could combine both ceramic and electrolytic capacitors in parallel. If this is done, the ceramic capacitors should be placed and grounded as close as possible to the load to be most effective. AC

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ripple voltage measurements should be made differentially across the ceramic capacitors with a very short ground lead.

The transient response of the A8583 depends on the number and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply: adding more capacitors in parallel, or by using higher quality capacitors. At the instant of a fast load transient (di/dt), the output voltage will change by the amount:

$$\Delta V_{OUT} = \Delta I_{LOAD} \times ESR_{CO} + \frac{di}{dt} ESL_{CO} \quad (11)$$

After the load transient occurs, the output voltage will deviate for a short time depending on the system bandwidth, the output inductor value, and output capacitance. After a short delay, the Error amplifier will bring the output voltage back to its nominal value. The speed at which the Error amplifier brings the output voltage back to its set point will depend mainly on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, a higher bandwidth system may be more difficult to obtain acceptable gain and phase margins. Selection of the compensation components (RZ, CZ, CP) are discussed in more detail in the Compensation Components section of this data sheet.

Input Capacitors (CIN)

Three factors should be considered when choosing the input capacitors. First, they must be chosen to support the maximum expected input voltage with adequate design margin. Second, their rms current rating must be higher than the expected rms input current to the regulator. Third, they must have enough capacitance and a low enough ESR to limit the input voltage dV/dt to something much less than the hysteresis of the UVLO circuitry (nominally 400 mV for the A8583) at maximum loading and minimum input voltage.

The input capacitors must deliver the rms current according to equation 12, where the duty cycle, $D \approx (V_{OUT} + V_f) / (V_{IN} + V_f)$ and V_f is the forward voltage of the asynchronous diode (D1 in figure 1):

$$I_{rms} = I_O \sqrt{D \times (1 - D)} \quad (12)$$

Figure 13 shows the normalized input capacitor rms current versus duty cycle. To use this graph, simply find the operational duty cycle (D) on the x axis and determine the input/output current multiplier on the y axis. For example, at a 20% duty cycle, the input/output current multiplier is 0.400. Therefore, if the regulator is delivering 3.5 A of steady-state load current, the input capacitor(s) must support 0.400 × 3.5 A or 1.4 A_{rms}. A single capacitor may support the rms input current requirement or several capacitors may have to be paralleled. Ceramic capacitors can deliver quite a bit of current but their total capacitance will be relatively low. For example, a 4.7 µF, 16 V, 1206, X7R ceramic capacitor can easily deliver 3 to 4 A_{rms}.

Electrolytic capacitors can typically deliver 100 to 500 mA_{rms} of current so 2 or 3 of these may be required to support the ripple current. Electrolytic capacitors will typically offer much more capacitance than the same quantity of ceramic capacitors. So, electrolytic capacitors are typically able to provide more current over extended periods of time where V_{IN} would otherwise droop. However, ceramic capacitors have very low ESR and inductance, so they are best for filtering the high frequency switching noise. A good design will employ both types of capacitors with the ceramic capacitors placed closest to the input pin of the A8583.

The input capacitors must limit the voltage deviations at the V_{IN} pin to something significantly less than the A8583 UVLO hysteresis during maximum load and minimum input voltage. Equation 13 allows us to calculate the minimum input capacitance:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{f_{SW(MIN)} \times (\Delta V_{IN(MIN)} - I_{OUT} \times ESR_{CIN})} \quad (13)$$

Where $\Delta V_{IN(MIN)}$ is chosen to be much less than the hysteresis of the VIN UVLO comparator ($\Delta V_{IN(MIN)} \leq 100$ mV is

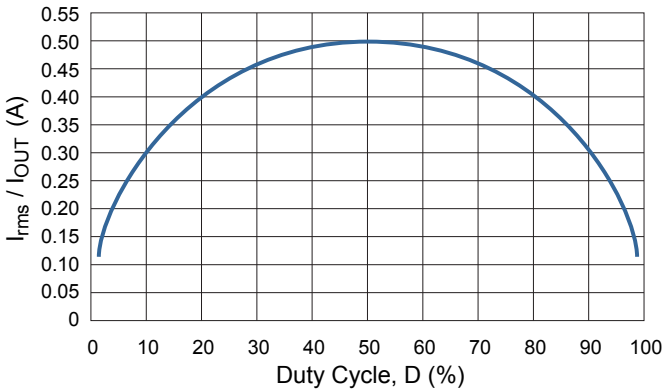

Figure 13. Normalized input capacitor ripple current versus duty cycle

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recommended), $f_{SW(MIN)}$ is the lowest expected PWM frequency, and ESR_{CIN} is the equivalent series resistance of the input capacitor(s).

If we choose ceramic input capacitors (ESR < 5 mΩ), the $I_{OUT} \times ESR_{CIN}$ term can be neglected in equation 13. Also, the $D \times (1 - D)$ term has an absolute maximum value of 0.25 at 50% duty cycle. So, for a conservative design, based on I_{OUT} = 3.5 A, $f_{SW(MIN)}$ = 1.6 MHz (2 MHz – 20%), $D \times (1 - D)$ = 0.25, and ΔV_{IN} =100 mV:

$$C_{IN} \geq \frac{3.5\ (A) \times 0.25}{1.6\ (MHz) \times 100\ (mV)} = 5.5\ \mu F$$

A good design should consider the DC-bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction) so these types should be avoided. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

For all ceramic capacitors, the DC-bias effect is even more pronounced on smaller case sizes, so a good design will use the largest affordable case size (such as 1206 or 1210). Also, it is advisable to select input capacitors with plenty of design margin in the voltage rating, to accommodate the worst case transient input voltage (for example, load dump as high as 40 V for automotive applications).

Asynchronous Diode (D1)

There are three requirements for the asynchronous diode. First, the asynchronous diode must be able to withstand the regulator input voltage when the high-side MOSFET is on. Therefore, the design should have a diode with a reverse voltage rating (V_r) higher than the maximum expected input voltage (that is, the surge voltage). Second, the forward voltage of the diode (V_f) should be minimized or the regulator efficiency will suffer. Also, if V_f is too high, the missing diode protection in the A8583 could be falsely activated. A Schottky-type diode, which can maintain a very low V_f when the converter output is shorted to ground at the coldest ambient temperature, is highly recommended. Third, the asynchronous diode must conduct the output current when the high-side MOSFET is off. Therefore, the average forward current rating of this diode ($I_{f(av)}$) must be high enough to deliver the load current according to equation 14, where D is the duty cycle $(V_{OUT} + V_f) / (V_{IN} + V_f)$ and $I_{OUT}(max)$ is the maximum continuous ouput current of the regulator:

$$I_{f(av)} \geq I_{OUT}(max)\ (1 - D(min)) \quad (14)$$

To save cost and PCB area, the designer might be tempted to use a diode with a relatively low current rating and the smallest PCB footprint. However, doing this usually results in a hotter diode and lower system efficiency. For the asynchronous converter, the majority of losses can occur in this diode. To optimize efficiency, one should use a higher rated, physically larger diode. Also, diodes with very high reverse voltage ratings usually have higher forward voltages, which reduces system efficiency. Therefore, a diode with the lowest possible reverse voltage rating should be used. However, care should be taken to be sure this diode is not destroyed during input voltage transients or surge events.

Bootstrap Capacitor (CBOOT)

A bootstrap capacitor must be connected between the BOOT and SW pins to provide floating gate drive to the high-side MOSFET. For most applications 100 nF is sufficient. This should be a high-quality ceramic capacitor, such as an X5R or X7R, with a voltage rating of at least 16 V. The A8583 incorporates a low-side MOSFET to ensure that the bootstrap capacitor is always charged, even when the converter is lightly loaded.

Soft Start and Hiccup Mode Timing (CSS)

The soft start time of the A8583 is determined by the value of the capacitance on the SS pin. When the A8583 is enabled, the voltage at the SS pin will start from 0 V and will be charged by the soft start current, I_{SSSU} (nominally 20 µA). However, PWM switching will not begin instantly because the voltage at the SS pin must rise above the COMP release voltage, $V_{SSRELEASE}$ (nominally 0.33 V). The soft start delay ($t_{SSDELAY}$) can be calculated using equation 15:

$$t_{SSDELAY} = C_{SS} \times \frac{0.33\ (V)}{I_{SSSU}} \quad (15)$$

If the A8583 is starting into a full load (nominally 3.5 A) and the soft start time (t_{SS}) is too fast, the pulse-by-pulse overcurrent threshold may be exceeded and Hiccup mode protection triggered. This occurs because the total of the full load current, the inductor ripple current, and the additional current required to

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charge the output capacitors ($I_{CO} = C_O \times dV_{OUT}/dt_{SS}$) is higher than the pulse-by-pulse current threshold, as shown in figure 14. This phenomenon is more pronounced when using high value electrolytic type output capacitors.

To avoid prematurely triggering hiccup mode the soft start capacitor, CSS, should be calculated using the following formula:

$$C_{SS} \geq \frac{20\ (\mu A) \times V_{OUT} \times C_{OUT}}{0.8\ (V) \times I_{CO}} \quad (16)$$

Where V_{OUT} is the output voltage, C_{OUT} is the output capacitance, I_{CO} is the amount of current allowed to charge the output capacitance during soft start (Allegro recommends 0.125 A < I_{CO} < 0.375 A). Higher values of I_{CO} result in faster soft start times. However, lower values of I_{CO} ensure that Hiccup mode is not falsely triggered as components vary.

Components can easily change due to initial tolerances, aging, or temperature (output capacitance, soft start capacitance, soft start charging currents, and so forth). Allegro recommends starting the design with an I_{CO} of 0.125 A and increasing it only if the soft start time is too slow. If a non-standard capacitor value for C_{SS} is calculated, the next larger value should be used.

The output voltage ramp time, t_{SS}, can be calculated by using either of the following formulas:

$$t_{SS} = V_{OUT} \times \frac{C_{OUT}}{I_{CO}} \quad (17a)$$

or

$$t_{SS} = 0.8\ (V) \times \frac{C_{SS}}{20\ (\mu A)} \quad (17b)$$

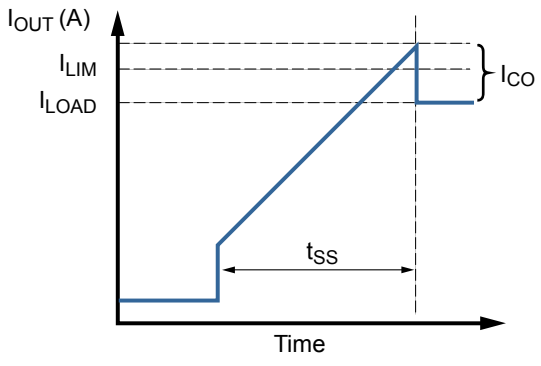

Figure 14. Output capacitor current (I_{CO}) during startup

When the A8583 is in Hiccup mode, the CSS capacitor is used as a timing capacitor and sets the hiccup period. The SS pin charges the CSS capacitor with I_{SSSU} (nominally 20 µA) during a startup attempt and discharges the CSS capacitor with I_{SSHIC} (nominally 10 µA) between startup attempts. Because the ratio of the SS pin currents is 2:1, the time between hiccups will be at least twice as long as the startup time. Therefore, the effective duty-cycle of the A8583 will be very low when the output is shorted to ground. With such a low duty cycle, the junction temperature of the A8583 will be maintained at an extremely low value, compared to other short circuit protection techniques.

Compensation Components (RZ, CZ, CP)

To compensate the system, it is important to understand where the buck power stage, load resistance, and output capacitance form their poles and zeros in frequency. Also, it is important to understand that the compensated Error amplifier introduces a zero and two more poles, and where these should be placed to maximize system stability, provide a high bandwidth, and optimize the transient response.

First, look at the power stage of the A8583, the output capacitors, and the load resistance. This circuitry is commonly referred as the “control to output” transfer function. The low frequency gain of this section depends on the COMP to SW current gain (g_{mPOWER}), and the value of the load resistor (R_{LOAD}). The DC gain of the control-to-output is:

$$G_{CO} = g_{mPOWER} \times R_{LOAD} \quad (18)$$

The control-to-output transfer function has a pole (f_{P1}) formed by the output capacitance (C_{OUT}) and load resistance (R_{LOAD}) at:

$$f_{P1} = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT}} \quad (19)$$

The control-to-output transfer function also has a zero (f_{Z1}) formed by the output capacitance (C_{OUT}) and its associated ESR:

$$f_{Z1} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad (20)$$

For a design with very low-ESR type output capacitors (for example, ceramic or OSCON output capacitors), the ESR zero (f_{Z1}) is usually at a high frequency, so it can be ignored. On the other hand, if the ESR zero falls below or near the 0 dB crossover frequency of the system (such as with electrolytic output capacitors), then it should be cancelled by the pole formed by the CP capacitor and the RZ resistor (discussed and identified later as f_{P3}).

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A Bode plot of the control-to-output transfer function for figure 1 (V_{OUT} = 3.3 V, R_{LOAD} = 0.94 Ω) is shown in figure 15. The pole at f_{P1} can be seen at 5.4 kHz, while the ESR zero, f_{Z1}, occurs at a very high frequency, 1.5 MHz (this is typical for a design using ceramic output capacitors).

Next, look at the feedback resistor divider, (RFB1 and RFB2), the Error amplifier (g_m), and its compensation network RZ/CZ/CP. It greatly simplifies the transfer function derivation if RO >> RZ, and CZ >> CP. In most cases, RO > 2 MΩ, 1 kΩ < RZ < 50 kΩ, 220 pF < CZ < 47 nF, and CP <100 pF, so the following analysis should be very accurate. The low frequency gain of the control section (G_C) is formed by the feedback resistor divider and the Error amplifier. It can be calculated using equation 21, where V_{OUT} is the output voltage, V_{FB} is the reference voltage (0.8 V), g_m is the Error amplifier transconductance (750 µA / V), and R_O is the Error amplifier output impedance (A_{VOL} /g_m):

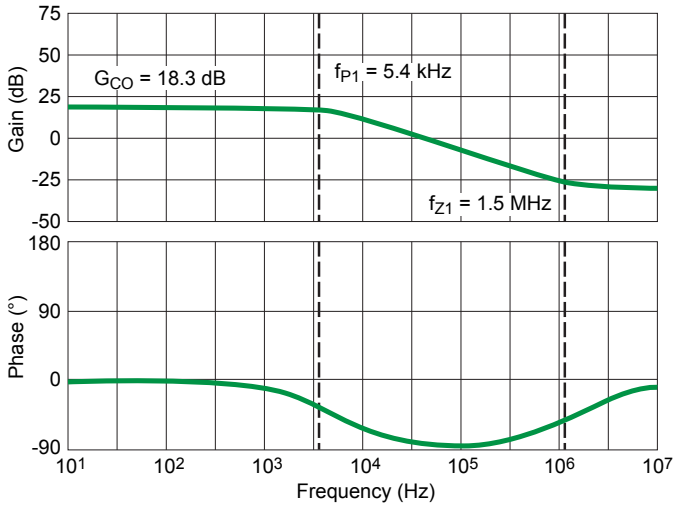

Figure 15. Control-to-output Bode plot for circuit in figure 1

$$G_C = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \times g_m \times R_O = \frac{V_{FB}}{V_{OUT}} \times g_m \times R_O = \frac{V_{FB}}{V_{OUT}} \times A_{VOL} \quad (21)$$

The transfer function of the compensated Error amplifier has a (very) low frequency pole (f_{P2}) dominated by the output Error amplifier output impedance (R_O) and the CZ compensation capacitor:

$$f_{P2} = \frac{1}{2\pi \times R_O \times C_Z} \quad (22)$$

The transfer function of the compensated Error amplifier also has a low frequency zero (f_{Z2}) dominated by the RZ resistor and the CZ capacitor:

$$f_{Z2} = \frac{1}{2\pi \times R_Z \times C_Z} \quad (23)$$

Lastly, the transfer function of the compensated Error amplifier has a higher frequency pole (f_{P3}) dominated by the RZ resistor and the CP capacitor:

$$f_{P3} = \frac{1}{2\pi \times R_Z \times C_P} \quad (24)$$

A Bode plot of the Error amplifier and its compensation network is shown in figure 16. f_{P2}, f_{P3}, and f_{Z2} are indicated on the gain (magnitude) plot. Notice that the zero (f_{Z2} at 7.3 kHz) has been placed so that it is in the vicinity of the pole at f_{P1} (5.4 kHz) previously shown in the control-to-output Bode plot, figure 15.

Finally, look at the combined Bode plot of both the control-to-output and the compensated Error amplifier in figure 17. Careful examination of this plot shows that the magnitude and phase of the entire system (red curve) are simply the sum of the Error amplifier response (blue curve, figure 16) and the control-to-output response (green curve, figure 15). As shown in figure 17, the bandwidth of this system is 142 kHz and the phase margin is approximately 90 degrees.

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A Generalized Tuning Procedure

1) Choose the system bandwidth, f_C, the frequency at which the magnitude of the gain will cross 0 dB. Recommended values for f_C based on the PWM switching frequency are: $f_{SW}/20 < f_C < f_{SW}/10$. A higher value of f_C will generally provide a better transient response, while a lower value of f_C will be easier to obtain higher gain and phase margins.

2) Calculate the RZ resistor value to set the required system bandwidth (f_C):

$$R_Z = f_C \times \frac{V_{OUT}}{V_{FB}} \times \frac{2 \times \pi \times C_{OUT}}{g_{mPOWER} \times g_m} \quad (25)$$

3) Determine the frequency of the pole (f_{P1}) formed by C_{OUT} and R_{LOAD} by using equation 19 (repeated here):

$$f_{P1} = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT}}$$

4) Calculate the CZ capacitor value by setting f_{Z2} at $1.5 \times f_{P1}$:

$$C_Z = \frac{1}{2 \times \pi \times R_Z \times 1.5 \times f_{P1}} \quad (26)$$

5) Calculate the frequency of the ESR zero (f_{Z1}) formed by the output capacitor(s) by using equation 20 (repeated here):

$$f_{Z1} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad (20)$$

5a) If f_{Z1} is at least 1 decade higher than the target crossover frequency (f_C) then f_{Z1} can be ignored. This is usually the case for a design using ceramic output capacitors. Use equation 24 to calculate the value of CP by setting f_{P3} to either $10 \times f_C$ or $f_{SW}/2$, whichever is higher.

5b) On the other hand, if f_{Z1} is near or below the target crossover frequency (f_C) then use equation 24 to calculate the value of CP by setting f_{P3} equal to f_{Z1}. This is usually the case for a design using high ESR electrolytic output capacitors.

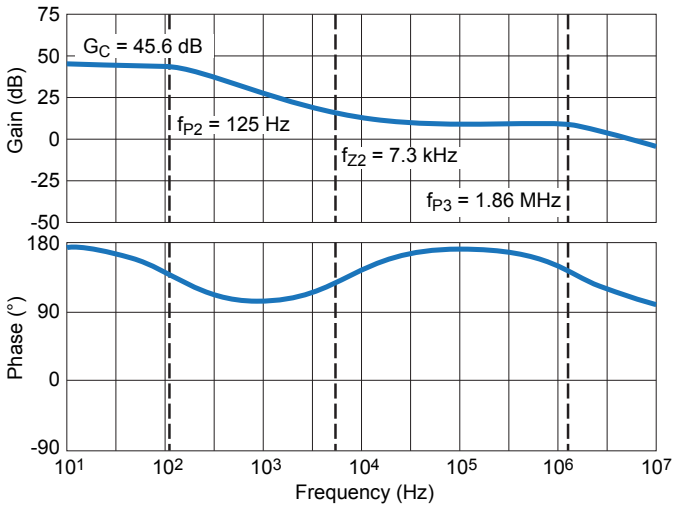

Figure 16. Compensated Error amplifier Bode plot

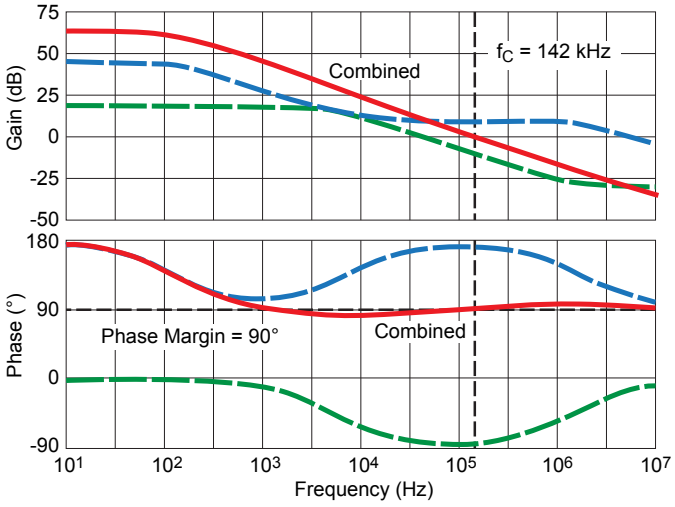

Figure 17. Bode plot for the complete system (combined = red curve)

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A Simple PSpice® Model for the A8583

Show in figure 18 is a very simple, first-order model for a current mode buck converter. This model allows a designer to easily modify the Error amplifier compensation, produce the Bode plot, and estimate the gain and phase margins. It should shorten the design time by allowing the designer to quickly examine the effects and trade-offs of modifying the system variables.

In the PSpice model, the transconductance Error amplifier is modelled by the GEA block with a gain of g_m. Its output impedance, R_O, is calculated as A_{VOL}/g_m (nominally 1.06 MΩ for the A8583). The compensation components of interest are Rz, Cz, and Cp shown at the COMP node. The PWM modulator and current control loop are simply modelled as the COMP to SW gain, g_{mPOWER}, documented in the electrical characteristics of this data sheet. R_{LOAD} is the load resistance and C_{OUT} is the output capacitance with its equivalent ESR.

The component labelled Lac (10 GH) is used to maintain a closed loop so PSpice can perform a DC bias point calculation, yet effectively "break" the loop for AC analysis. Also, the components labelled Cac (10 GF) and source V2 are used to inject a 1 V, AC signal for frequency response analysis. This model will predict the magnitude of the gain and 0 dB crossover frequency (f_C) fairly accurately, provided that $f_{SW} / 20 < f_C < f_{SW} / 10$. It will be optimistic when predicting the phase margin because the the PWM current control is approximated as a simple gain. The designer should try to obtain at least 60 degrees of phase margin with the model and then verify the bandwidth and gain/phase margins with a network analyzer on the actual circuit.

To produce the control-to-output Bode plot use:

dB(V(Vout)/V(VC)) and P(V(Vout)/V(VC))

To produce the Bode plot of the error amplifier, its compensation, and the feedback resistor divider use:

dB(V(COMP)/V(Vout)) and P(V(COMP)/V(Vout))

To produce the overall system Bode plot use:

dB(V(COMP)/V(VC)) and P(V(COMP)/V(VC))

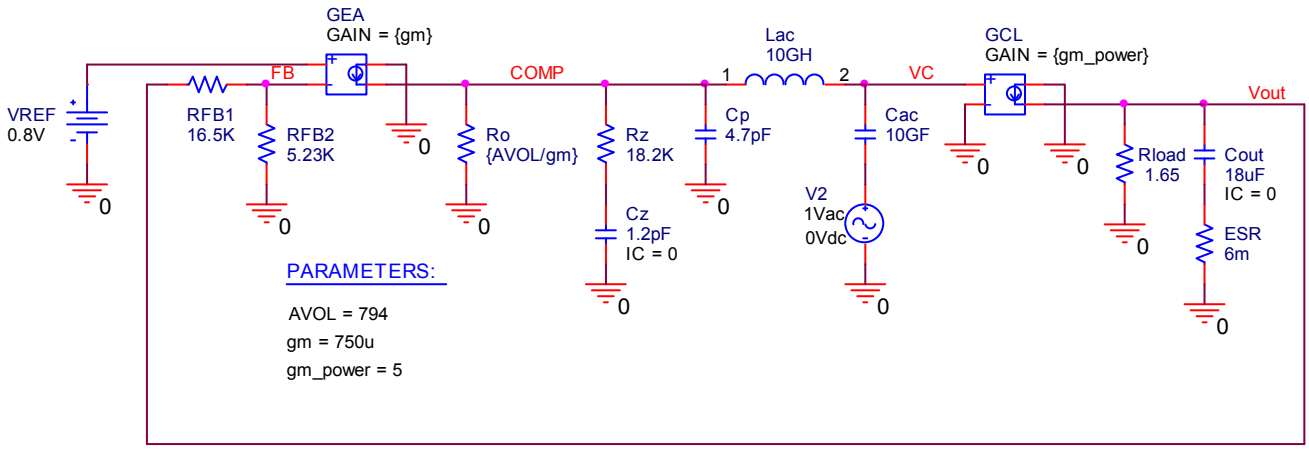

Figure 18. A simple PSpice model for the A8583 current mode buck converter

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Power Dissipation and Thermal Calculations

The power dissipated in the A8583 is the sum of the power dissipated from the V_{IN} supply current (P_{IN}), the power dissipated due to the switching of the internal power MOSFET (P_{SW}), the power dissipated by the internal gate driver (P_{DRIVER}), and the power dissipated due to the rms current being conducted by the internal MOSFET (P_{COND}).

The power dissipated from the V_{IN} supply current can be calculated using equation 27, where V_{IN} is the input voltage and I_Q is the input quiescent current drawn by the A8583 (nominally 3 mA):

$$P_{IN} = V_{IN} \times I_Q + Q_G \times f_{SW} \times (V_{IN} - V_{GS}) \quad (27)$$

The power dissipated by the internal high-side MOSFET while it is switching can be calculated using equation 28, where V_{IN} is the input voltage, I_{OUT} is the regulator output current, f_{SW} is the PWM switching frequency, and t_r and t_f are the rise and fall times measured at the SW node. The exact rise and fall times at the SW node will depend on the external components and PCB layout, so each design should be measured at full load. Approximate values for both t_r and t_f range from 5 ns to 10 ns.

$$P_{SW} = \frac{V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}}{2} \quad (28)$$

The power dissipated by the internal gate driver can be calculated using equation 29, where V_{GS} is the internal gate drive voltage (nominally 5 V), Q_G is the total gate charge to get to V_{GS} (typically about 4 nC), and f_{SW} is the switching frequency.

$$P_{DRIVER} = Q_G \times V_{GS} \times f_{SW} \quad (29)$$

The power dissipated by the internal high-side MOSFET while it is conducting can be calculated using equation 30, where I_{OUT} is the regulator output current, ΔI_L is the peak-to-peak inductor ripple current, $R_{DS(on)HS}$ is the drain-to-source on-resistance of the high-side MOSFET, and V_f is the forward voltage of the asynchronous diode, D1.

$$P_{COND} = I^2_{rms(FET)} \times R_{DS(on)HS}$$

$$= \left(\frac{V_{OUT} + V_f}{V_{IN} + V_f}\right) \times \left(I^2_{OUT} + \frac{\Delta I^2_L}{12}\right) \times R_{DS(on)HS} \quad (30)$$

The $R_{DS(on)}$ of the high-side MOSFET will have some part-to- part tolerance plus an increase from self-heating and elevated ambient temperatures. A conservative design should accommodate an $R_{DS(on)}$ with at least a 25% initial tolerance plus 0.4%/°C increase due to temperature.

Finally, the total power dissipated (P_{TOT}) is the sum of the previous four equations:

$$P_{TOT} = P_{IN} + P_{SW} + P_{DRIVER} + P_{COND} \quad (31)$$

The average junction temperature can be calculated with equation 32, where P_{TOT} is the total power dissipated, $R_{\theta JA}$ is the junction-to-ambient thermal resistance (34 °C/W on a 4-layer PCB), and T_A is the ambient temperature:

$$T_J = P_{TOT} \times R_{\theta JA} + T_A \quad (32)$$

The maximum junction temperature will be dependent on how efficiently heat can be transferred from the PCB to ambient air. The thermal pad on the bottom of the IC should be connected to a at least one ground plane using multiple vias for optimum performance. A small amount of airflow can improve the thermal performance considerably.

As with any regulator, there are limits to the amount of power that can be delivered and heat that can be dissipated before risking thermal shutdown. There are tradeoffs between ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, and airflow. Figures 19, 20, and 21 were derived using the equations shown in this section to estimate the safe operating areas for 12 V_{IN} at 2 MHz, 1 MHz, and 500 kHz for a 4-layer PCB with a thermal resistance of 40 °C/W, zero airflow, and no nearby heat sources (such as other power components). These curves should be consulted so reasonable expectations are set regarding ambient temperature, switching frequency, input/output voltage (duty cycle), and output current. Thermal performance is improved considerably if there is a low to medium amount of airflow.

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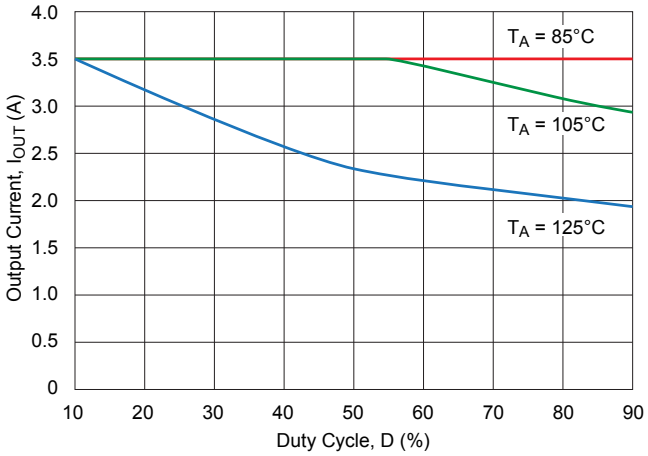

Figure 19. Output Current versus duty cycle; 12 V_{IN}, 2 MHz at various T_A

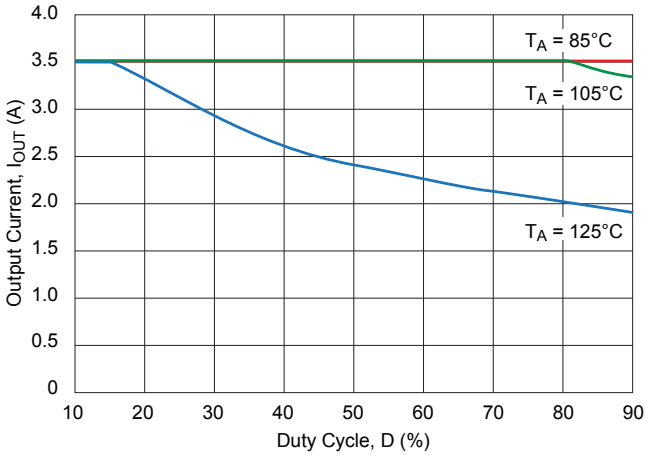

Figure 20. Output Current versus duty cycle; 12 V_{IN}, 1 MHz at various T_A

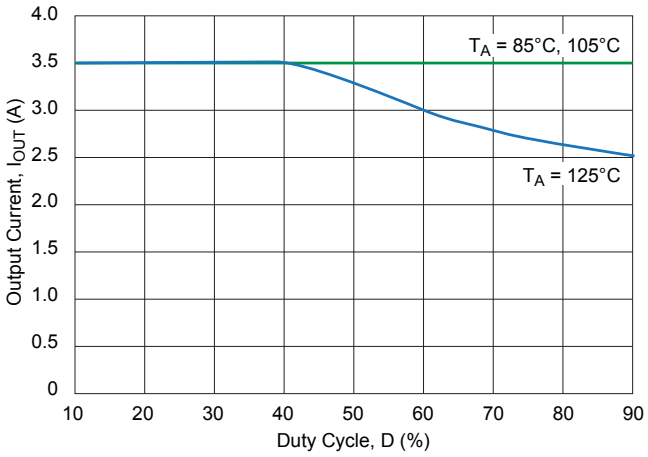

Figure 21. Output Current versus duty cycle; 12 V_{IN}, 500 kHz at various T_A

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PCB Component Placement and Routing

A good PCB layout is critical if the regulator is to provide clean, stable output voltages. Follow these guidelines to insure good PCB layout. Figure 22(a) shows an example component placment and routing. Figure 22(b) shows the three critical current loops that should be minimized and connected by relatively wide traces.

1) By far, the highest di/dt occurs at the instant the upper FET turns on and the asynchronous diode (D1) undergoes reverse recovery. The ceramic input capacitors (CIN) must deliver this high frequency current. Therefore, the loop from the ceramic input capacitors through the upper FET and asynchronous diode to ground should be minimized. Ideally this connection is made on both the top (component) layer and via the ground plane.

2) When the upper FET is on, current flows from the input supply/capacitors, through the upper FET, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces. Ideally this connection is made on both the top (component) layer and via the ground plane.

3) When the upper FET is off, “free-wheeling” current flows from ground through the asynchronous diode, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces. Ideally this connection is made on both the top (component) layer and via the ground plane.

4) The voltage on the SW node (pins 15 and 16) transitions from 0 V to V_{IN} very quickly and is the root cause of many noise issues. Its best to place the asynchronous diode and output inductor close to the A8583 to minimize the size of the SW polygon. Also, keep low level analog signals (like FB, FBX, COMP, and FSET) away from the SW polygon.

5) Place the feedback resistor divider (RFB1 and RFB2) very close to the FB pin (pin 9). Place the overvoltage sense resistor divider (RS1 and RS2) very close to the FBX pin (pin 10). Ground both resistor dividers as close as possible to the A8583 and to each other.

6) To have the highest output voltage accuracy, the regulation sense trace (from VOUT to RFB1) should be connected as close as possible to the load.

7) For optimal system reliability, its best to have two independent traces for regulation (FB, RFB1, RFB2) and overvoltage protection (FBX, RS1, RS2).

8) Place the frequency setting resistor (RFSET) as close as possible to the FSET pin (pin 8). Place a via to the GND plane as close as possible to the resistor solder pad.

9) Place the compensation components (RZ, CZ, and CP) as close as possible to the COMP pin (pin 11). Place vias to the GND plane as close as possible to these components.

10) Place the soft start capacitor (CSS) as close as possible to the SS pin (pin 4). Place a via to the GND plane as close as possible to this component.

11) Place the boot strap capacitor (CBOOT) near the BOOT pin (pin 14) and keep the routing to this capacitor as short as possible.

12) When routing the input and output ceramic capacitors (CIN, COUT), use multiple vias to GND and place the vias as close as possible to the component solder pads.

13) To minimize PCB losses and improve system efficiency, the input (VIN) and output (VOUT) traces should be as wide as possible and be duplicated on multiple layers, if possible.

14) To improve thermal performance, place multiple vias to the GND plane around the anode of the asynchronous diode.

15) The thermal pad under the A8583 must connect to the GND plane using multiple vias; more vias will insure the lowest operating temperature and highest efficiency. For even better thermal performance, the thermal via pattern can be extended beyond (above and below) the footprint of the A8583 as shown in figure 22(a).

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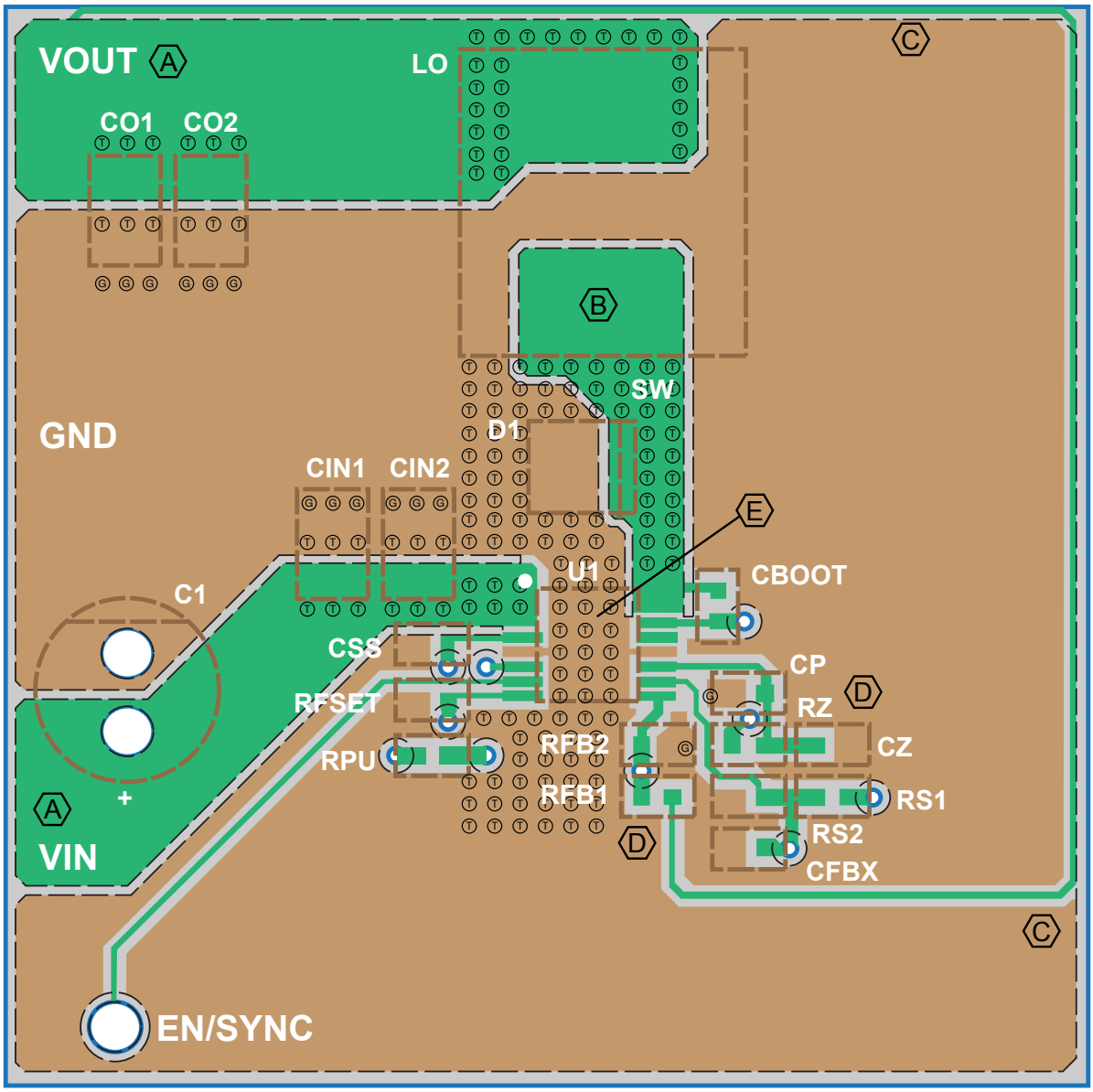

A. VOUT, VIN on multiple layers
B. SW polygon minimized
C. VOUT sense trace
D. Feedback and compensation components
E. Exposed pad under device soldered to GND

CO1, CO2 output capacitors
C1 input bulk capacitor
CIN1, CIN2 input ceramic capacitors
CBOOT boot capacitor
D1 Asynchronous diode

Figure 22(a). Example PCB component placement and routing

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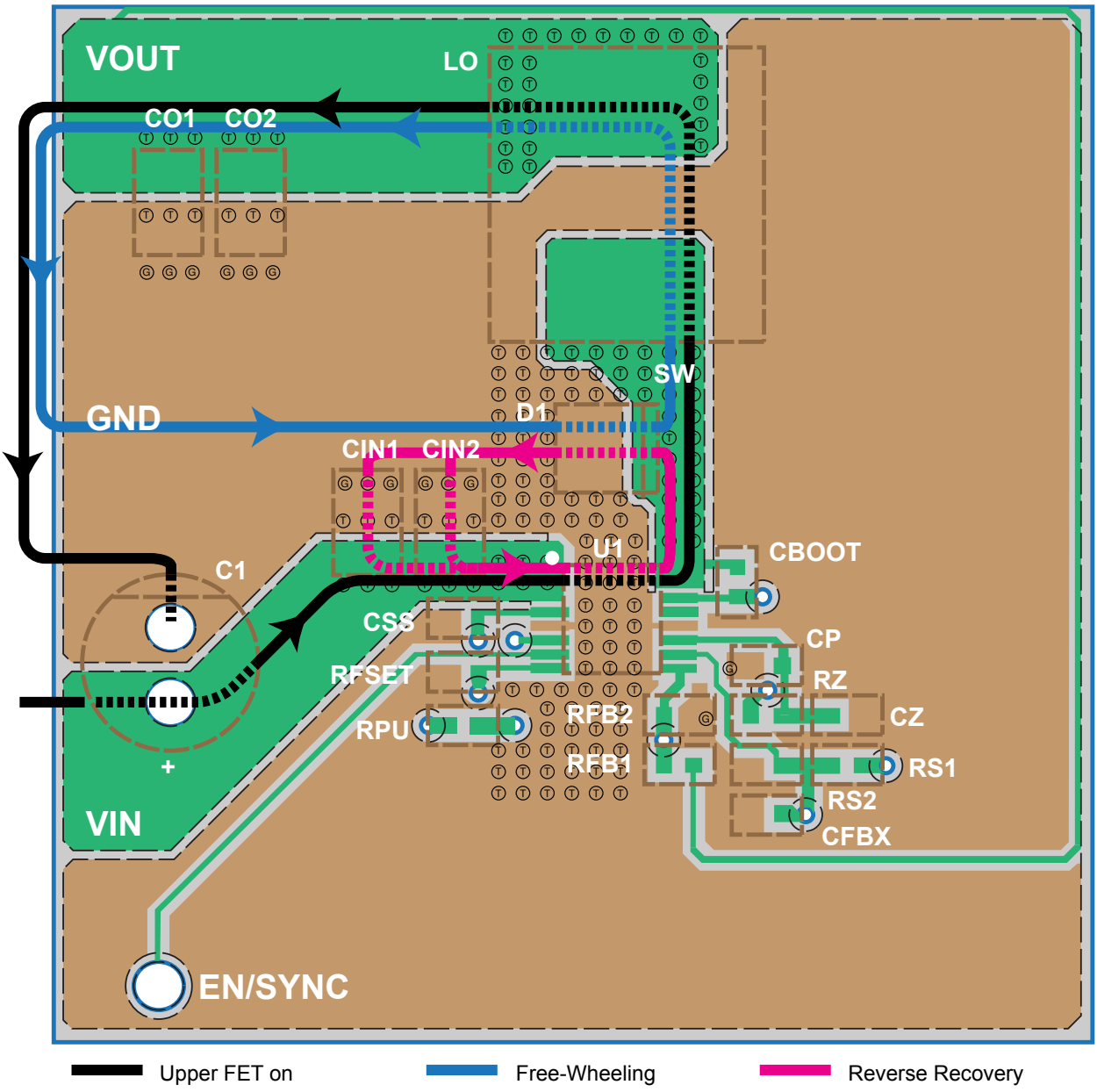

Figure 22(b). Current loops that should be minimized and connected by wide traces

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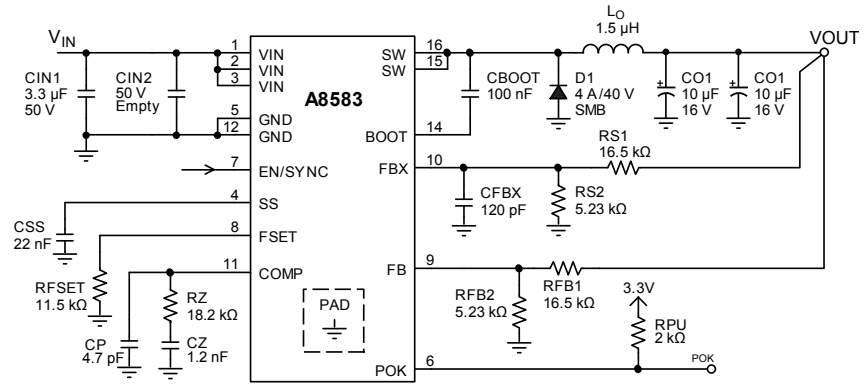
APPLICATION CIRCUIT AND PERFORMANCE



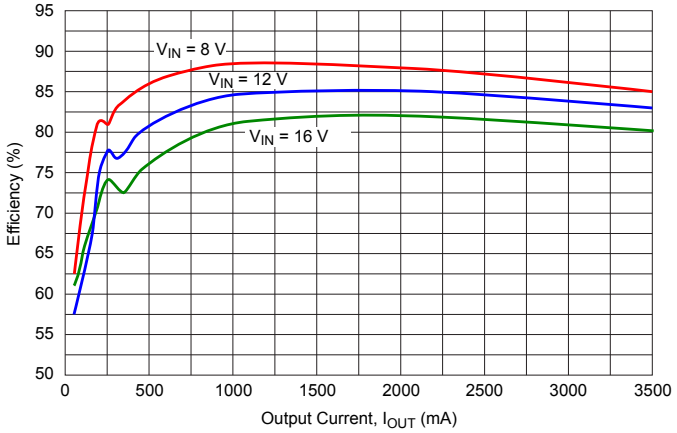
Recommended Components

L1: 1.5 µH, 14 mΩ, 18 A_{SAT}, 6.5 × 6.9 × 3.0 mm
Vishay: IHLP2020BZER1R5M01

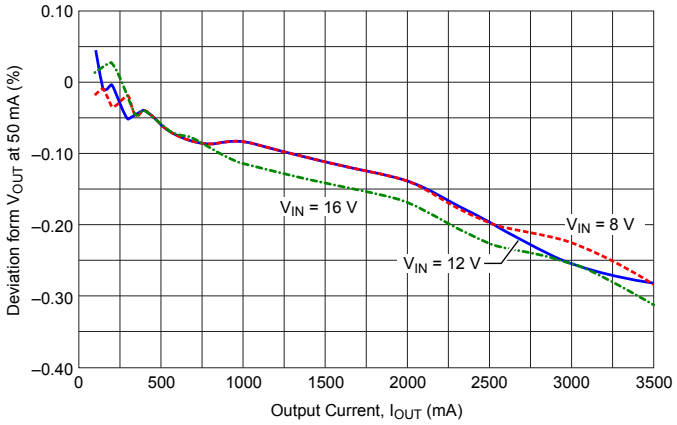
D1: Schottky, 4 A, 40 V, SMB
Vishay: SSB44-E3/52T

CO1, CO2: 10 µF, 10%, 16 V, X7R, 1206
Murata: GRM32DR71C106KA01L, or
TDK: C3216X7R1C106K

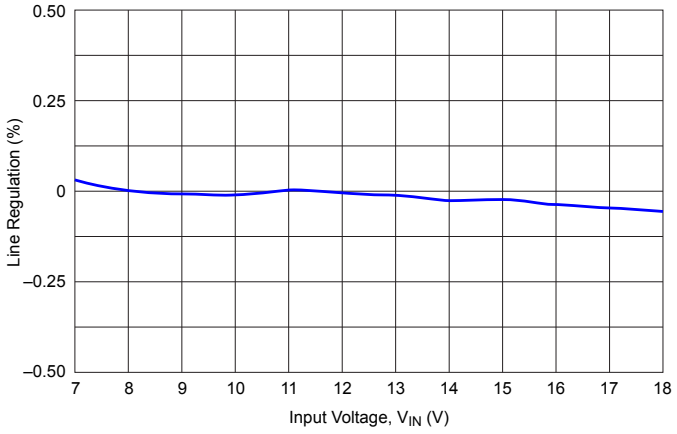
CIN1: 3.3 µF, 10% or 20%, 50 V, X5R or X7R, 1210
Murata: GRM55DR71H335MA01L, or
TDK: C3225X7R1H335M



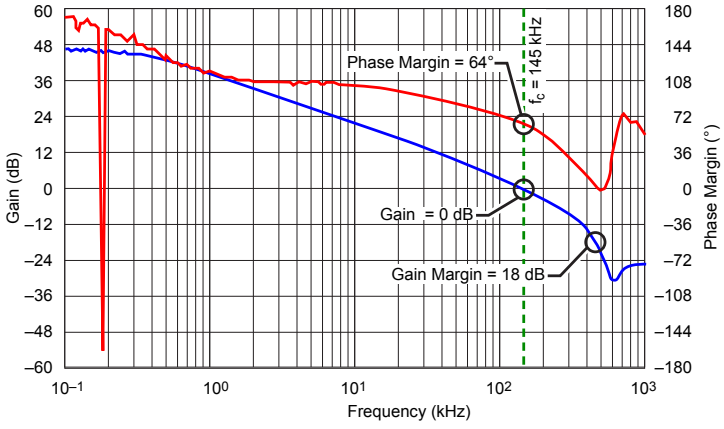
Efficiency versus Output Current, f_{SW} = 2 MHz, and V_{OUT} = 3.3 V



Load Regulation versus Output Current, f_{SW} = 2 MHz, and V_{OUT} = 3.3 V



Line Regulation versus Output Current, f_{SW} = 2 MHz, and V_{OUT} = 3.3 V



Bode Plot

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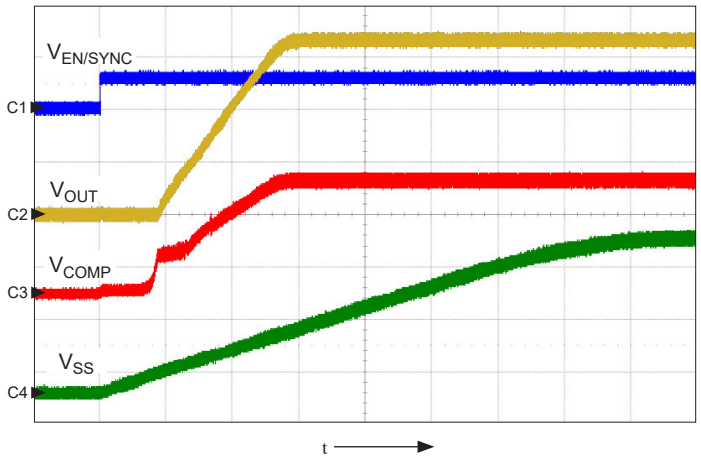
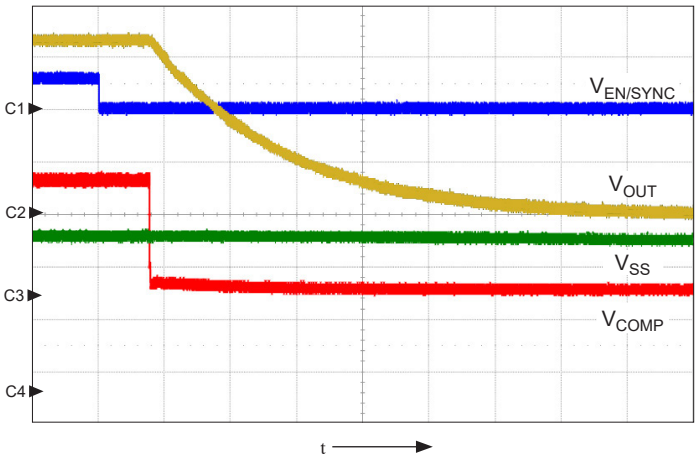
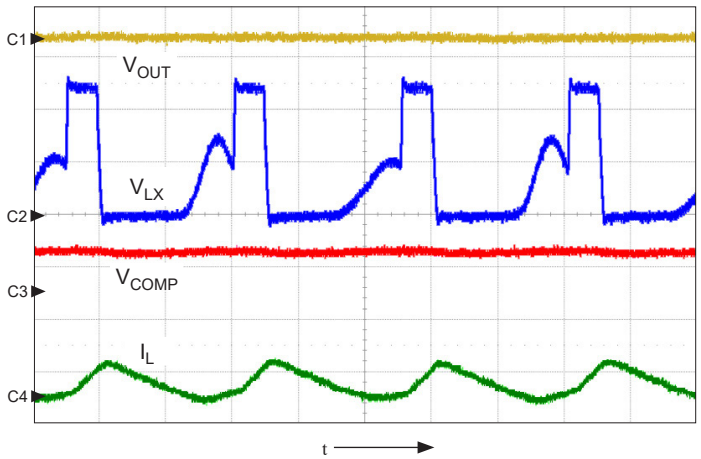


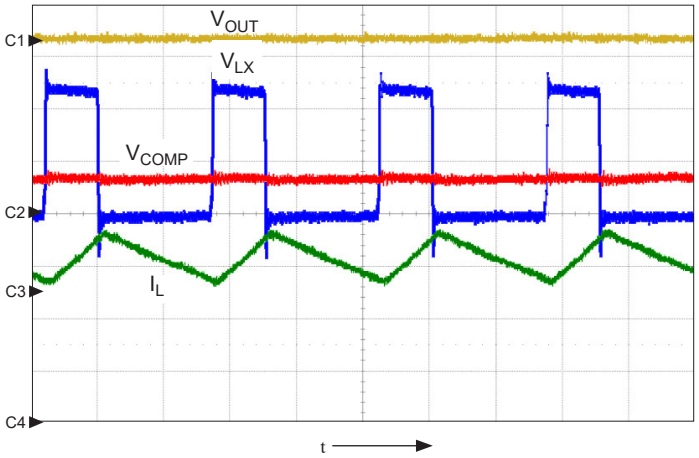
Startup at 3.3 A; shows $V_{EN/SYNC}$ (ch1, 10 V/div.), V_{OUT} (ch2, 1 V/div.), V_{COMP} (ch3, 500 mV/div.), V_{SS} (ch3, 1 V/div.), t = 500 µs/div.



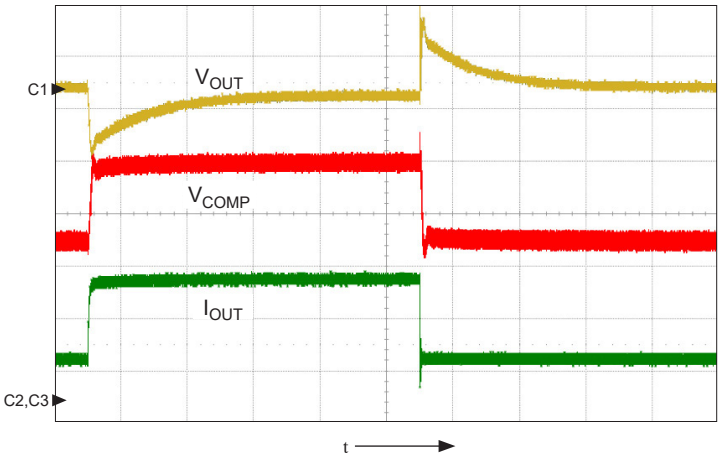
Shutdown at 3.3 A; shows $V_{EN/SYNC}$ (ch1, 10 V/div.), V_{OUT} (ch2, 1 V/div.), V_{COMP} (ch3, 500 mV/div.), V_{SS} (ch3, 1 V/div.), t = 500 µs/div.



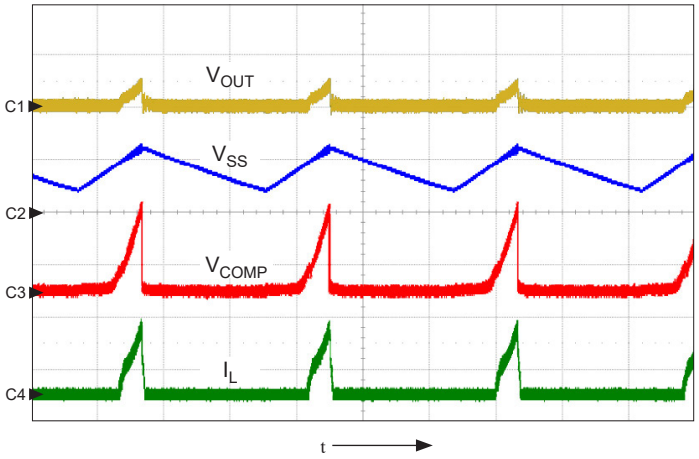
PWM at 220 mA Load; shows V_{OUT} (ch1, 1 V/div.), V_{LX} (ch2, 5 V/div.), V_{COMP} (ch3, 500 mV/div.), I_L (ch4, 1 A/div.), t = 200 ns/div.



PWM at 3.3 A Load; shows V_{OUT} (ch1, 1 V/div.), V_{LX} (ch2, 5 V/div.), V_{COMP} (ch3, 500 mV/div.), I_L (ch4, 1 A/div.), t = 200 ns/div.



0.7 to 2.3 A (1.6A) Transient Response; shows V_{OUT} (ch1, 50 mV/div.), V_{COMP} (ch2, 200 mV/div.), I_{OUT} (ch3, 1 A/div.), t = 50 µs/div.



Hiccup Mode Operation; shows V_{OUT} (ch1, 1 V/div.), V_{SS} (ch2, 500 mV/div.), V_{COMP} (ch3, 1 V/div.), I_L (ch4, 5 A/div.), t = 500 µs/div.

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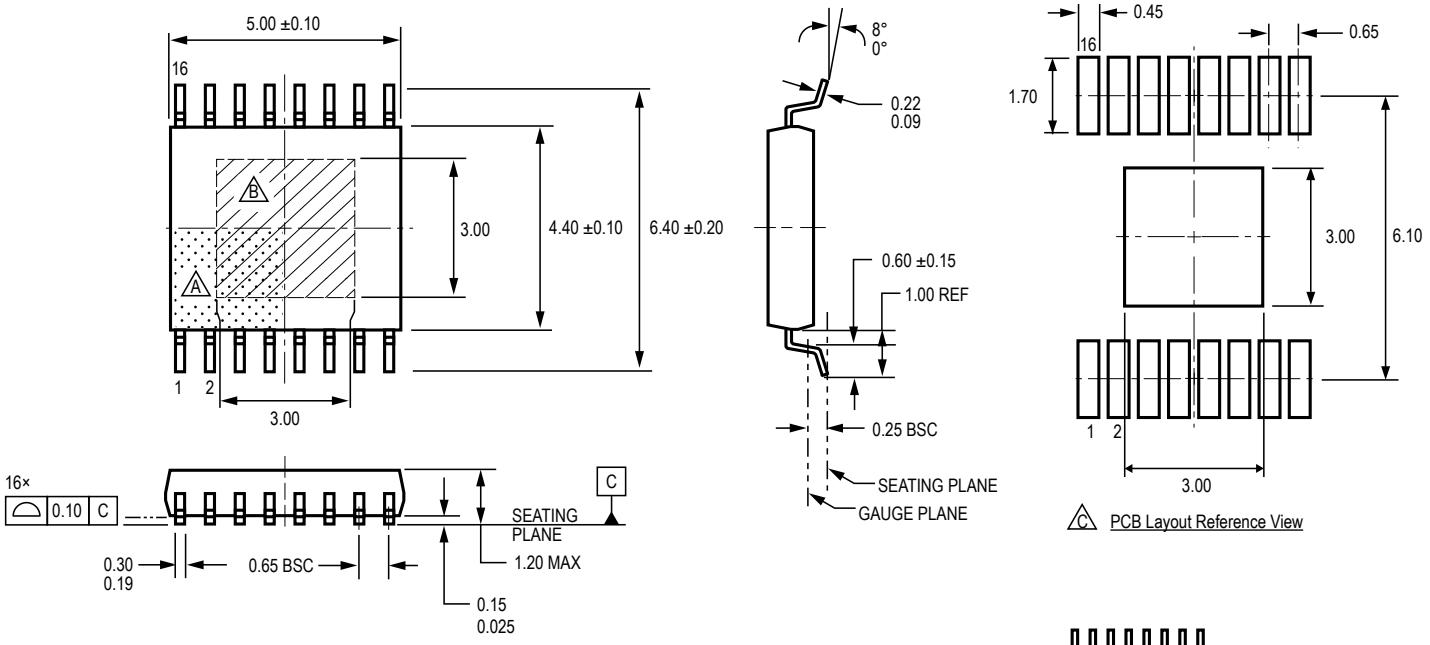
Package LP, 16-Pin TSSOP with Exposed Thermal Pad

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153 ABT; Allegro DWG-0000379, Rev. 3)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View

Lines 1, 2 = 7 characters
Line 3 = 5 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

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REVISION HISTORY

Number	Date	Description
16	October 10, 2013	Update T_{stg}
17	May 8, 2020	Minor editorial updates
18	May 9, 2022	Updated package drawing (page 32) and minor editorial updates

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