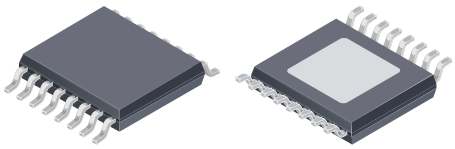
Wide Input Voltage, 2.4 MHz, 2.5 A, Asynchronous Buck Regulator with Low-IQ Standby, Sleep Mode, External Synchronization, and NPOR Output

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Withstands surge voltages up to 40 V
- Operates as low as 3.4 V_{IN} (typ) with V_{IN} decreasing
- Utilizes pulse frequency modulation (PFM) to draw only tens of microamperes from VIN while maintaining keep-alive VOUT
- PWM/PFMn mode control input pin
- Delivers up to 2.5 A of output current with integrated 110 mΩ high voltage MOSFET
- SLEEPn input pin commands ultra-low current shutdown mode
- Adjustable output voltage with ±1.0% accuracy from 0°C to 85°C, ±1.5% from –40°C to 150°C
- Programmable switching frequency: 250 kHz to 2.4 MHz
- Synchronization capability: applying a clock input to the PWM/PFMn input pin will increase the PWM frequency
- Active low, power-on reset (NPOR) open-drain output
- Maximized duty cycle for low dropout

Continued on the next page…

PACKAGE: 16-pin TSSOP with exposed thermal pad (suffix LP)



Not to scale

DESCRIPTION

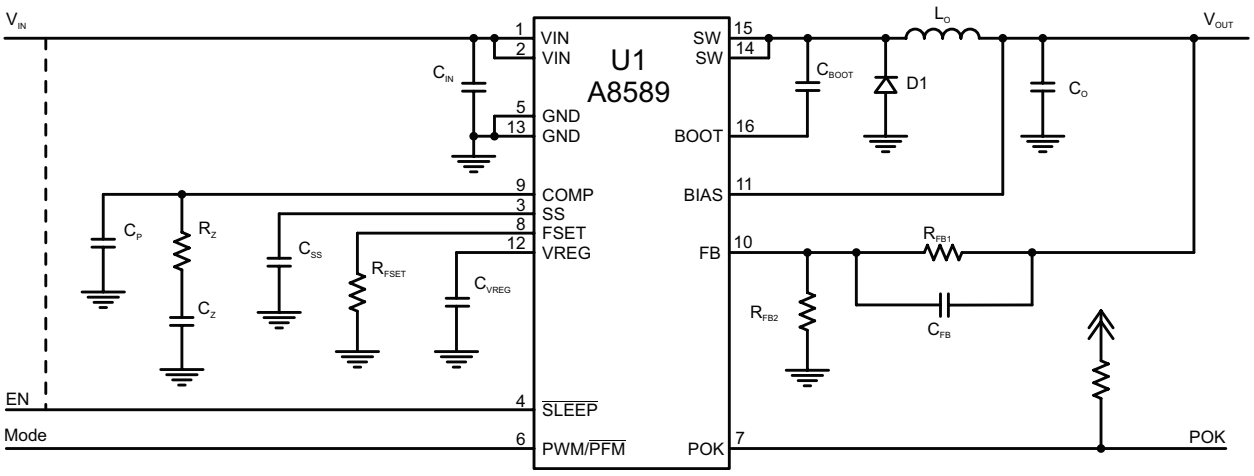
Designed to provide the power supply requirements of next generation car audio and infotainment systems, the A8589 provides all the control and protection circuitry to produce a high current regulator with ±1.0% output voltage accuracy. The A8589 employs pulse frequency modulation (PFM) to draw less than 50 µA from 12 V_{IN} while supplying 3.3 V/40 µA. After startup, the A8589 operates down to at least 3.6 V_{IN} (V_{IN} falling).

Features of the A8589 include a PWM/PFMn mode control input to enable PWM (logic high) or PFM (logic low). If the PWM/PFMn input is driven by an external clock signal higher than the base frequency (f_{OSC}) the PWM frequency synchronizes to the incoming clock frequency. The SLEEPn input pin commands an ultra-low current shutdown mode requiring less than 5 µA for internal circuitry and 10 µA (max) for MOSFET leakage at 16 V_{IN}, 85°C. The A8589 has external compensation to accommodate a wide range of frequencies and external components and provides a power-on reset (NPOR) signal validated by the output voltage.

Continued on the next page…

APPLICATIONS:

- Automotive:
  - □ Instrument clusters
  - □ Audio Systems
  - □ Navigation
  - □ HVAC
- Home Audio



Typical Application Diagram

FEATURES AND BENEFITS (continued)

- Pre-bias startup capable, VOUT will not cause a reset
- External compensation for maximum flexibility
- Stable with ceramic or electrolytic output capacitors
- Excellent set of protection features to satisfy the most demanding applications
- Overvoltage, pulse-by-pulse current limit, hiccup mode short circuit, and thermal protection
- Robust FMEA, with pin open/short and component faults
- Thermally enhanced, surface mount package

DESCRIPTION (continued)

Extensive protection features of the A8589 include pulse-by-pulse current limit, hiccup mode short circuit protection, open/short asynchronous diode protection, BOOT open/short voltage protection, VIN undervoltage lockout, V_{OUT} overvoltage protection and thermal shutdown.

The A8589 is supplied in a low profile 16-pin TSSOP package with exposed power pad (suffix LP). It is lead (Pb) free, with 100% matte-tin leadframe plating.

Selection Guide

Part Number	Operating Ambient Temperature Range T_A, (°C)	Packing
A8589KLPTR-T	–40 to 125	4000 pieces per 13-in. reel

Contact Allegro for additional packing options.

Table of Contents

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SPECIFICATIONS

Absolute Maximum Ratings*

Characteristic	Symbol	Notes	Rating	Unit
VIN, SLEEPn, SS Pin Voltage			–0.3 to 40	V
SW Pin Voltage	V_{SW}	Continuous (minimum limit is a function of temperature)	–0.3 to V_{IN} + 0.3	V
		t < 50 ns	–1.0 to V_{IN} + 3	V
BOOT Pin Voltage	V_{BOOT}	Continuous	V_{SW}–0.3 to V_{SW} + 5.5	V
		BOOT OV Fault Condition	V_{SW}–0.3 to V_{SW} + 7.0	V
BIAS Pin Voltage	V_{BIAS}	Continuous	–0.3 to 5.5	
		BIAS OV Fault Condition	–0.3 to 6	V
All Other Pins Voltage			–0.3 to 5.5	V
Operating Ambient Temperature	T_A	K temperature range	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

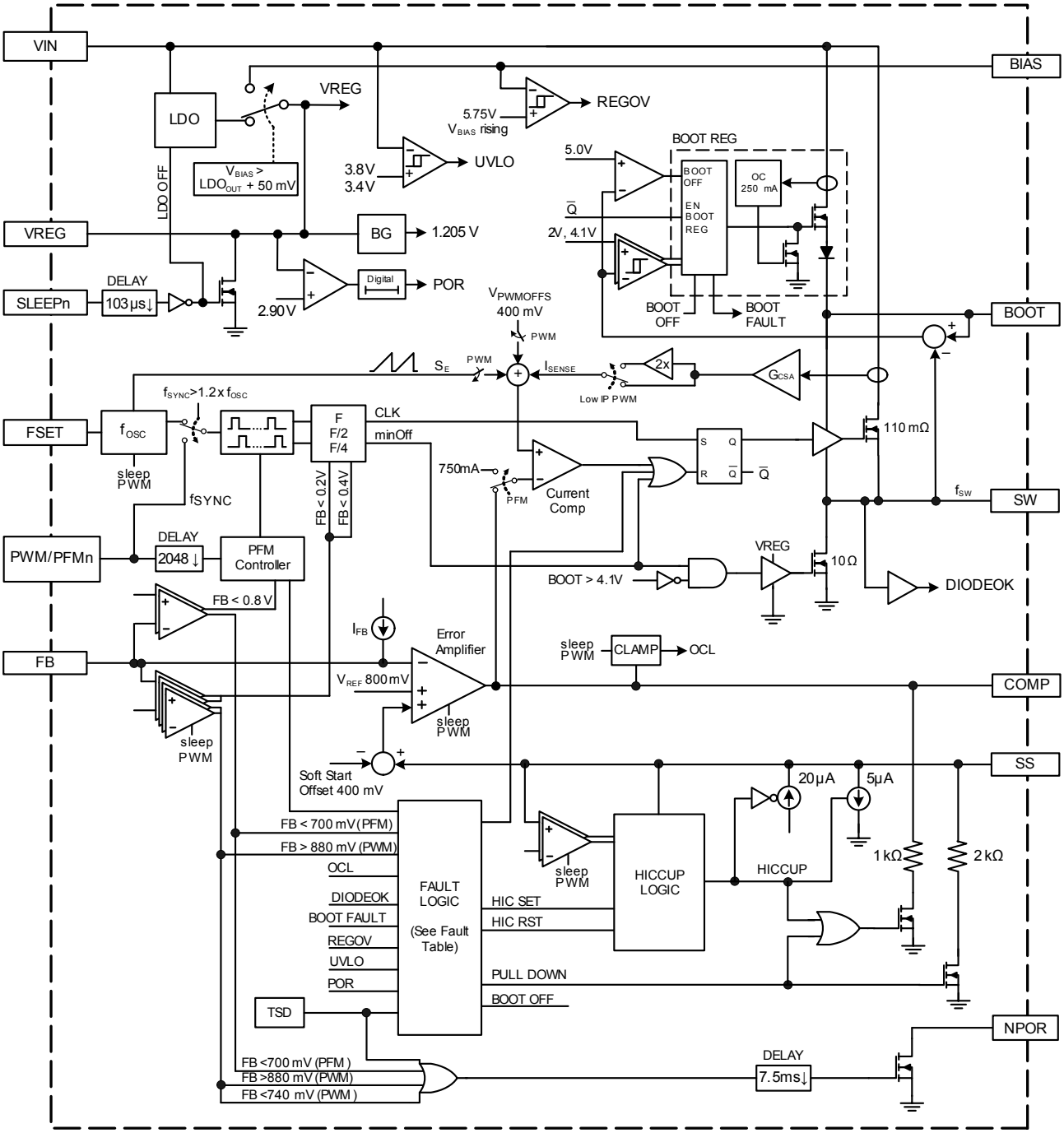
*Operation at levels beyond the ratings listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	34	°C/W

*Additional thermal information available on the Allegro website.

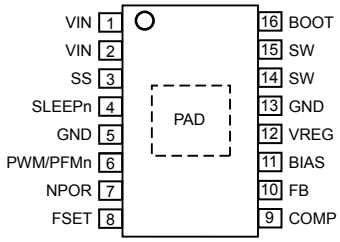
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



Functional Block Diagram

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Pinout Diagram and Terminal List



Package LP, 16-Pin TSSOP Pinout Diagram

Terminal List Table

Name	Number	Function
11	BIAS	Bias input, supplies internal circuitry.
16	BOOT	High-side gate drive boost input. This pin supplies the drive for the high-side N-channel MOSFET. Connect a 47 nF ceramic capacitor from BOOT to SW.
9	COMP	Output of the error amplifier and compensation node for the current mode control loop. Connect a series RC network from this pin to GND for loop compensation. See the Design and Component Selection section of this datasheet for further details.
10	FB	Feedback (negative) input to the error amplifier. Connect a resistor divider from the regulator output, VOUT, to this pin to program the output voltage.
8	FSET	Frequency setting pin. A resistor, R_{FSET}, from this pin to GND sets the base PWM switching frequency (f_{OSC}). See the Design and Component Selection section for information on determining the value of R_{FSET}.
5, 13	GND	Ground pins.
7	NPOR	Active low, power-on reset output signal. This pin is an open drain output that transitions from low to high impedance after the output has maintained regulation for $t_{D(NPOR)}$.
–	PAD	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 6 vias, directly in the pad land.
6	PWM/PFMn	Sets operating output mode (f_{SW}). Setting this pin low forces Low-IQ PFM mode (f_{SW} set by load). Setting this pin high forces PWM mode switching at the base frequency (f_{OSC}), set by R_{FSET}. Applying an external clock input to this pin forces synchronization of PWM to the clock input rate (f_{SYNC}), at a rate higher than f_{OSC}. SLEEPn low overrides this pin.
4	SLEEPn	Setting this pin low forces sleep mode (very low current shutdown mode: V_{OUT} = 0 V). This pin must be set high to enable the A8589. If the application does not require a sleep mode, then this pin can be tied directly to VIN. Do not float this pin.
3	SS	Soft start and hiccup pin. Connect a capacitor, C_{SS}, from this pin to GND to set soft start mode duration. The capacitor also determines the hiccup period during overcurrent.
14, 15	SW	The source of the high-side N-channel MOSFET. The external free-wheeling diode (D1) and output inductor (L_O) should be connected to this pin. Both D1 and L_O should be placed close to this pin and connected with relatively wide traces.
1, 2	VIN	Power input for the control circuits and the drain of the high-side N-channel MOSFET. Connect this pin to a power supply providing from 4.0 to 35 V. A high quality ceramic capacitor should be placed and grounded very close to this pin.
12	VREG	Internal voltage regulator bypass capacitor pin. Connect a 1 µF ceramic capacitor from this pin to ground and place it very close to the A8589.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: valid at 4.0 V ≤ V_{IN} ≤ 35 V, –40°C ≤ T_A = T_J ≤ 150°C; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Voltage						
Input Voltage Range[1]	V_{IN}		4.0	–	35	V
VIN UVLO Start	$V_{INUV(ON)}$	V_{IN} rising	3.6	3.8	4.0	V
VIN UVLO Stop	$V_{INUV(OFF)}$	V_{IN} falling	3.2	3.4	3.6	V
VIN UVLO Hysteresis	$V_{INUV(HYS)}$		–	400	–	mV
Input Supply Current						
Sleep Mode Input Supply Current[2,6]	$I_{IN(SLEEP)}$	V_{SLEEPn} ≤ 0.5 V, T_J = 85°C, V_{IN} =16 V	–	5	15	µA
		V_{SLEEPn} ≤ 0.5 V, T_J = 85°C, V_{IN} = 35 V	–	7	25	µA
PWM Mode Input Supply Current[2]	$I_{IN(PWM)}$	V_{BIAS} > 3.2 V, I_{OUT} = 0 mA	–	2.5	5.0	mA
Low-IQ PFM Input Supply Current[2,3]	$I_{LO\_IQ(0)}$	V_{IN} = 12 V, V_{OUT} = 3.3 V, $V_{PWMPFMn}$ ≤ 0.8 V, I_{OUT} = 40 µA, T_A =25°C, components selected per table 3	–	–	50	µA
	$I_{LO\_IQ(1)}$	V_{IN} = 12 V, V_{OUT} = 5.0 V, $V_{PWMPFMn}$ ≤ 0.8 V, I_{OUT} = 200 µA, T_A = 25°C, components selected per table 3	–	–	250	µA
	$I_{LO\_IQ(2)}$	V_{IN} = 12 V, V_{OUT} = 6.5 V, $V_{PWMPFMn}$ ≤ 0.8 V, I_{OUT} = 1 mA, T_A = 25°C, components selected per table 3	–	–	750	µA
Voltage Regulation						
Feedback Voltage Accuracy[4]	V_{FB}	0°C < T_J < 85°C, V_{IN} ≥ 4.1 V, V_{FB} = V_{COMP}	792	800	808	mV
		–40°C < T_J < 150°C, V_{IN} ≥ 4.1 V, V_{FB} = V_{COMP}	788	800	812	mV
Low-IQ PFM Mode Output Voltage Setting Range[1,3]	$V_{OUT(LO\_IQ)}$	3.0 V < V_{BIAS} < 5.5 V and I_{LO_IQ} specifications satisfied	3.3	–	6.5	V
PWM Output Voltage Setting Range[3]	V_{OUT}	V_{BIAS} = GND, PWM only, no PFM mode	0.8	–	10	V
Output Dropout Voltage[3]	$V_{OUT(SAT)}$	T_A = 85°C, DCR_{LO} ≤ 75 mΩ, V_{IN} = 3.6 V, I_{OUT} = 1 A, f_{SW} = 425 kHz	3.27	3.3	–	V
		T_A = 85°C, DCR_{LO} ≤ 75 mΩ, V_{IN} = 5.3 V, I_{OUT} = 1 A, f_{SW} = 425 kHz	4.95	5.0	–	V
		T_A = 85°C, DCR_{LO} ≤ 50 mΩ, V_{IN} = 3.75 V, I_{OUT} = 1 A, f_{SW} = 2 MHz	3.25	3.3	–	V
		T_A = 85°C, DCR_{LO} ≤ 50 mΩ, V_{IN} = 5.5 V, I_{OUT} = 1 A, f_{SW} = 2 MHz	4.89	5.0	–	V
Low-IQ PFM Mode Ripple Voltage[3]	$\Delta V_{OUT(LO\_IQ)}$	8 V < V_{IN} < 12 V, components selected per table 3	–	30	65	mV_{PP}
Low-IQ PFM Mode Peak Current Threshold	$I_{PEAK(LO\_IQ)}$	f_{SW} < 750 kHz	–	750	–	mA_{PEAK}
		f_{SW} > 750 kHz	–	850	–	mA_{PEAK}
Low-IQ PFM Mode DC Load Current[3]	$I_{OUT(LO\_IQ)}$	Maximum load to maintain $\Delta V_{OUT(LO\_IQ)}$, components selected per table 3	400	550	700	mA

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): valid at 4.0 V ≤ V_{IN} ≤ 35 V, –40°C ≤ T_A = T_J ≤ 150°C; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Error Amplifier						
Feedback Input Bias Current[2]	I_{FB}		–38	–	–16	nA
Open Loop Voltage Gain	A_{VOL}	V_{COMP} = 1.2 V	–	65	–	dB
Transconductance	g_m	400 mV < V_{FB}	550	750	950	µA/V
		0 V < V_{FB} < 400 mV	275	375	475	µA/V
Output Current	I_{EA}	V_{COMP} = 1.2 V	–	±75	–	µA
COMP Pull-Down Resistance	R_{COMP}	FAULT = 1 or HICCUP = 1	–	1	–	KΩ
Pulse Width Modulation (PWM)						
PWM Ramp Offset	PWM_{OFFS}	V_{COMP} level required for 0% duty cycle	–	400	–	mV
Minimum Controllable PWM On-Time	$t_{ON(MIN)PWM}$	12 V < V_{IN} < 16 V, I_{OUT} = 1 A, V_{BOOT} – V_{SW} = 4.5 V	–	95	135	ns
Minimum Switch Off-Time	$t_{OFF(MIN)PWM}$		–	95	130	ns
COMP to SW Current Gain	g_{mPOWER}		–	2.85	–	A/V
Slope Compensation[3]	S_E	f_{OSC} = 2.44 MHz	2.1	3.0	3.9	A/µs
		f_{OSC} = 1.00 MHz	0.60	0.91	1.2	A/µs
		f_{OSC} = 252 kHz	0.14	0.20	0.26	A/µs
MOSFET Parameters[1]						
High-Side MOSFET On-Resistance[5]	$R_{DS(on)HS}$	T_J =25°C, V_{BOOT} – V_{SW} = 4.5 V, I_{DS} = 0.4 A	–	110	125	mΩ
		T_J =150°C, V_{BOOT} – V_{SW} = 4.5 V, I_{DS} = 0.4 A	–	190	215	mΩ
High-Side MOSFET Leakage[2,6]	$I_{lkg(HS)}$	T_J < 85°C, V_{SLEEPn} ≤ 0.5 V, V_{SW} = 0 V, V_{IN} = 16 V	–	–	10	µA
		T_J ≤ 150°C, V_{SLEEPn} ≤ 0.5 V, V_{SW} = 0 V, V_{IN} = 16 V	–	60	150	µA
SW Node Slew Rate[3]	SR_{SW}	12 V < V_{IN} < 16 V	–	0.72	–	V/ns
Low-Side MOSFET On-Resistance[5]	$R_{DS(on)LS}$	T_J = 25°C, V_{IN} ≥ 6 V, I_{DS} = 0.1 A	–	–	10	Ω
PWM Switching Frequency						
Base PWM Switching Frequency	f_{OSC}	R_{FSET} = 8.06 kΩ, $V_{PWM/PFMn}$= high	2.20	2.44	2.70	MHz
		R_{FSET} = 23.7 kΩ, $V_{PWM/PFMn}$= high	0.90	1.00	1.10	MHz
		R_{FSET} = 102 kΩ, $V_{PWM/PFMn}$= high	–	252	–	kHz
PWM Synchronization Timing						
Synchronization Frequency Range	$f_{SYNC(MULT)}$		1.2 × f_{OSC}(typ)	–	1.5 × f_{OSC}(typ)	–
Synchronized PWM Frequency	$f_{SYNC(PWM)}$		–	–	2.9	MHz
Synchronization Input Duty Cycle	D_{SYNC}		–	–	80	%
Synchronization Input Pulse Width	t_{wSYNC}		200	–	–	ns
Synchronization Input Rise Time[3]	t_{rSYNC}		–	10	15	ns
Synchronization Input Fall Time[3]	t_{fSYNC}		–	10	15	ns

Continued on the next page…

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): valid at 4.0 V ≤ V_{IN} ≤ 35 V, –40°C ≤ T_A = T_J ≤ 150°C; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PWM/PFMn Pin Input Thresholds						
PWM/PFMn High Threshold	$V_{PWMPFMn(H)}$	3.0 V < V_{BIAS} < 3.6 V, $V_{PWMPFMn}$ rising	–	–	2.0	V
		4.5 V < V_{BIAS} < 5.5 V, $V_{PWMPFMn}$ rising	–	–	2.6	V
PWM/PFMn Low Threshold	$V_{PWMPFMn(L)}$	3.0 V < V_{BIAS} < 3.6 V, $V_{PWMPFMn}$ falling	0.8	–	–	V
		4.5 V < V_{BIAS} < 5.5 V, $V_{PWMPFMn}$ falling	1.2	–	–	V
PWM/PFMn Hysteresis	$V_{PWMPFMnhys}$	3.0 V < V_{BIAS} < 3.6 V, $V_{PWMPFM(H)}$ – $V_{PWMPFM(L)}$	–	200	–	mV
		4.5 V < V_{BIAS} < 5.5 V, $V_{PWMPFM(H)}$ – $V_{PWMPFM(L)}$	–	400	–	mV
PWM/PFMn Input Resistance	$R_{PWMPFMn}$		120	200	280	kΩ
Low-IQ PFM Transition Delay	$t_{D(LO\_IQ)}$	PWM/PFMn = low, V_{SS} > HIC/PFM_{EN}, NPOR = high	–	2048	–	counts
PFM Mode Timing						
Constant PFM Off-Time	$t_{OFF(PFM)}$	f_{OSC} < 1.5 MHz	–	435	–	ns
		f_{OSC} > 1.5 MHz	–	275	–	ns
Maximum PFM On-Time	$t_{ON(PFM)MAX}$		–	4.1	–	µs
SLEEPn Pin Input Thresholds						
SLEEPn High Threshold	$V_{SLEEP(H)}$	V_{SLEEPn} rising	–	1.3	2.1	V
SLEEPn Low Threshold	$V_{SLEEP(L)}$	V_{SLEEPn} falling	0.5	1.2	–	V
SLEEPn Delay	$t_{D(SLEEP)}$	V_{SLEEPn} transitioning low	55	103	150	µs
SLEEPn Input Bias Current	$I_{SLEEPBIAS}$	V_{SLEEPn} = 5 V	–	500	–	nA
VREG Pin Output						
VREG Output Voltage	V_{VREG}	V_{BIAS} = 0 V	–	3.05	–	V
BIAS Pin Input						
BIAS Input Voltage Range	V_{BIAS}		3.2	–	5.5	V
BOOT Regulator						
BOOT Voltage Enable Threshold	$V_{BOOT(EN)}$	V_{BOOT} rising	1.7	2.0	2.2	V
BOOT Voltage Enable Hysteresis	$V_{BOOT(HYS)}$		–	200	–	mV
BOOT Voltage Low-Side Switch Disable Threshold	$V_{BOOTLS(DIS)}$	V_{BOOT} rising	–	4.1	–	V
Soft Start Pin						
FAULT, HICCUP Reset Voltage	V_{SSRST}	V_{SS} falling due to $R_{SS(FLT)}$	–	200	275	mV
Hiccup OCP (and Low IQ PFM Counter Enable) Threshold	HIC/PFM_{EN}	V_{SS} rising	–	2.3	–	V
Maximum Charge Voltage	$V_{SS(MAX)}$		–	V_{VREG}	–	–
Startup (Source) Current	I_{SSSU}	HICCUP = FAULT = 0	–30	–20	–10	µA
Hiccup (Sink) Current	I_{SSHIC}	HICCUP = 1	2.4	5	10	µA
Pull-Down Resistance	$R_{SS(FLT)}$	FAULT = 1 or V_{SLEEPn} = low	–	2	–	kΩ

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): valid at 4.0 V ≤ V_{IN} ≤ 35 V, –40°C ≤ T_A = T_J ≤ 150°C; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Soft Start Pin (continued)						
Soft Start Frequency Foldback	$f_{SW(SS)}$	0 V < V_{FB} < 200 mV	–	f_{OSC} / 4	–	–
		200 mV < V_{FB} < 400 mV	–	f_{OSC} / 2	–	–
		400 mV < V_{FB}	–	f_{OSC}	–	–
Soft Start Delay Time[3]	$t_{D(SS)}$	C_{SS} = 22 nF	–	440	–	µs
Soft Start Output Ramp Time[3]	t_{SS}	C_{SS} = 22 nF	–	880	–	µs
Hiccup Modes						
Hiccup, OCP Count	OCP_{LIM}	V_{SS} > 2.3 V and OCL = 1	–	120	–	counts
Hiccup, BOOT Undervoltage (Shorted) Count	$BOOT_{UV}$		–	120	–	counts
Hiccup, BOOT Overvoltage (Open) Count	$BOOT_{OV}$		–	7	–	counts
Overcurrent Protection (OCP)						
PWM Pulse-by-Pulse Limit	$I_{LIM(TONMIN)}$	t_{ON} = $t_{ON(MIN)PWM}$	3.6	4.1	4.6	A
	$I_{LIM(TONMAX)}$	t_{ON} = (1 / f_{SW}) – $t_{OFF(MIN)PWM}$, no PWM synchronization	2.3	3.1	3.9	A
Output Voltage Protection (OVP)						
VOUT Overvoltage PWM Threshold	$V_{OUT(OV)PWM}$	V_{FB} rising, PWM mode	860	880	902	mV
VOUT Overvoltage Hysteresis	$V_{OUT(OV)HYS}$	V_{FB} falling, relative to $V_{OUT(OV)PWM}$	–	–10	–	mV
VOUT Undervoltage PWM Threshold	$V_{OUT(UV)PWM}$	V_{FB} falling, PWM mode	715	740	765	mV
VOUT Undervoltage Hysteresis	$V_{OUT(UV)HYS}$	V_{FB} rising, relative to $V_{OUT(UV)PWM}$	–	10	–	mV
VOUT Undervoltage PFM Threshold	$V_{OUT(UV)PFM}$	V_{FB} falling, Low-IQ PFM mode	665	700	735	mV
Power-On Reset (NPOR) Output						
NPOR Rising Delay	$t_{D(NPOR)}$	V_{FB} rising only	5	7.5	10	ms
NPOR Low Output Voltage	$V_{NPOR(L)}$	I_{NPOR} = 5 mA	–	185	400	mV
NPOR Leakage Current[2]	$I_{NPOR(LKG)}$	V_{NPOR} = 5.5 V	–1	–	1	µA
Thermal Protection						
Thermal Shutdown Rising Threshold[3]	T_{SD}	PWM stops immediately and COMP and SS are pulled low	155	170	185	°C
Thermal Shutdown Hysteresis[3]	T_{SDHYS}		–	20	–	°C

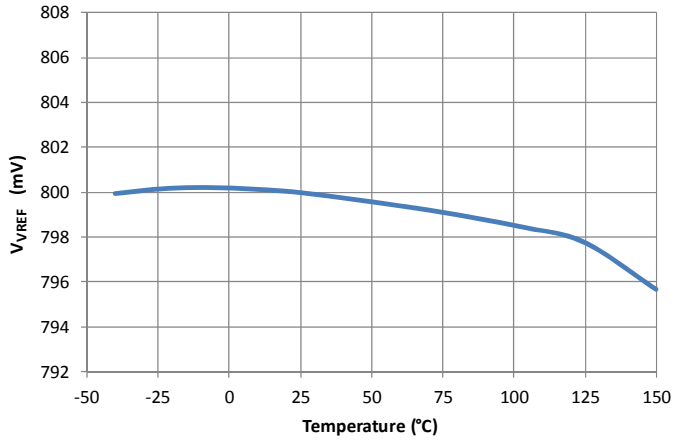
[1] Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[2] Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[3] Ensured by design and characterization, not production tested.
[4] Performance at the 0°C and 85°C ranges ensured by design and characterization, not production tested.
[5] Performance at 25°C ensured by design and characterization, not production tested.
[6] Performance at 85°C ensured by design and characterization, not production tested.

ALLEGRO microsystems

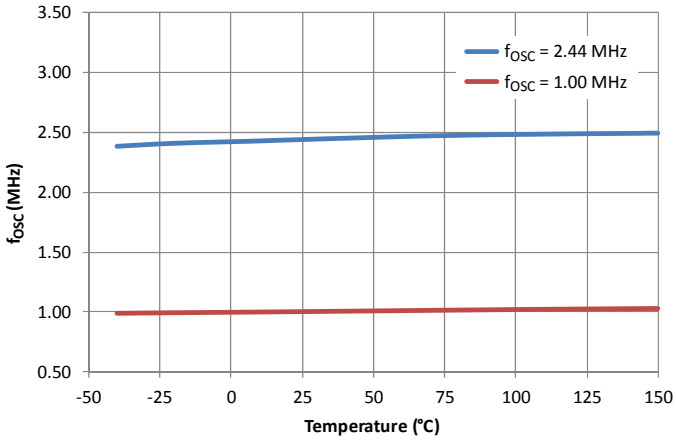
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

CHARACTERISTIC PERFORMANCE

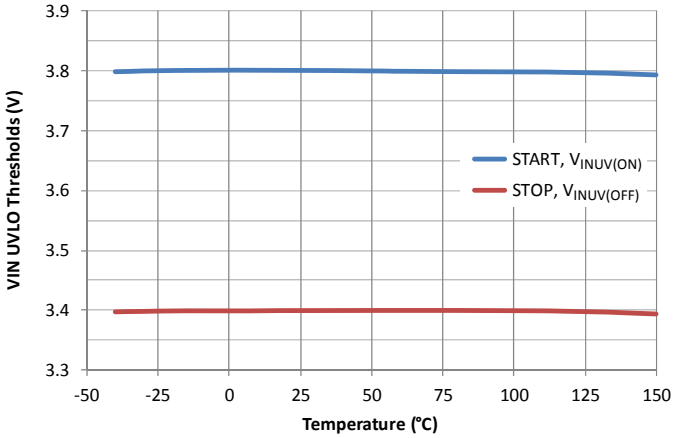
Reference Voltage versus Temperature



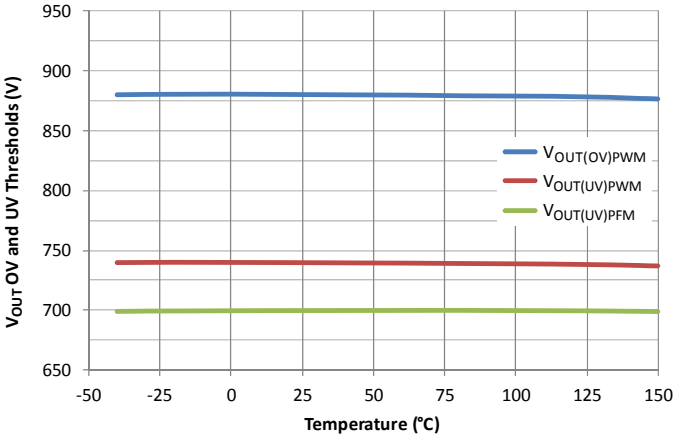
Switching Frequency versus Temperature



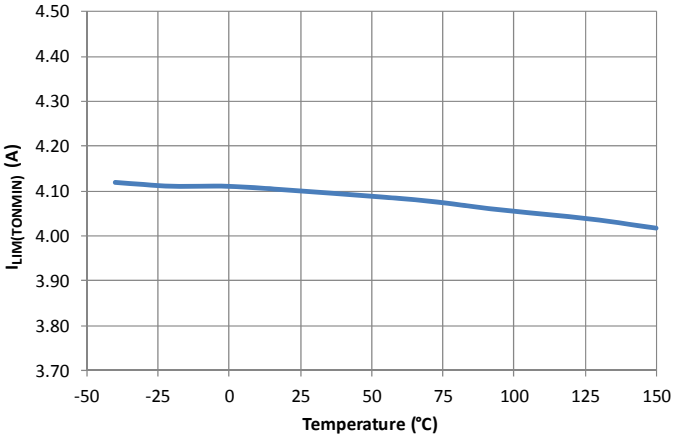
VIN UVLO Start and Stop Thresholds versus Temperature



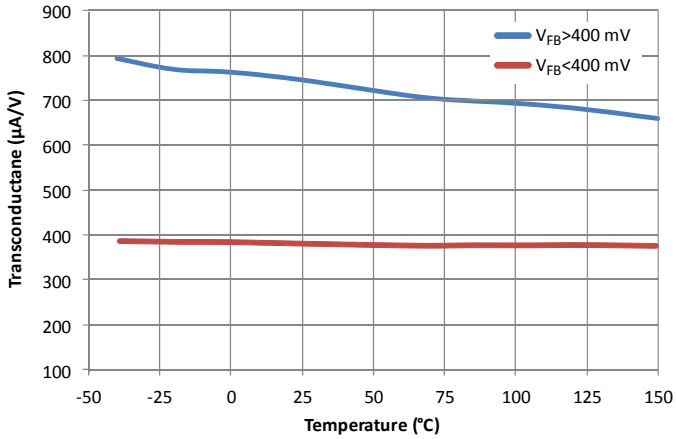
V_{OUT} Overvoltage and Undervoltage Thresholds versus Temperature



Pulse-by-Pulse Current Limit at $t_{ON(MIN)PWM}$ ($I_{LIM(TONMIN)}$) versus Temperature

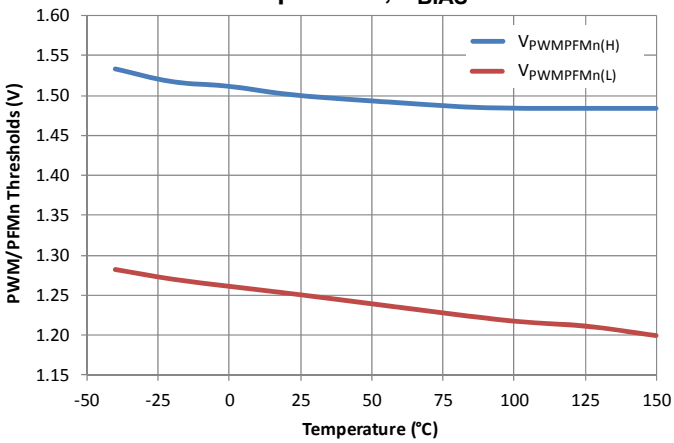


Error Amplifier Transconductance versus Temperature

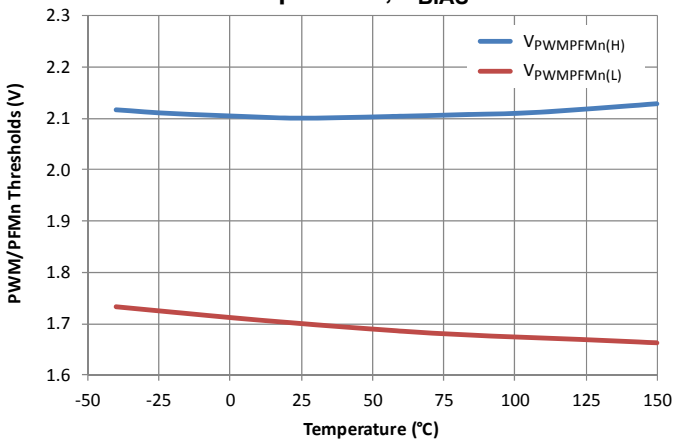


Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

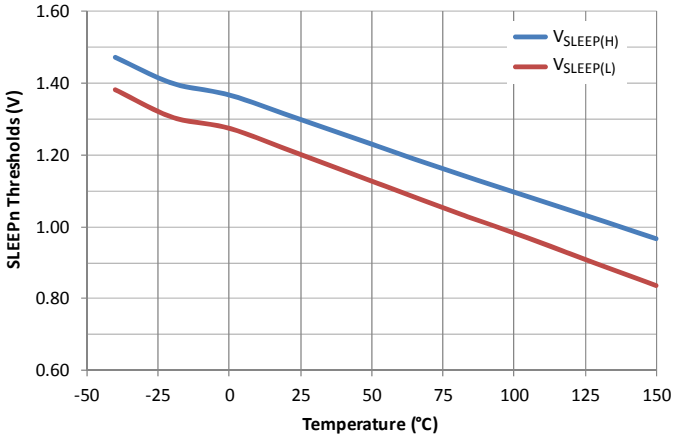
PWM/PFMn High and Low Voltage Thresholds versus Temperature, V_{BIAS} = 3.3 V



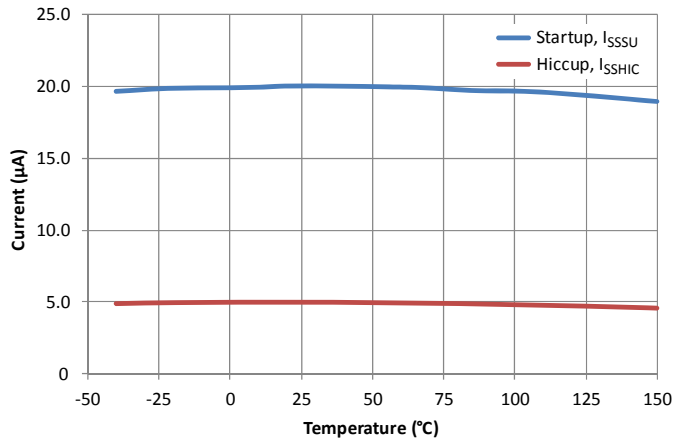
PWM/PFMn High and Low Voltage Thresholds versus Temperature, V_{BIAS} = 5.0 V



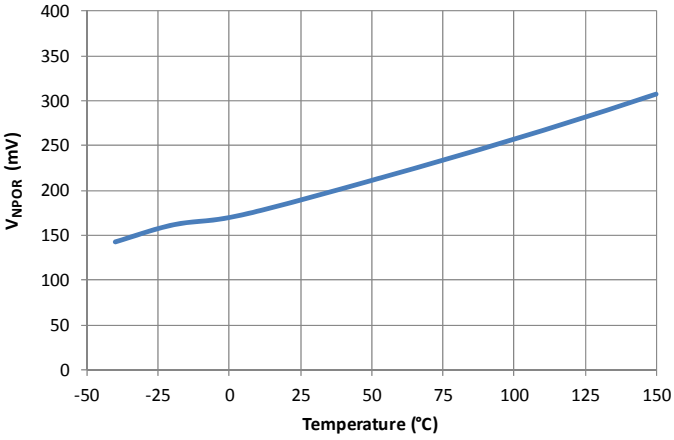
SLEEPn High and Low Voltage Thresholds versus Temperature



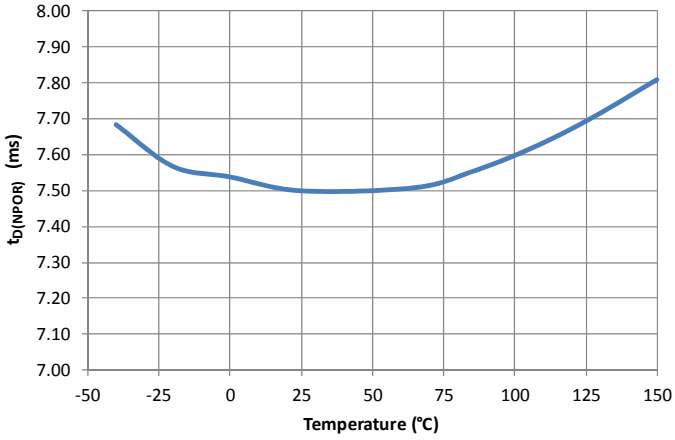
SS Start and Hiccup Currents versus Temperature



NPOR Low Output Voltage at 5 mA versus Temperature



NPOR Time Delay versus Temperature



ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

Overview

The A8589 is an asynchronous, current mode, buck regulator that incorporates all the control and protection circuitry necessary to provide the power supply requirements of car audio and infotainment systems.

The A8589 has three modes of operation. First, the A8589 can deliver up to 2.5 A in pulse width modulation (PWM) mode. Second, in Low-IQ pulse frequency modulation (PFM) mode, the A8589 will draw only tens of microamperes from V_{IN} while maintaining V_{OUT} (at no load). Under most conditions, Low-IQ PFM mode is typically capable of supporting up to 550 mA. Third, with the SLEEPn pin low, the A8589 will enter an ultra-low current shutdown (sleep) mode where V_{OUT} = 0 V and the total current drawn from V_{IN} will typically be less than 10 µA.

The PWM/PFMn input pin is used to select either PWM or Low-IQ PFM mode. In PFM mode the A8589 is able to supply a relatively high amount of current (typically 550 mA). This allows enough current for a microcontroller or DSP to fully power-up. After power-up, to obtain the full current capability of the A8589, the microcontroller or DSP must change the PWM/PFMn input from a logic low to a logic high to force PWM mode. This will provide full current to the remainder of the system.

The A8589 was designed to support up to 2.5 A. However, the exact amount of current it will supply, before possible thermal shutdown, depends heavily on: duty cycle, ambient temperature, airflow, PCB layout, and PCB construction. Figure 1 shows calculated current ratings versus ambient temperature for V_{IN} = 12 V, and V_{OUT} = 3.3 V and 5.0 V, at both f_{SW} = 425 kHz and f_{SW} = 2 MHz. This analysis assumed a 4-layer PCB constructed according to the JEDEC standard (yielding a thermal resistance of 34°C/W), with no nearby heat sources, and no airflow.

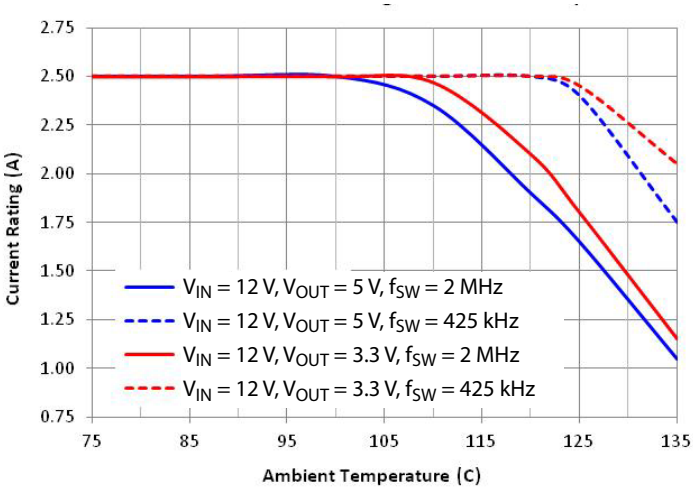


Figure 1: A8589 Typical Current Derating

Reference Voltage

The A8589 incorporates an internal reference that allows output voltages (V_{OUT}) as low as 0.8 V. The accuracy of the internal reference is ±1.0% from 0°C to 85°C and ±1.5% from −40°C to 150°C. The output voltage is programmed by connecting a resistor divider from VOUT to the FB pin of the A8589, as shown in the Typical Applications schematics.

PWM Switching Frequency

The PWM switching frequency of the A8589 is adjustable from 250 kHz to 2.4 MHz and has an accuracy of about ±10% across the operating temperature range.

During startup, the PWM switching frequency changes from 25% to 50% and finally to 100% of f_{OSC}, as V_{OUT} rises from 0 V to the regulation voltage. The startup switching frequency is discussed in more detail in the section describing soft start, below.

If the regulator output is shorted to ground, $V_{FB} \approx 0$ V, the PWM frequency will be 25% of f_{OSC}. In this case, the extra low switching frequency allows extra off-time between SW pulses. The extra off-time allows the output inductor current to decay back to 0 A before the next SW pulse occurs. This prevents the inductor current from climbing to a value that could damage the A8589 or the output inductor.

SLEEPn Input

The A8589 has a SLEEPn logic level input pin. To get the A8589 to operate, the SLEEPn pin must be a logic high (>2.1 V). The SLEEPn pin is rated to 40 V, allowing the SLEEPn pin to be connected directly to VIN if there is no suitable logic signal available to wake up the A8589.

When SLEEPn transitions low, the A8589 waits approximately 103 µs before shutting down. This delay provides plenty of filtering to prevent the A8589 from prematurely entering sleep mode because of any small glitch coupling onto the PCB trace or SLEEPn pin.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PWM/PFMn Input and PWM Synchronization

The PWM/PFMn pin provides two major functions. It is a control input that sets the operating mode, and also an optional clock input for setting PWM frequency.

If PWM/PFMn is a logic high, the A8589 operates in PWM mode. If PWM/PFMn is a logic low, the A8589 operates in Low-IQ PFM (keep alive) mode. When PWM/PFMn transitions from logic high to logic low, the A8589 checks for V_{SS} >2.3 V and NPOR at logic high. If these two conditions are satisfied, then the A8589 will wait 2048 internal clock cycles and then enter Low-IQ PFM mode. This delay provides plenty of filtering to prevent the regulator from prematurely entering PFM mode because of any small glitch coupling onto the PCB trace or PWM/PFMn pin.

Also, note that the SLEEPn pin must be a logic high or the PWM/PFMn input has no effect. The interaction between the SLEEPn pin and PWM/PFMn pin is summarized in Table 1.

If an external clock is applied to the PWM/PFMn pin, the A8589 synchronizes its PWM frequency to the external clock. The external clock may be used to increase the A8589 base PWM frequency (f_{OSC}) set by R_{FSET}. Synchronization operates from $1.2 \times f_{OSC}$(typ) to $1.5 \times f_{OSC}$(typ). The external clock pulses must satisfy the pulse width, duty cycle, and rise/fall time requirements shown in the Electrical Characteristics table in this datasheet.

Table 1: A8589 Modes of Operation

Pin Inputs		Operating Mode		
SLEEPn	**PWM/PFMn**	**Name**	**Description**	
Low	Don't care	Sleep	V_{OUT} = 0 V	
High	High	PWM	$f_{SW} = f_{OSC}$	V_{OUT} = OK and $I_{OUT} \le$ 2.5 A
High			f_{SW} = PWM/PFMn clock in	
High		Enter Low-IQ PFM after 2048 cycles, if V_{SS} > 2.3 V (typ) and NPOR = high		
High	Low	Low-IQ PFM	f_{SW} is VOUT dependent	V_{OUT} = OK and $I_{OUT} \le$ 550 mA (typ)
High	Low	Low-IP PWM	Fault, I_{LIM} at 50%	

BIAS Input Functionality, Ratings, and Connections

When the A8589 is powering up, it operates from an internal LDO regulator, directly from VIN. However, V_{IN} can be a relatively high voltage and an LDO is very inefficient and generates extra heat. To improve efficiency, especially in Low-IQ PFM mode, a BIAS pin is utilized. For most applications, the BIAS pin should be connected directly to the output of the regulator, V_{OUT}. When V_{OUT} rises to an adequate level (approximately 3.1 V), the A8589 will shut down the inefficient LDO and begin running its control circuitry directly from the output of the regulator. This makes the A8589 much more efficient and cooler.

The BIAS pin is designed to operate in the range from 3.2 to 5.5 V. If the output of the regulator is in this range, then V_{OUT} should be routed directly to the BIAS pin. However, if the output of the regulator is above 5.6 V, then a very small LDO, capable of at least 5 mA, must be used to reduce the voltage to either 3.3 V or 5.0 V before routing it to the BIAS pin. Operating with an external LDO will reduce the efficiency in Low-IQ PFM mode.

The BIAS pin may be driven by an external power supply. For startup, there are no sequencing requirements between VIN and BIAS. However, for shutdown, VIN should be removed before BIAS. If BIAS is removed before VIN it will cause the A8589 to reset. The reset will cause the A8589 to terminate PWM switching and V_{OUT} will decay. Also, NPOR, V_{SS}, and V_{COMP} will be pulled low. Ideally, the SLEEPn pin should be used to set the mode of the A8589 before VIN and/or BIAS are turned on or off.

If the BIAS pin is grounded, the A8589 will simply operate continuously from VIN. However, during PFM mode, the input current will increase, and the PFM efficiency will be significantly reduced.

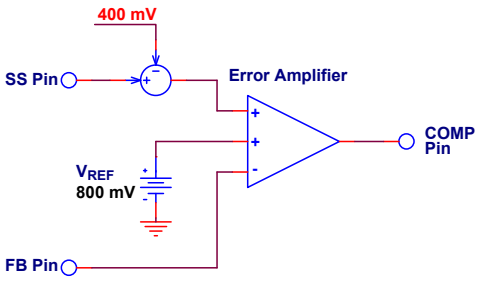


Figure 2: The A8589 Error Amplifier

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Transconductance Error Amplifier

The transconductance error amplifier primary function is to control the regulator output voltage. The error amplifier is shown in Figure 2. Here, it is shown as a three-terminal input device with two positive and one negative input. The negative input is simply connected to the FB pin and is used to sense the feedback voltage for regulation. The two positive inputs are used for soft start and steady-state regulation. The error amplifier performs an analog OR selection between its two positive inputs. The error amplifier regulates to either the soft start pin voltage (minus 400 mV) or the A8589 internal reference, V_{REF}, whichever is lower.

To stabilize the regulator, a series RC compensation network (RZ and CZ) must be connected from the error amplifier output (the COMP pin) to GND, as shown in the Typical Applications schematics. In most instances an additional, relatively low value, capacitor (CP) should be connected in parallel with the RZ-CZ components to reduce the loop gain at very high frequencies. However, if the CP capacitor is too large, the phase margin of the regulator may be reduced. Calculating RZ, CZ, and CP is covered in detail in the Component Selection section of this datasheet.

If a fault occurs or the regulator is disabled (SLEEPn = low), the COMP pin is pulled to GND via approximately 1 kΩ and PWM switching is inhibited.

Slope Compensation

The A8589 incorporates internal slope compensation (S_E) to allow PWM duty cycles above 50% for a wide range of input/output voltages and inductor values. The slope compensation signal is added to the sum of the current sense amplifier output and the PWM ramp offset. As shown in the Electrical Characteristics table, the amount of slope compensation scales with the base switching frequency set by R_{FSET} (f_{OSC}). The amount of slope compensation does not change when the regulator is synchronized to an external clock.

The value of the output inductor should be chosen such that S_E is from 0.5× to 1× the falling slope of the inductor current (S_F).

Current Sense Amplifier

The A8589 incorporates a high-bandwidth current sense amplifier to monitor the current in the high-side MOSFET. This current signal is used by both the PWM and PFM control circuitry to regulate the peak current. The current signal is also used by the protection circuitry to prevent damage to the A8589.

Power MOSFETs

The A8589 includes a 40 V, 110 mΩ high-side N-channel MOSFET, capable of delivering at least 2.5 A. The A8589 also includes a 10 Ω, low-side MOSFET to help ensure the BOOT capacitor is always charged. The typical $R_{DS(on)}$ increase versus temperature is shown in Figure 3.

BOOT Regulator

The A8589 contains a regulator to charge the boot capacitor. The voltage across the BOOT capacitor is typically 5.0 V. If the BOOT capacitor is missing, the A8589 detects a boot overvoltage. Similarly, if the BOOT capacitor is shorted the A8589 detects a boot undervoltage. Also, the BOOT regulator has a current limit to protect itself during a short circuit condition. The details of how each type of boot fault is handled by the A8589 are shown in Figures 13 and 14 and summarized in Table 2.

Pulse Width Modulation (PWM) Mode

The A8589 utilizes fixed-frequency, peak current mode control to provide excellent load and line regulation, fast transient response, and ease of compensation. A high-speed comparator and control logic, capable of typical pulse widths of 95 ns, are included in the A8589. The inverting input of the PWM comparator is connected to the output of the error amplifier. The non-inverting input is connected to the sum of the current sense signal, the slope compensation, and a DC offset voltage ($V_{PWMOFFS}$, 400 mV (typ)).

At the beginning of each PWM cycle, the CLK signal sets the PWM flip flop and the high-side MOSFET is turned on. When the summation of the DC offset, slope compensation, and current sense signal rises above the error amplifier voltage, the PWM flip flop is reset and the high-side MOSFET is turned off.

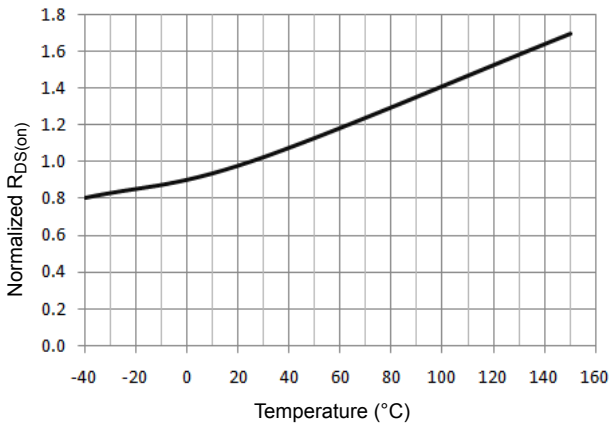


Figure 3: Typical MOSFET $R_{DS(on)}$ versus Temperature

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The PWM flip flop is reset-dominant, so the error amplifier may override the CLK signal in certain situations. For example, at very light loads or extremely high input voltages the error amplifier reduces (temporarily) output voltage below the 400 mV DC offset and the PWM flip flop will ignore one or more of the incoming CLK pulses. The high-side MOSFET will not turn on, and the regulator will skip pulses to maintain output voltage regulation.

In PWM mode, all A8589 fault detection circuits are active. See Figure 13 for a timing diagram showing how faults are handled when in PWM mode. Also, the Protection Features section of this datasheet provides a detailed description of each fault and Table 2 presents a summary.

Maximized Duty Cycle Control

Most fixed frequency PWM controllers have limited maximum duty cycle. This is due to the off-time required to keep the BOOT capacitor charged in order to drive the high-side N-channel MOSFET. This limitation becomes significant in high-frequency, low-input voltage regulators. It may cause the output voltage to drop out of regulation during stop/start profiles in automotive designs.

The A8589 employs a technique that helps extend the maximum duty cycle during drop out conditions. Without this technique the typical maximum duty cycle would be 74% at 2 MHz switching frequency. Utilizing the extended duty cycle technique, the A8589 can achieve typical drop out duty cycles of greater than 95% in 2 MHz designs.

Low-IQ Pulse Frequency Modulation (PFM) Mode

The A8589 enters Low-IQ PFM mode after 2048 internal clock cycles, if SLEEPn is high, V_{SS} > HIC/PFM_{EN} (2.3 V (typ)), and NPOR is high. In Low-IQ PFM mode, the regulator operates with a switching frequency, f_{SW}, that depends on the load condition.

In Low-IQ PFM mode, a comparator monitors the voltage at the FB pin. If V_{FB} is above about 800 mV, the A8589 remains in coast mode and draws extremely low current from the input supply.

If the voltage at the FB pin drops below about 800 mV, the A8589 will fully power-up, delay approximately 2.5 µs while it wakes up, and then turn on the high-side MOSFET. V_{OUT} will rise at a rate dependent on the input voltage, inductor value, output capacitance, and load. The high-side MOSFET will be turned off when either:

- current in the high-side MOSFET reaches $I_{PEAK(LO\_IQ)}$, or
- the high-side MOSFET has been on for $t_{ON(PFM)MAX}$.

After the high-side MOSFET is turned off, the A8589 will again

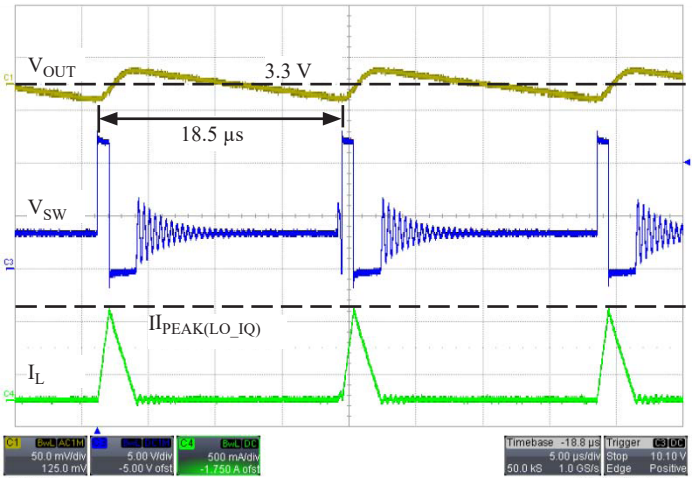


Figure 4. Low-IQ PFM Mode Operation at V_{IN} = 12 V, V_{OUT} = 3.3 V, and I_{OUT} = 66 mA. SW turns on only once every 18.5 µs to regulate V_{OUT}

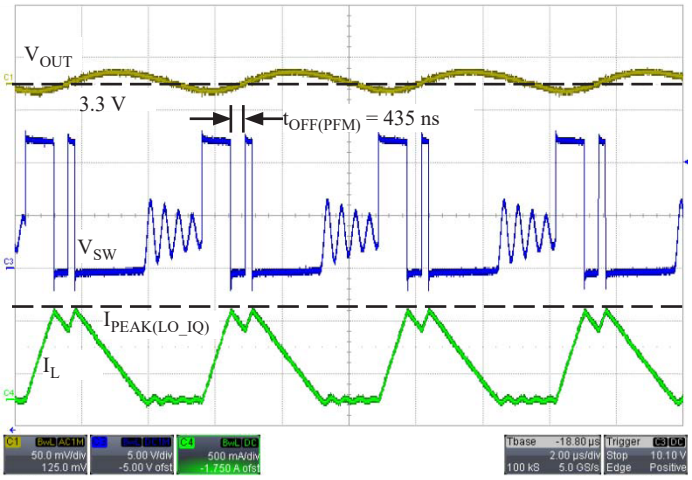
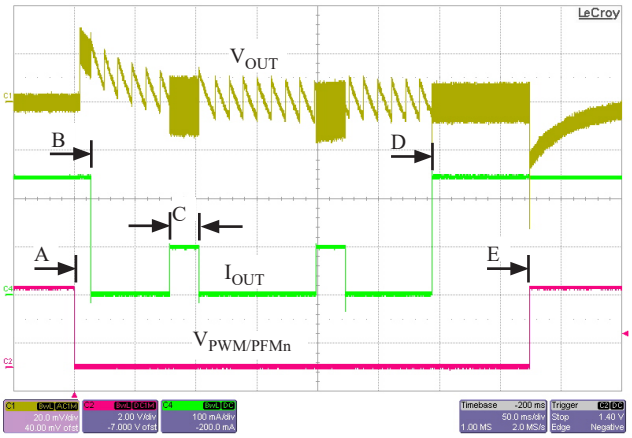
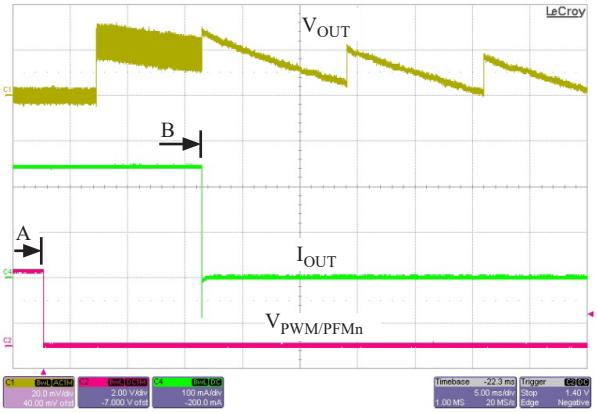


Figure 5. Low-IQ PFM Mode Operation at V_{IN} = 12 V, V_{OUT} = 3.3 V, and I_{OUT} = 330 mA. SW turns on only twice every 5 µs to regulate V_{OUT}

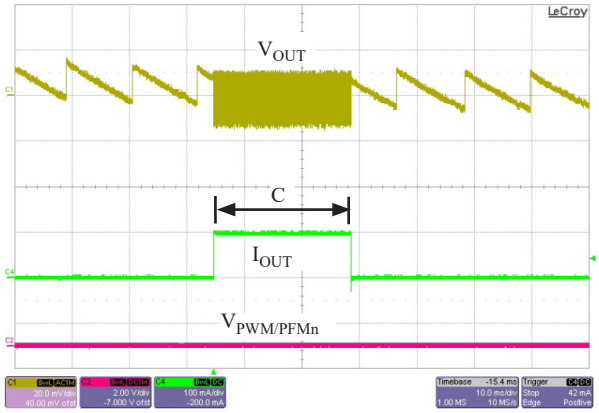
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Overall Waveforms

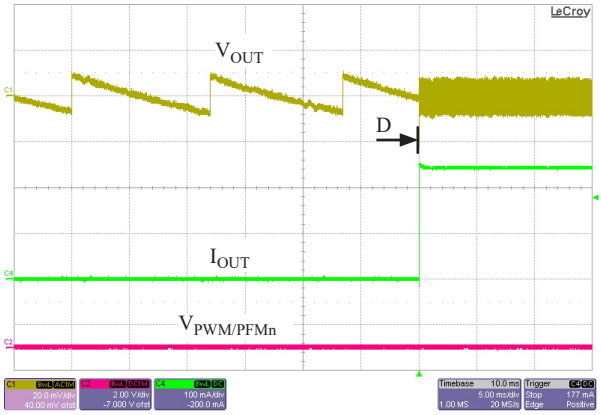




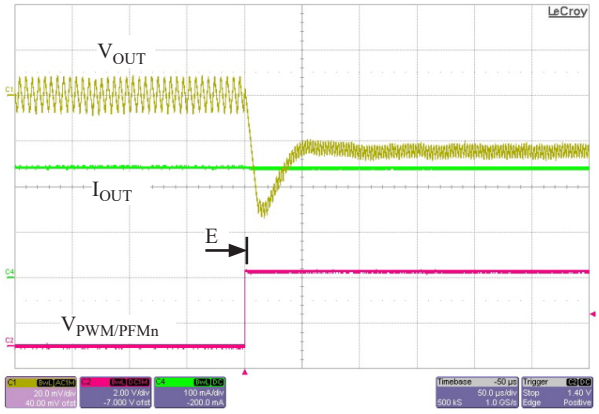
Time A: Transition from PWM to PFM at 250 mA
Time B: Load steps from 250 mA to 0 A in Low-IQ PFM mode



Time C: Load steps from 0 A to 100 mA and back to 0 A in Low-IQ PFM mode



Time D: Load steps from 0 A to 250 mA in Low-IQ PFM mode



Time E: Transition from Low-IQ PFM to PWM mode at 250 mA

Figure 6: Transitions between PWM Mode and Low-IQ PFM Mode, and Load Transient Responses; using circuit in typical application schematic B (V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 425 kHz)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

delay approximately $t_{OFF(PFM)}$ and either:

- turn on the MOSFET again, if V_{FB} < 800 mV, or
- return to the Low-IQ PFM mode

Figures 4 and 5 demonstrate Low-IQ PFM mode operation for a light load (66 mA) and a heavy load (330 mA), respectively.

In Low-IQ PFM mode the average current drawn from the input supply depends primarily on both the load, and how often the A8589 must fully power-up to maintain regulation. In Low-IQ PFM mode the following faults are detected: a missing asynchronous diode, an open or shorted boot capacitor, VOUT shorted to ground, and SW shorted to ground. As described in the next section, if any of these faults occur the A8589 will transition from Low-IQ PFM mode to Low-IP PWM mode, with operation at 50% of the current limit of the PWM switching mode. See Figure 14 for a timing diagram showing operation of the A8589 in Low-IQ PFM mode.

In Low-IQ PFM mode the A8589 dissipates very little power, so the thermal monitoring circuit (TSD) is not needed and is disabled to minimize the quiescent current and improve efficiency.

Figure 6 shows PWM to Low-IQ PFM transitions for a typical microcontroller or DSP system. The system starts in PWM mode at I_{OUT} = 250 mA and then transitions to Low-IQ PFM mode, also at I_{OUT} = 250 mA (time A). While in Low-IQ PFM mode the current drops from 250 mA to 0 A (time B) and cycles from no load to 100 mA (time C). In Low-IQ PFM mode the load steps from I_{OUT} = 0 A to 250 mA (time D) and then the A8589 transitions back to PWM mode (time E). For this example, the output ripple voltage is always less than 30 mV_{PP} and the transient deflection between modes is always less than 50 mV_{PEAK}.

Reduced Current (Low-IP) PWM Mode

The A8589 supports two different levels of current limiting in PWM modes:

- *100% current*, which is during normal PWM, and
- *Low-IP*, in which the current is limited to about 50% of the typical current limit

The Low-IP PWM mode is invoked when the A8589 is supposed to be in PFM mode but a fault occurs. The purpose of the Low-IP PWM mode is to give priority to maintaining reliable regulation of V_{OUT} while enabling all the protection circuits inside the A8589 that are normally debiased during Low-IQ PFM mode (high precision comparators, timers, and counters).

There are several faults that cause a transition from Low-IQ PFM to Low-IP PWM mode: a missing asynchronous diode, an open or shorted boot capacitor, VOUT shorted to ground, or SW shorted to ground. See Figure 14 for a timing diagram showing operation when the A8589 transitions from Low-IQ PFM mode to Low-IP PWM mode.

Soft Start (Startup) and Inrush Current Control

Inrush current is controlled by a soft start function. When the A8589 is enabled and all faults are cleared, the soft start pin will source I_{SSSU} and the voltage on the soft start capacitor, C_{SS} , will ramp upward from 0 V. When the voltage at the soft start pin exceeds approximately 400 mV, the error amplifier will slew its output voltage above the PWM Ramp Offset ($V_{PWMOFFS}$). At that instant, the high-side and low-side MOSFETs will begin switching. As shown in Figure 7, there is a small delay ($t_{D(SS)}$) between when the enable pin transitions high, and when both the soft start voltage exceeds 400 mV and the error amplifier slews its output high enough to initiate PWM switching.

After the A8589 begins switching, the error amplifier will regulate the voltage at the FB pin to the soft start pin voltage minus approximately 400 mV. During the active portion of soft start,

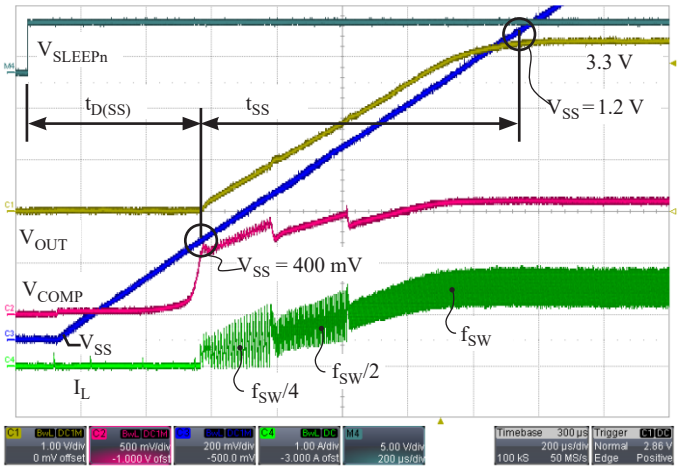


Figure 7: Normal Startup to V_{OUT} = 3.3 V and I_{OUT} = 1.6 A; PWM/PFMn Pin = high, SLEEPn Pin Transitions from Low to High

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

the voltage at the soft start pin rises from 400 mV to 1.2 V (a difference of 800 mV), the voltage at the FB pin rises from 0 V to 800 mV, and the regulator output voltage rises from 0 V to the targeted setpoint, which is determined by the feedback resistor divider on the FB pin.

During startup, the PWM switching frequency is reduced to 25% of f_{OSC} while V_{FB} is below 200 mV. If V_{FB} is above 200 mV but below 400 mV, the switching frequency is reduced to 50% of f_{OSC}. Also, if V_{FB} is below 400 mV, the g_m of the error amplifier is reduced to $g_m / 2$. When V_{FB} is above 400 mV the switching frequency will be f_{OSC} and the error amplifier gain will be g_m. The reduced switching frequencies and error amplifier gain are necessary to help improve output regulation and stability when VOUT is at a very low voltage. When V_{OUT} is very low, the PWM control loop requires on-times near the minimum controllable on-time, as well as extra-low duty cycles that are not possible at the base operating switching frequencies.

When the voltage at the soft start pin reaches approximately 1.2 V, the error amplifier will change mode and begin regulating the voltage at the FB pin to the A8589 internal reference, 800 mV. The voltage at the soft start pin will continue to rise to approximately V_{REG}. Complete soft start operation from V_{OUT} = 0 V is shown in Figure 7.

If the A8589 is disabled or a fault occurs, the internal fault latch will be set and the capacitor on the soft start pin will be discharged to ground very quickly by an internal 2 kΩ pull-down resistor. The A8589 will clear the internal fault latch when the voltage at the soft start pin decays to approximately 200 mV (V_{SSRST}). Conversely, if the A8589 enters hiccup mode, the capacitor on the soft start pin is slowly discharged by a current sink, I_{SSHIC}. Therefore, the soft start capacitor (C_{SS}) not only controls the startup time but also the time between soft start attempts in hiccup mode. Hiccup mode operation is discussed in more detail in the Protection Features section of this datasheet.

Pre-Biased Startup

If the output of the regulator (V_{OUT}) is pre-biased to some voltage, the A8589 will modify the normal startup routine to prevent discharging the output capacitors. As described previously, the error amplifier usually becomes active when the voltage at the soft start pin exceeds 400 mV. If the output is pre-biased, the FB pin will be at some non-zero voltage. The A8589 will not start switching until the voltage at the soft start pin increases to approximately V_{FB} + 400 mV. When the soft start pin voltage exceeds this value: the error amplifier becomes active, the voltage at the COMP pin rises, PWM switching starts, and V_{OUT} ramps upward from the pre-bias level. Figure 8 shows startup when the output voltage is pre-biased to 1.6 V.

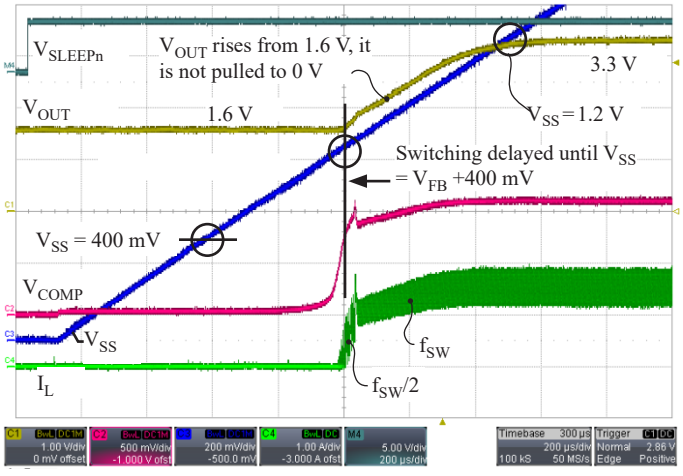


Figure 8: Pre-biased Startup from V_{OUT} = 1.6 V to V_{OUT} = 3.3 V, at I_{OUT} = 1.6 A

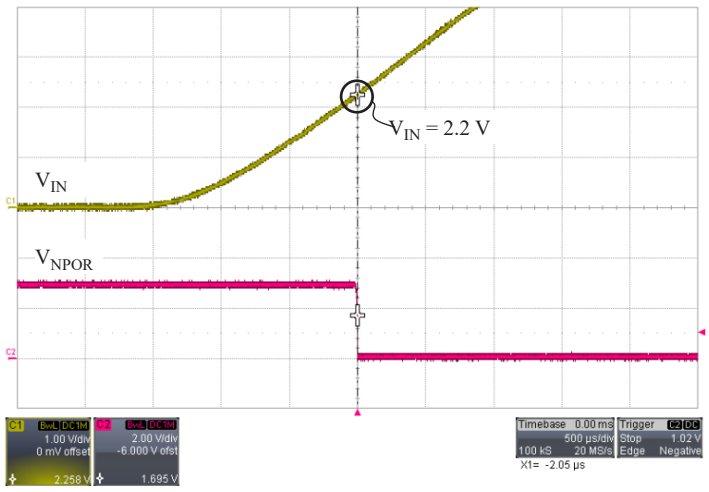


Figure 9: Initialization of NPOR as V_{IN} Ramps Up

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Not Power-On Reset (NPOR) Output

The A8589 has an inverted power-on reset output (NPOR) with a fixed delay of its rising edge ($t_{D(NPOR)}$). The NPOR output is an open drain output so an external pull-up resistor must be used, as shown in the Typical Applications schematics. NPOR transitions high when the output voltage (V_{OUT}), sensed at the FB pin, is within regulation. In PWM mode, NPOR is high when the output voltage is typically within 92.5% to 110% of the target value. In PFM mode, NPOR is high when the output voltage is typically above 87.5% of the target value. The NPOR overvoltage and undervoltage comparators incorporate a small amount of hysteresis (10 mV typically) and filtering (5 µs typically) to help reduce chattering due to voltage ripple at the FB pin.

The NPOR output is immediately pulled low either: if an output overvoltage or an undervoltage condition occurs, or if the A8589 junction temperature exceeds the thermal shutdown threshold (T_{SD}). For other faults, NPOR behavior depends on the output voltage. Table 2 summarizes all the A8589 fault modes and their effect on NPOR.

At power-up, NPOR must be initialized (set to a logic low) when V_{IN} is relatively low. Figure 9 shows V_{IN} ramping up, and also NPOR being set to a logic low when V_{IN} is only 2.2 V. For this test, NPOR was pulled up to an external 3.3 V supply via a 2 kΩ resistor.

At power-down, NPOR must be held in the logic low state as long as possible. Figure 10 shows V_{IN} ramping down and NPOR being held low until V_{IN} is only 1.3 V. For this test, NPOR was pulled up to an external 3.3 V supply via a 2 kΩ resistor.

Protection Features

The A8589 was designed to satisfy the most demanding automotive and non-automotive applications. In this section, a description of each protection feature is described and Table 2 summarizes the protection features and operation.

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout (UVLO) comparator monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the stop threshold ($V_{INUV(OFF)}$). The UVLO comparator incorporates some hysteresis ($V_{INUV(HYS)}$) to help reduce on-off cycling of the regulator due to resistive or inductive drops in the V_{IN} path during heavy loading or during startup.

PULSE-BY-PULSE OVERCURRENT PROTECTION (OCP)

The A8589 monitors the current in the high-side MOSFET and if the current exceeds the pulse-by-pulse overcurrent threshold (I_{LIM}) then the high-side MOSFET is turned off. Normal PWM operation resumes on the next clock pulse from the internal oscillator. The A8589 includes leading edge blanking to prevent falsely triggering the pulse-by-pulse current limit when the high-side MOSFET is turned on.

Because of the addition of the slope compensation ramp to the

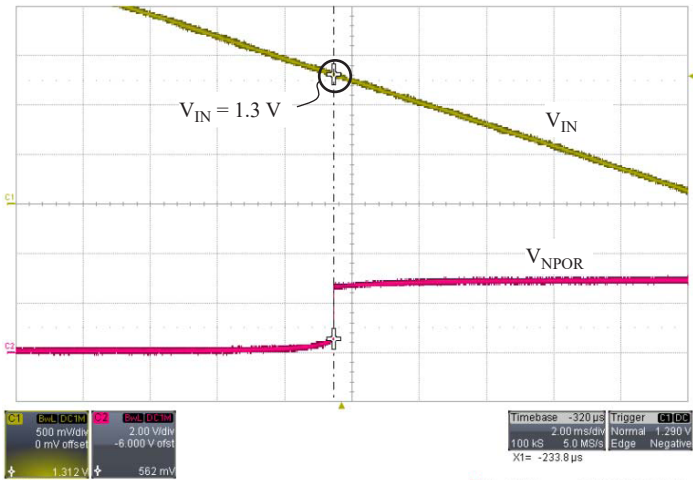


Figure 10: NPOR being Held Low as V_{IN} Ramps Down

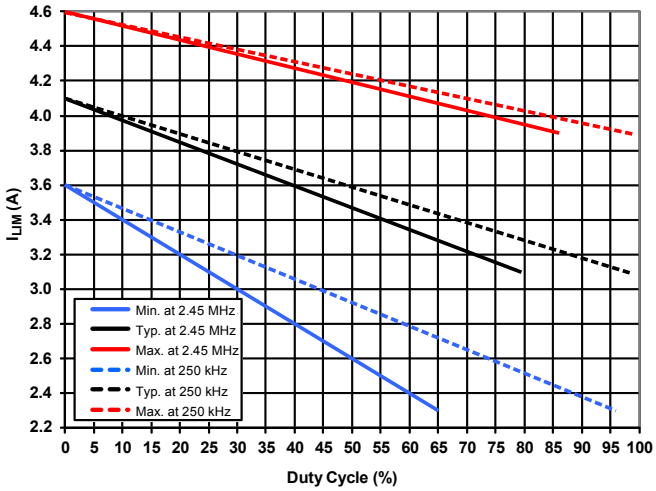


Figure 11: Pulse-by-pulse Current Limiting versus Duty Cycle; at f_{SW} = 250 kHz (dashed curves) and f_{SW} = 2.45 MHz (solid curves)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

inductor current, the A8589 delivers more current at lower duty cycles and less current at higher duty cycles. Also, the slope compensation is not a perfectly linear function of switching frequency. For a given duty cycle, this results in a little more current being available at lower switching frequencies than higher frequencies. Figure 11 shows the typical and worst-case min/max pulse-by-pulse current limits versus duty cycle at f_{SW} = 250 kHz and 2.45 MHz.

If the synchronization input (PWM/PFMn) is used to increase the switching frequency, the on-time and the current ripple will decrease. This will allow slightly more current than at the base switching frequency (f_{OSC}).

The exact current the buck regulators can support is heavily dependent on: duty cycle (V_{IN}, V_{OUT}, V_f), ambient temperature, thermal resistance of the PCB, airflow, component selection, and nearby heat sources.

OVERCURRENT PROTECTION (OCP) AND HICCUP MODE

An OCP counter and hiccup mode circuit protect the buck regulator when the output of the regulator is shorted to ground or when the load is too high. When the voltage at the soft start pin is below the hiccup OCP threshold (HIC/PFM_{EN}) the hiccup mode counter is disabled. Two conditions must be met for the OCP counter to be enabled and begin counting:

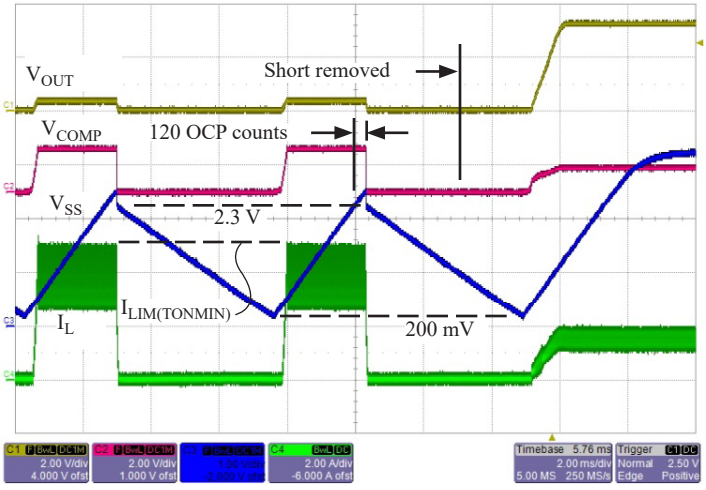


Figure 12. Hiccup Mode Operation and Recovery to V_{OUT} = 3.3 V, I_{OUT} = 1.6 A

- V_{SS} > HIC/PFM_{EN} (2.3 V (typ)) and
- V_{COMP} is clamped at its maximum voltage (OCL =1)

As long as these two conditions are met, the OCP counter remains enabled and will count pulses from the overcurrent comparator. If the COMP pin voltage decreases (OCL = 0) the OCP counter is cleared.

If the OCP counter reaches OCP_{LIM} counts (120), a hiccup latch is set and the COMP pin is quickly pulled down by a relatively low resistance (1 kΩ). The hiccup latch also enables a small current sink connected to the soft start pin (I_{SSHIC}). This causes the voltage at the soft start pin to slowly ramp downward. When the voltage at the soft start pin decays to a low enough level (V_{SSRST}, 200 mV (typ)) the hiccup latch is cleared and the small current sink turned off. At that instant, the soft start pin will begin to source current (I_{SSSU}) and the voltage at the soft start pin will ramp upward. This marks the beginning of a new, normal soft start cycle as described earlier. (Note: OCP is the only fault that results in hiccup mode that is ignored when V_{SS} < 2.3 V.)

When the voltage at the soft start pin exceeds the soft start offset (typically 400 mV) the error amplifier forces the voltage at the COMP pin to quickly slew upward and PWM switching will resume. If the short circuit at the regulator output remains, another hiccup cycle will occur. Hiccups will repeat until the short circuit is removed or the regulator is disabled. If the short circuit is removed, the A8589 will soft start normally and the output voltage will automatically recover to the target level, as shown in Figure 12.

BOOT CAPACITOR PROTECTION

The A8589 monitors the voltage across the BOOT capacitor to detect if the capacitor is missing or short circuited. If the BOOT capacitor is missing, the regulator will enter hiccup mode after 7 PWM cycles. If the BOOT capacitor is short circuited, the regulator will enter hiccup mode after 120 PWM cycles, provided there is no VOUT overvoltage detection. At no load or very light loads, the boot charging circuit will increase the output voltage (via the output inductor) and cause an overvoltage condition to be detected if V_{IN} > V_{OUT} + 5.7 V.

For a boot fault, hiccup mode will operate virtually the same as described previously for an output short circuit fault (OCP) with the soft start pin ramping up and down as a timer to initiate repeated soft start attempts. Boot faults are a non-latched condition, so the A8589 will automatically recover when the fault is corrected.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ASYNCHRONOUS DIODE PROTECTION

If the asynchronous diode (D1 in the Typical Applications schematics) is missing or damaged (open) the SW pin will be subject to unusually high negative voltages. These negative voltages may cause the A8589 to malfunction and could lead to damage.

The A8589 includes protection circuitry to detect when the asynchronous diode is missing. If the SW pin is below typically −1.25 V for more than about 50 ns, the A8589 will enter hiccup mode after detecting one missing diode fault. Also, if the asynchronous diode is short circuited, the A8589 will experience extremely high currents in the high-side MOSFET. If this occurs the A8589 will enter hiccup mode after detecting one short circuited diode fault.

OUTPUT OVERVOLTAGE PROTECTION (OVP)

The A8589 provides a basic level of overvoltage protection by monitoring the voltage level at the FB pin. Two overvoltage conditions can be detected:

- The FB pin is disconnected from its feedback resistor divider. In this case, a tiny internal current source forces the voltage at the FB pin to rise. When the voltage at the FB pin exceeds the overvoltage threshold ($V_{OUT(OV)PWM}$, 880 mV (typ)) PWM switching will stop and NPOR will be pulled low.
- A higher, external voltage supply is accidently shorted to the A8589s output. V_{FB} will probably rise above the overvoltage threshold and be detected as an overvoltage condition. In this case, the low-side MOSFET will continue to operate and can correct the OVP condition, provided that only a few milliamperes of pull-down current are required. In either case, if the condition causing the overvoltage is corrected the regulator will automatically recover.

PIN-TO-GROUND AND PIN-TO-PIN SHORT PROTECTIONS

The A8589 is designed to satisfy the most demanding automotive applications. For example, the A8589 has been carefully designed from the very beginning to withstand a short circuit to ground at each pin without suffering damage.

In addition, care was taken when defining the A8589 pin-out to optimize protection against pin-to-pin adjacent short circuits. For example, logic pins and high voltage pins are separated as much as possible. Inevitably, some low voltage pins are located adjacent to high voltage pins, but in these instances the low voltage pins are designed to withstand increased voltages, with clamps and/or series input resistance, to prevent damage to the A8589.

THERMAL SHUTDOWN (TSD)

The A8589 monitors junction temperature and will stop PWM switching and pull NPOR low if it becomes too hot. Also, to prepare for a restart, the soft start and COMP pins will be pulled low until $V_{SS} < V_{SS(RST)}$. TSD is a non-latched fault, so the A8589 will automatically recover if the junction temperature decreases by approximately 20°C.

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

TABLE 2: Summary of A8589 Fault Modes and Operation

Fault Mode	V_{SS}	During fault counting, before Hiccup mode			BOOT Charging	NPOR State	Latched?	Reset Condition
		V_{COMP}	High-Side MOSFET	Low-Side MOSFET				
Output overcurrent, V_{FB}< 200 mV	Hiccup, after 120 OCP faults	Clamped for I_{LIM}, then pulled low for hiccup	f_{OSC} / 4 due to V_{FB} < 200 mV, responds to V_{COMP}	Can be activated if V_{BOOT} is too low	Not affected	Depends on V_{OUT}	No	Automatic, after remove the short
Output overcurrent, V_{FB} > 400 mV	Hiccup, after 120 OCP faults	Clamped for I_{LIM}, then pulled low for hiccup	f_{OSC} due to V_{FB} > 400 mV, responds to V_{COMP}	Can be activated if V_{BOOT} is too low	Not affected	Depends on V_{OUT}	No	Automatic, after decrease load current
Boot capacitor open/missing ($BOOT_{OV}$)	Hiccup, after 7 $BOOT_{OV}$ faults	Pulled low for hiccup	Forced off when $BOOT_{OV}$ fault occurs	Forced off when BOOT fault occurs	Off after BOOT fault occurs	Depends on V_{OUT}	No	Automatic, after replace capacitor
Boot capacitor shorted ($BOOT_{UV}$)	Hiccup, after 120 $BOOT_{UV}$ faults	Not affected, pulled low for hiccup	Forced off when $BOOT_{UV}$ fault occurs	Forced off only during hiccup	Off only during hiccup	Depends on V_{OUT}	No	Automatic, after unshort capacitor
Asynchronous diode missing	Hiccup after 1 fault	Pulled low for hiccup	Forced off after 1 fault	Can be activated if V_{BOOT} is too low	Not affected	Depends on V_{OUT}	No	Automatic, after install diode
Asynchronous diode (or SW) hard short to ground	Hiccup after 1 fault	Pulled low for hiccup	Forced off after 1 fault	Can be activated if V_{BOOT} is too low	Not affected	Depends on V_{OUT}	No	Automatic, after remove short
Asynchronous diode (or SW) soft short to ground	Hiccup, after 120 OCP faults	Clamped for I_{LIM}, then pulled low for hiccup	Active, responds to V_{COMP}	Can be activated if V_{BOOT} is too low	Not affected	Depends on V_{OUT}	No	Automatic, after remove short
FB pin open (FB floats high)	Begins to ramp up for soft start	Transitions low via loop response	Forced off by low V_{COMP}	Active during $t_{OFF(MIN)PWM}$	Off when V_{FB} is too high	Pulled low when V_{FB} is too high	No	Automatic, after connect FB pin
Output overvoltage (V_{FB} > 880 mV)	Not affected	Transitions low via loop response	Forced off by low V_{COMP}	Active during $t_{OFF(MIN)PWM}$	Off when V_{FB} is too high	Pulled low when V_{FB} is too high	No	Automatic, after V_{FB} returns to normal range
Output undervoltage	Not affected	Transitions high via loop response	Active, responds to V_{COMP}	Can be activated if V_{BOOT} is too low	Not affected	Pulled low when V_{FB} is too low	No	Automatic, after V_{FB} returns to normal range
Thermal shutdown	Pulled low and latched until V_{SS} < V_{SSRST}	Pulled low and latched until V_{SS} < V_{SSRST}	Forced off by low V_{COMP}	Disabled	Off	Pulled low	No	Automatic, after part cools down
VREG or BIAS overvoltage (REGOV)	Not affected	Transitions low via loop response	Forced off by low V_{COMP}	Active during $t_{OFF(MIN)PWM}$	Off	Pulled low	No	Automatic, VREG or BIAS to normal range

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

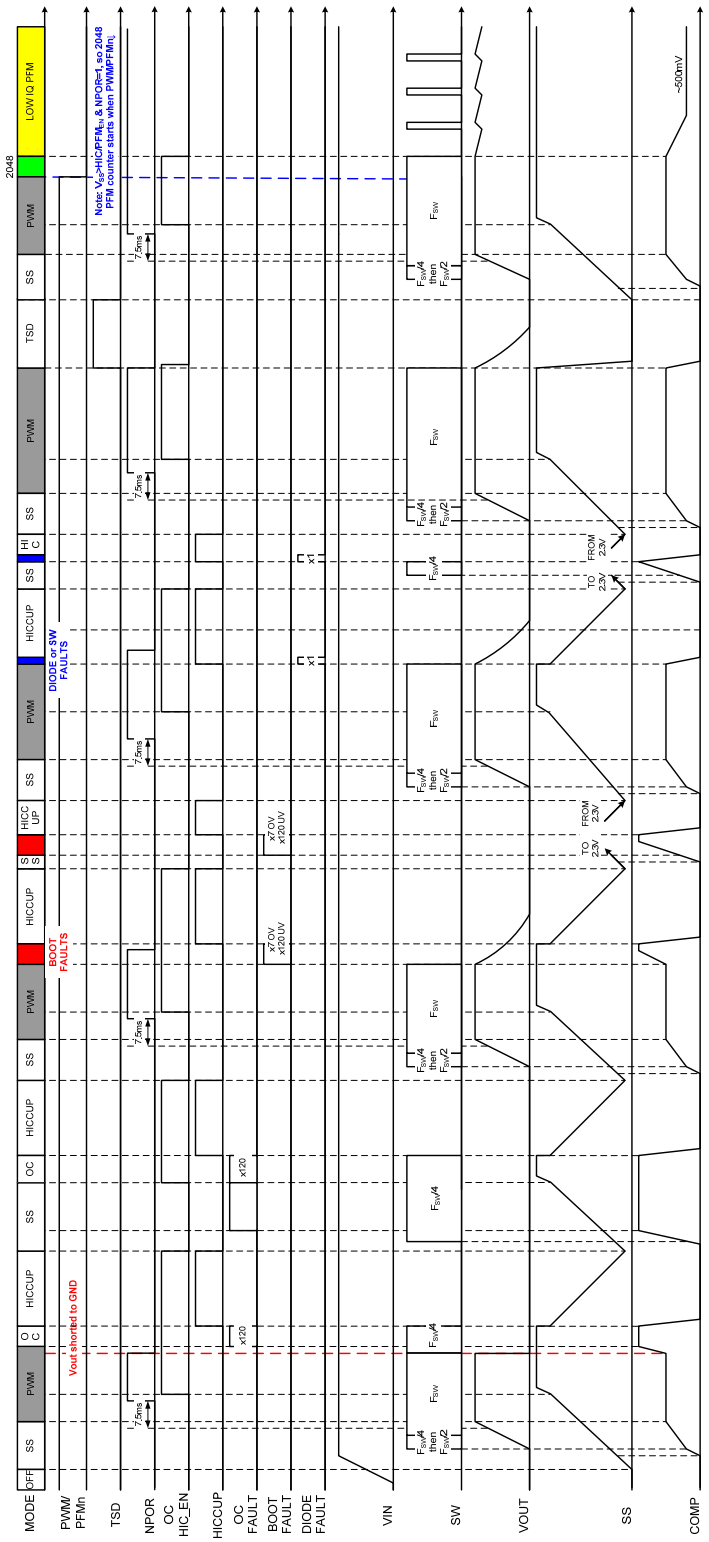


Figure 13: Operation with SLEEPn = high and PWM/PFMn = high (PWM mode)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

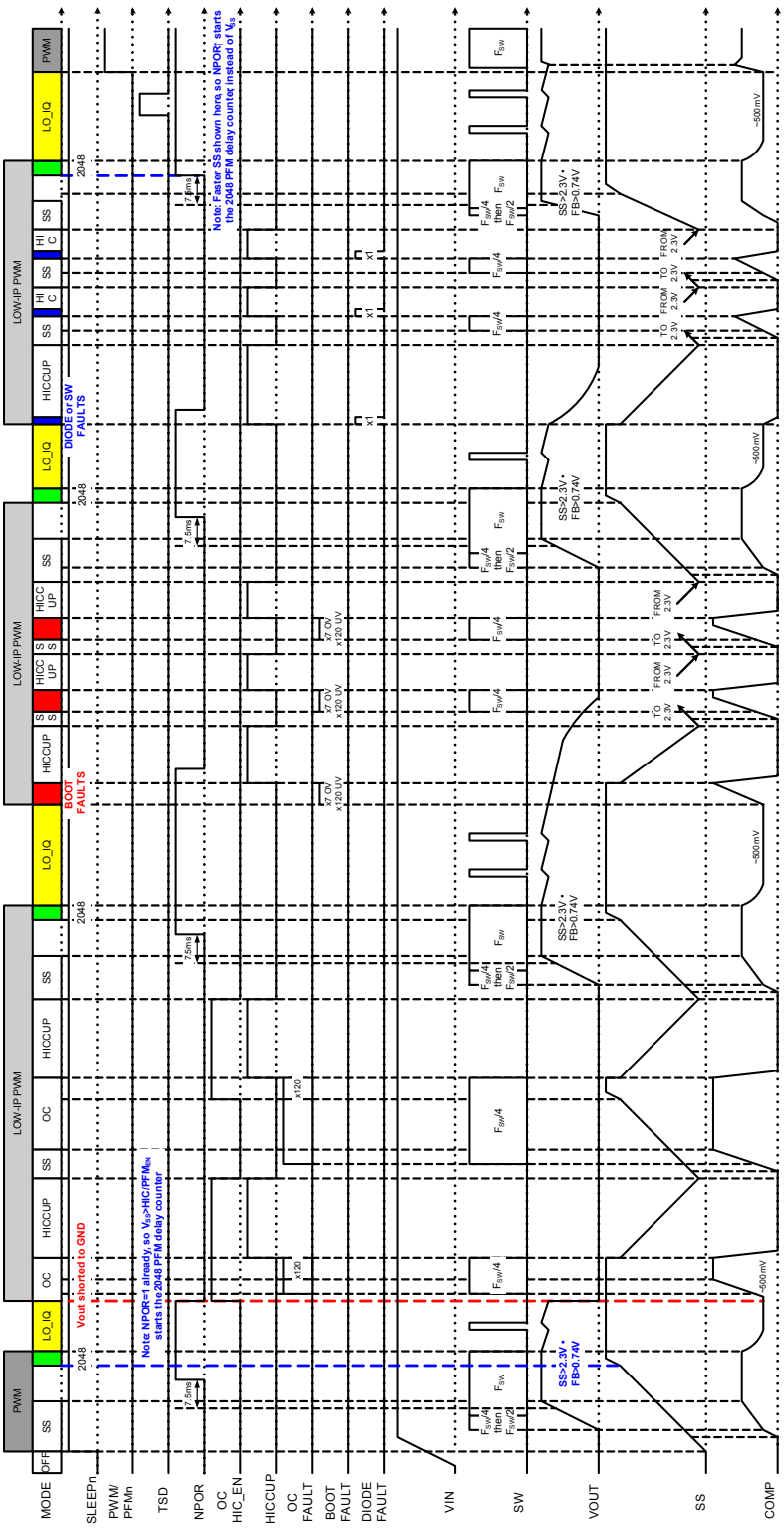


Figure 14: Operation with SLEEPn = high and PWM/PFMn = low (Low-IQ PFM mode and transition to Low-IP PWM mode)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATION INFORMATION

Design and Component Selection

SETTING THE OUTPUT VOLTAGE (V_{OUT})

The output voltage of the regulator is determined by connecting a resistor divider from the output node (VOUT) to the FB pin as shown in Figure 15. There are trade-offs when choosing the value of the feedback resistors. If the series combination (RFB1 + RFB2) is too low, then the light load efficiency of the regulator will be reduced. So to maximize the efficiency, it is best to choose higher values of resistors. On the other hand, if the parallel combination (RFB1 // RFB2) is too high, then the regulator may be susceptible to noise coupling onto the FB pin.

The feedback resistors must satisfy the ratio shown in the following equation to produce the target output voltage, V_{OUT}:

$$\frac{R_{FB1}}{R_{FB2}} = \left(\frac{V_{OUT}}{0.8\ (V)} - 1\right) \qquad (1)$$

Compared to typical buck regulators, a PFM capable buck regulator presents some unique challenges when determining its feedback divider. This resistor divider must draw minimal current from VOUT or it will reduce the efficiency during Low-IQ PFM operation. With this in mind, Allegro recommends the resistor values show in Table 3 on page 34.

For Low-IQ PFM mode, a feedforward capacitor (CFB) should be connected in parallel with RFB1, as shown in Figure 16. The purpose of this capacitor is to offset any stray capacitance (C_{STRAY}) from the FB pin to ground. Without CFB, the stray capacitance and the relatively high resistor values used for the feedback network form a low pass filter and introduce lag to the Low-IQ PFM feedback path. The feedforward capacitor helps to maintain sensitivity during Low-IQ PFM mode and to assure the output voltage ripple is minimized.

In general, CFB should be calculated as:

$$C_{FB} > (1.5 \times C_{STRAY}) \times (R_{FB2} / R_{FB1}) \qquad (2)$$

where C_{STRAY} is typically 15 to 25 pF.

PWM BASE SWITCHING FREQUENCY (F_{OSC}, R_{FSET})

The PWM base switching frequency, f_{OSC}, is set by connecting a resistor from the FSET pin to ground. Figure 17 is a graph show-

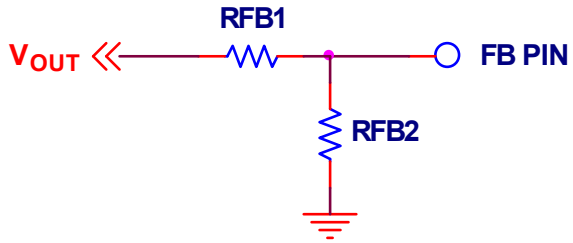


Figure 15: Connecting a Feedback Resistor Divider to Set the Output Voltage

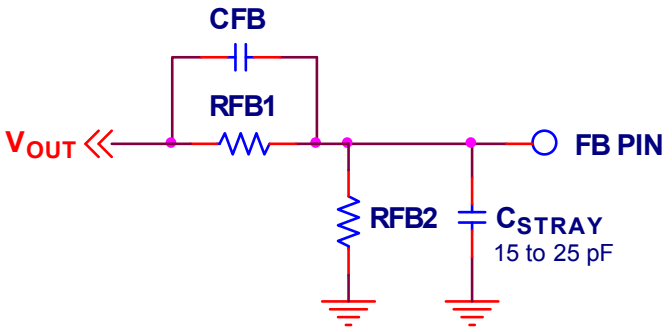


Figure 16: Addition of CFB to Cancel Stray Capacitance at the FB Pin in PFM Mode

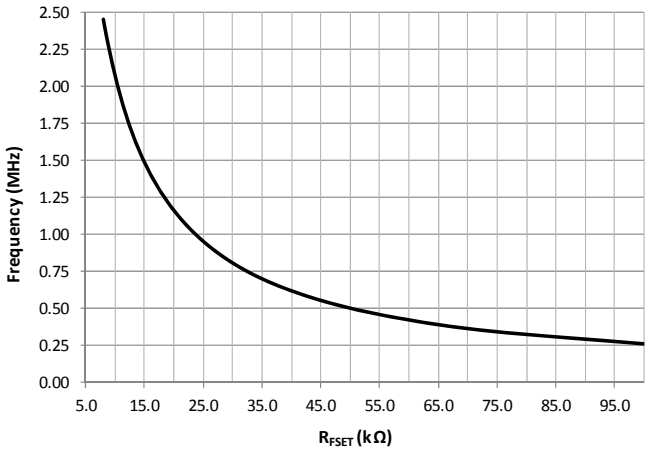


Figure 17: PWM Switching Frequency versus R_{FSET}

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ing the relationship between the typical switching frequency and the FSET resistor. The base frequency is the output frequency, f_{SW}, when PWMPFMn is high (no external clocking signal). For a given base switching frequency (f_{OSC}), the FSET resistor can be calculated as follows:

$$R_{FSET} = \left(\frac{26385}{f_{OSC}} - 2.75 \right) \quad (3)$$

where f_{OSC} is in kHz and R_{FSET} is in kΩ.

When the PWM base switching frequency is chosen the designer should be aware of the minimum controllable on-time, $t_{ON(MIN)PWM}$ of the A8589. If the system required on-time is less than the A8589 minimum controllable on-time, switch node jitter occurs and the output voltage will have increased ripple or oscillations.

The PWM base switching frequency required should be calculated as follows:

$$f_{OSC} < \frac{V_{OUT}}{t_{ON(MIN)PWM} \times V_{IN(MAX)REQ}} \quad (4)$$

where

V_{OUT} is the output voltage,

$t_{ON(MIN)PWM}$ is the minimum controllable on-time of the A8589 (95 ns (typ), 135 ns (max)), and

$V_{IN(MAX)REQ}$ is the maximum required operational input voltage (not the peak surge voltage).

If the A8589 PWM synchronization function is employed, then the base switching frequency should be chosen such that jitter will not result at the maximum synchronized switching frequency, determined from equation 4:

$$f_{OSC} < 0.66 \times \frac{V_{OUT}}{t_{ON(MIN)PWM} \times V_{IN(MAX)REQ}} \quad (5)$$

OUTPUT INDUCTOR (L_O)

For a peak current mode regulator, it is common knowledge that, without adequate slope compensation, the system will become unstable when the duty cycle is near or above 50%. However, the slope compensation in the A8589 is a fixed value (S_E). Therefore, it is important to calculate an inductor value such that the falling slope of the inductor current (S_F) will work well with the A8589 slope compensation. The following equation can be used to calculate a range of values for the output inductor based on the well-known approach of providing slope compensation that matches 50% to 100% of the falling slope of the inductor current:

$$\left(\frac{V_{OUT} + V_f}{2 \times S_E} \right) \leq L_O \leq \left(\frac{V_{OUT} + V_f}{S_E} \right) \quad (6)$$

where V_f is the forward voltage of the asynchronous diode, and L_O is in µH.

In equation 6, the slope compensation (S_E) is a function of switching frequency according the following:

$$S_E = 0.23 \times f_{OSC}^2 + 0.63 \times f_{OSC} + 0.038 \quad (7)$$

where S_E is in A/µs and f_{OSC} is in MHz.

More recently, Dr. Raymond Ridley presented a formula to calculate the amount of slope compensation required to critically damp the double poles at half the PWM switching frequency:

$$L_o \geq \frac{V_{OUT}+V_f}{S_E} \left(1 - \frac{0.18}{D} \right)$$

$$= \frac{V_{OUT}+V_f}{S_E} \left(1 - 0.18 \times \frac{(V_{IN}(\min)+V_f)}{V_{OUT}+V_f} \right) \quad (8)$$

This formula allows the inclusion of the duty cycle (D), which should be calculated at the minimum input voltage to insure optimal stability. Also, to avoid dropout (that is, saturation of the buck regulator), V_{IN}(min) must be approximately 1 to 1.5 V above V_{OUT} when calculating the inductor value with equation 8.

If equations 7 or 8 yield an inductor value that is not a standard value, then the next highest available value should be used. The final inductor value should allow for 10% to 20% of initial tolerance and 20% to 30% of inductor saturation.

The saturation current of the inductor should be higher than the peak current capability of the A8589. Ideally, for output short circuit conditions, the inductor should not saturate even at the highest pulse-by-pulse current limit at minimum duty cycle, 4.6 A.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

This may be too costly. At the very least, the inductor should not saturate at the peak operating current according to the following:

$$I_{PEAK} = 4.1 - \frac{S_E \times (V_{OUT}+V_f)}{1.15 \times f_{OSC} \times (V_{IN}(max)+V_f)} \quad (9)$$

where $V_{IN}(max)$ is the maximum continuous input voltage, such as 18 V (not a surge voltage, such as 40 V).

Starting with equation 9, and subtracting half of the inductor ripple current, provides us with an interesting equation to predict the typical DC load capability of the regulator at a given duty cycle (D):

$$I_{OUT(DC)} = 4.1 - \frac{S_E \times D}{f_{OSC}} - \frac{V_{OUT} \times (1-D)}{2 \times f_{OSC} \times L_O} \quad (10)$$

After an inductor is chosen, it should be tested during output short circuit conditions. The inductor current should be monitored using a current probe. A good design would ensure neither the inductor nor the regulator are damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

OUTPUT CAPACITORS

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage and they store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{OUT}) is a function of the output capacitor parameters: C_{OUT}, ESR_{COUT}, and ESL_{COUT}:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{COUT} + \frac{V_{IN}-V_{OUT}}{L_O} \times ESL_{COUT} + \frac{\Delta I_L}{8 f_{SW} C_{OUT}} \quad (11)$$

The type of output capacitors will determine which terms of equation 11 are dominant. For ceramic output capacitors the ESR_{COUT} and ESL_{COUT} are virtually zero, so the output voltage ripple will be dominated by the third term of equation 11:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 f_{SW} C_{OUT}} \quad (12)$$

To reduce the voltage ripple of a design using ceramic output capacitors, simply: increase the total capacitance, reduce the inductor current ripple (that is, increase the inductor value), or increase the switching frequency.

For electrolytic output capacitors the value of capacitance will be relatively high, so the third term in equation 11 will be very small. The output voltage ripple will be determined primarily by the first two terms of equation 11:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{COUT} + \frac{V_{IN}-V_{OUT}}{L_O} \times ESL_{COUT} \quad (13)$$

To reduce the voltage ripple of a design using electrolytic output capacitors, simply: decrease the equivalent ESR_{CO} and ESL_{CO} by using a high(er) quality capacitor, or add more capacitors in parallel, or reduce the inductor current ripple (that is, increase the inductor value).

The ESR of some electrolytic capacitors can be quite high so Allegro recommends choosing a quality capacitor for which the ESR or the total impedance is clearly documented in the data-sheet. Also, the ESR of electrolytic capacitors usually increases significantly at cold ambients, as much as 10×, which increases the output voltage ripple and, in most cases, reduces the stability of the system.

The transient response of the regulator depends on the quantity and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (di/dt), the output voltage will change by the amount:

$$\Delta V_{OUT} = \Delta I_{LOAD} \times ESR_{COUT} + \frac{di}{dt} ESL_{COUT} \quad (14)$$

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

After the load transient occurs, the output voltage will deviate from its nominal value for a short time. This time will depend on the system bandwidth, the output inductor value, and output capacitance. Eventually, the error amplifier will bring the output voltage back to its nominal value.

The speed at which the error amplifier brings the output voltage back to its setpoint depends mainly on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, with a higher bandwidth system, it may be more difficult to obtain acceptable gain and phase margins. Selection of the compensation components (RZ, CZ, and CP) are discussed in more detail in the Compensation Components section of this datasheet.

LOW-IQ PFM OUTPUT VOLTAGE RIPPLE CALCULATION

After choosing an output inductor and output capacitor(s), its important to calculate the output voltage ripple ($\Delta V_{OUT(PFM)}$) that will occur during Low-IQ PFM mode. With ceramic output capacitors the output voltage ripple in PWM mode is usually negligible, but that is not the case during Low-IQ PFM mode.

First, calculate the high-side MOSFET on-time and off-time. The on-time is defined as the time it takes for the inductor current to reach the peak current threshold, $I_{PEAK(LO\_IQ)}$:

$$t_{ON} = \frac{I_{PEAK(LO\_IQ)} \times L_O}{V_{IN} - V_{OUT} - I_{PEAK(LO\_IQ)} \times (R_{DS(on)HS} + DCR_{LO})} \quad (15)$$

Where $R_{DS(on)}$ is the on-resistance (110 mΩ (typ)) of the high-side MOSFET and DCR_{LO} is the DC resistance of the output inductor, L_O. For relatively low input voltages, the on-time during Low-IQ PFM mode is internally limited to about 4.1 µs.

The off-time is defined as the time it takes for the inductor current to decay from $I_{PEAK(LO\_IQ)}$ to 0 A:

$$t_{OFF} = \frac{I_{PEAK(LO\_IQ)} \times L_O}{V_{OUT} + V_f} \quad (16)$$

Finally, the Low-IQ PFM output voltage ripple can be calculated:

$$\Delta V_{OUT(LO\_IQ)} = \frac{I_{PEAK(LO\_IQ)} \times (t_{ON} + t_{OFF})}{2 \times C_{OUT}} \quad (17)$$

If the Low-IQ PFM output voltage ripple appears to be too high, then the output capacitance should be increased and/or the output inductance should be decreased. Decreasing the inductor value has the drawback of increasing the ripple current, so a higher load current will be required to transition from discontinuous conduction mode (DCM) to continuous conduction mode (CCM). This might not be acceptable.

In general, the Low-IQ PFM output voltage ripple increases as the input voltage decreases. Also, from equation 15, note that t_{ON} increases as the V_{OUT}/V_{IN} ratio increases (that is, as V_{IN} decreases). If the V_{OUT}/V_{IN} ratio is too high, the system is not able to achieve $I_{PEAK(LO\_IQ)}$ in only one PFM pulse. In this case the on-time is limited to approximately 4.1 µs and a second PFM pulse is required, about $t_{OFF(PFM)}$ later, as shown in figure 5.

INPUT CAPACITORS

Three factors should be considered when choosing the input capacitors. First, they must be chosen to support the maximum expected input surge voltage with adequate design margin. Second, the capacitor rms current rating must be higher than the expected rms input current to the regulator. Third, they must have enough capacitance and a low enough ESR to limit the input voltage dV/dt to something much less than the hysteresis of the VIN pin UVLO circuitry ($V_{INUV(HYS)}$, nominally 400 mV for the A8589), at maximum loading and minimum input voltage.

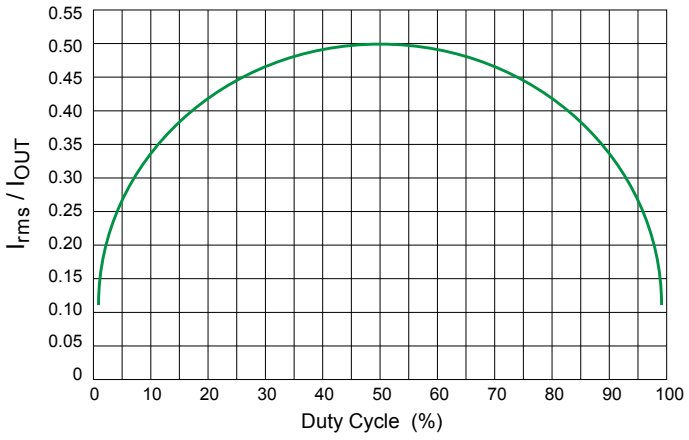


Figure 18: Input Capacitor Ripple versus Duty Cycle

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The input capacitors must deliver the rms current according to:

$$I_{rms} = I_{OUT} \sqrt{D \times (1 - D)} \quad (18)$$

where the duty cycle is:

$$D \approx (V_{OUT} + V_f) / (V_{IN} + V_f) \quad (19)$$

and V_f is the forward voltage of the asynchronous diode, D_1.

Figure 18 shows the normalized input capacitor rms current versus duty cycle. To use this graph, simply find the operational duty cycle (D) on the x-axis and determine the input/output current multiplier on the y-axis. For example, at a 20% duty cycle, the input/output current multiplier is 0.40. Therefore, if the regulator is delivering 2.5 A of steady-state load current, the input capacitor(s) must support 0.40 × 2.5 A, or 1.0 A_{rms}.

The input capacitor(s) must limit the voltage deviations at the VIN pin to something significantly less than the A8589 VIN pin UVLO hysteresis during maximum load and minimum input voltage. The minimum input capacitance can be calculated as follows:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{0.85 \times f_{OSC} \times \Delta V_{IN(MIN)}} \quad (20)$$

where $\Delta V_{IN(MIN)}$ is chosen to be much less than the hysteresis of the VIN pin UVLO comparator ($\Delta V_{IN(MIN)} \leq 150$ mV is recommended).

The D × (1-D) term in equation 20 has an absolute maximum value of 0.25 at 50% duty cycle. So, for example, a very conservative design, based on: I_{OUT} = 2.5 A, f_{OSC} = 85% of 425 kHz, D × (1-D) = 0.25, and ΔV_{IN} = 150 mV, yields:

$$C_{IN} \geq \frac{2.5\ (A) \times 0.25}{361\ (kHz) \times 150\ (mV)} = 11.5\ \mu F$$

A good design should consider the DC bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction) so these types should be avoided. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

For all ceramic capacitors, the DC bias effect is even more pronounced on smaller sizes of device case, so a good design uses the largest affordable case size (such as 1206 or 1210). Also, it is advisable to select input capacitors with plenty of design margin in the voltage rating to accommodate the worst-case transient input voltage (such as a load dump as high as 40 V for automotive applications).

ASYNCHRONOUS DIODE (D1)

There are three requirements for the asynchronous diode. First, the asynchronous diode must be able to withstand the regulator input voltage when the high-side MOSFET is on. Therefore, one should choose a diode with a reverse voltage rating (V_R) higher than the maximum expected input voltage (that is, the surge voltage).

Second, the forward voltage of the diode (V_f) should be minimized or the regulator efficiency suffers. Also if V_f is too high, the A8589 missing diode protection function could be falsely activated. A Schottky type diode that can maintain a very low V_f when the regulator output is shorted to ground, at the coldest ambient temperature, is highly recommended.

Third, the asynchronous diode must conduct the output current when the high-side MOSFET is turned off. Therefore, the average forward current rating of this diode ($I_{f(AVG)}$) must be high enough to deliver the load current according to

$$I_{f(AVG)} \geq I_{OUT(MAX)} (1 - D_{MIN}) \quad (21)$$

where D_{MIN} is the minimum duty cycle defined in equation 19, and $I_{OUT(MAX)}$ is the maximum continuous output current of the regulator.

BOOTSTRAP CAPACITOR

A bootstrap capacitor must be connected between the BOOT and SW pins to provide the floating gate drive to the high-side MOSFET. Usually, 47 nF is an adequate value. This capacitor should be a high-quality ceramic capacitor, such as an X5R or X7R, with a voltage rating of at least 16 V.

The A8589 incorporates a 10 Ω low-side MOSFET to ensure that the bootstrap capacitor is always charged, even when the regulator is lightly loaded or pre-biased.

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SOFT START AND HICCUP MODE TIMING (C_{SS})

The soft start time of the A8589 is determined by the value of the capacitance at the soft start pin, C_{SS}. When the A8589 is enabled, the voltage at the soft start pin starts from 0 V and is charged by the soft start current, I_{SSSU}. However, PWM switching does not begin instantly because the voltage at the soft start pin must rise above 400 mV. The soft start delay ($t_{D(SS)}$) can be calculated as:

$$t_{D(SS)} = C_{SS} \times \left(\frac{400\ (\text{mV})}{I_{SSSU}} \right) \quad (22)$$

If the A8589 is starting with a very heavy load, a very fast soft start time may cause the regulator to exceed the pulse-by-pulse overcurrent threshold. This occurs because the total of the full load current, the inductor ripple current, and the additional current required to charge the output capacitors:

$$I_{CO} = C_{OUT} \times V_{OUT} / t_{SS} \quad (23)$$

is higher than the pulse-by-pulse current threshold, as shown in figure 19. This phenomenon is more pronounced when using high value electrolytic type output capacitors. To avoid prematurely triggering hiccup mode the soft start capacitor, C_{SS}, should be calculated according to:

$$C_{SS} \geq \frac{I_{SSSU} \times V_{OUT} \times C_{OUT}}{0.8\ (\text{V}) \times I_{CO}} \quad (24)$$

where V_{OUT} is the output voltage, C_{OUT} is the output capacitance, I_{CO} is the amount of current allowed to charge the output capacitance during soft start (recommended: 0.1 A < I_{CO} < 0.3 A). Higher values of I_{CO} result in faster soft start times. However, lower values of I_{CO} ensure that hiccup mode is not falsely triggered. Allegro recommends starting the design with an I_{CO} of 0.1 A and increasing it only if the soft start time is too slow. If a non-standard capacitor value for C_{SS} is calculated, the next larger value should be used.

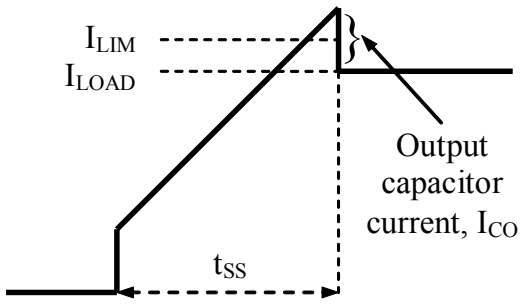


Figure 19: Output Current (I_{CO}) During Startup

The output voltage ramp time, t_{SS}, can be calculated by using either of the following methods:

$$t_{SS} = V_{OUT} \times \frac{C_{OUT}}{I_{CO}} \quad (25)$$

or

$$t_{SS} = 0.8\ (\text{V}) \times \frac{C_{SS}}{I_{SSSU}} \quad (26)$$

When the A8589 is in hiccup mode, the soft start capacitor is used as a timing capacitor and sets the hiccup period. The soft start pin charges the soft start capacitor with I_{SSSU} during a startup attempt and discharges the same capacitor with I_{SSHIC} between startup attempts. Because the ratio I_{SSSU} / I_{SSHIC} is approximately 4:1, the time between hiccups will be about four times as long as the startup time. Therefore, the effective duty-cycle of the A8589 will be very low and the junction temperature will be kept low.

COMPENSATION COMPONENTS (RZ, CZ, AND CP)

To properly compensate the system, it is important to understand where the buck power stage, load resistance, and output capacitance form their poles and zeros in frequency. Also, it is important to understand that the (Type II) compensated error amplifier introduces a zero and two more poles, and where these should be placed to maximize system stability, provide a high bandwidth, and optimize the transient response.

First, consider the power stage of the A8589, the output capacitors, and the load resistance. This circuitry is commonly referred as the *control-to-output* transfer function. The low frequency gain of this circuitry depends on the COMP to SW current gain (g_{mPOWER}), and the value of the load resistor (R_L). The DC gain ($G_{CO(0Hz)}$) of the control-to-output is:

$$G_{CO(0Hz)} = g_{mPOWER} \times R_L \quad (27)$$

The control-to-output transfer function has a pole (f_{P1}), formed

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

by the output capacitance (C_{OUT}) and load resistance (R_L), located at:

$$f_{P1} = \frac{1}{2\pi \times R_L \times C_{OUT}} \quad (28)$$

The control-to-output transfer function also has a zero (f_{Z1}) formed by the output capacitance (C_{OUT}) and its associated ESR:

$$f_{Z1} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad (29)$$

For a design with very low-ESR type output capacitors (such as ceramic or OS-CON™ output capacitors), the ESR zero (f_{Z1}) is usually at a very high frequency, so it can be ignored. On the other hand, if the ESR zero falls below or near the 0 dB crossover frequency of the system (as is the case with electrolytic output capacitors), then it should be cancelled by the pole formed by the CP capacitor and the RZ resistor (discussed and identified later as f_{P3}).

A Bode plot of the control-to-output transfer function for the configuration shown in typical application schematic B (V_{OUT} = 5.0 V, I_{OUT} = 2.5 A, R_L = 2 Ω) is shown in Figure 20. The pole at f_{P1} can easily be seen at 1.9 kHz while the ESR zero (f_{Z1}) occurs at a very high frequency, 636 kHz (this is typical for a

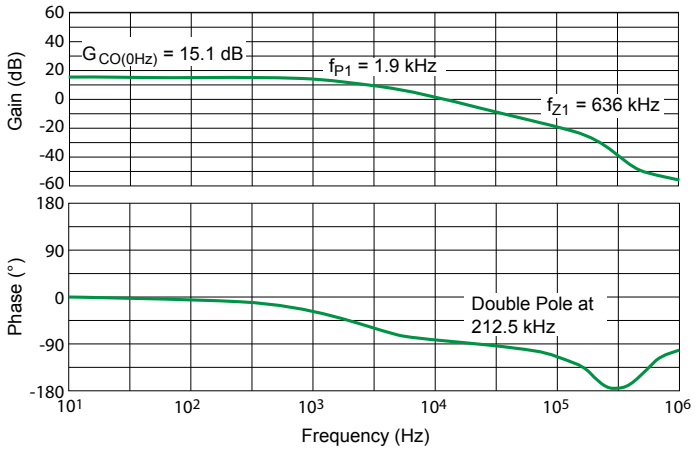


Figure 20: Control-to-Output Bode Plot

design using ceramic output capacitors). Note: There is more than 90° of total phase shift because of the double-pole at half the switching frequency.

Next, consider the feedback resistor divider (RFB1 and RFB2), and the error amplifier (g_m) and compensation network RZ-CZ-CP. It greatly simplifies the transfer function derivation if $R_O >> R_Z$, and $C_Z >> C_P$. In most cases, R_O > 2 MΩ, 1 kΩ < R_Z < 100 kΩ, 220 pF < C_Z < 47 nF, and C_P < 50 pF, so the following equations are very accurate.

The low frequency gain of the control section ($G_{C(0Hz)}$) is formed by the feedback resistor divider and the error amplifier. It can be calculated using:

$$G_{C(0Hz)} = \frac{R_{FB2}}{R_{FB1}+R_{FB2}} \times g_m \times R_O = \frac{V_{FB}}{V_{OUT}} \times g_m \times R_O = \frac{V_{FB}}{V_{OUT}} \times A_{VOL} \quad (30)$$

where

V_{OUT} is the output voltage,

V_{FB} is the reference voltage (0.8 V),

g_m is the error amplifier transconductance (750 µA/V), and

R_O is the error amplifier output impedance (A_{VOL}/g_m).

The transfer function of the Type-II compensated error amplifier has a (very) low frequency pole (f_{P2}) dominated by the output error amplifier output impedance (R_O) and the C_Z compensation capacitor:

$$f_{P2} = \frac{1}{2\pi \times R_O \times C_Z} \quad (31)$$

The transfer function of the Type-II compensated error amplifier also has frequency zero (f_{Z2}) dominated by the R_Z resistor and the C_Z capacitor:

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

$$f_{Z2} = \frac{1}{2\pi \times R_Z \times C_Z} \quad (32)$$

$$f_{P3} = \frac{1}{2\pi \times R_Z \times C_P} \quad (33)$$

Lastly, the transfer function of the Type-II compensated error amplifier has a (very) high frequency pole (f_{P3}) dominated by the R_Z resistor and the C_P capacitor:

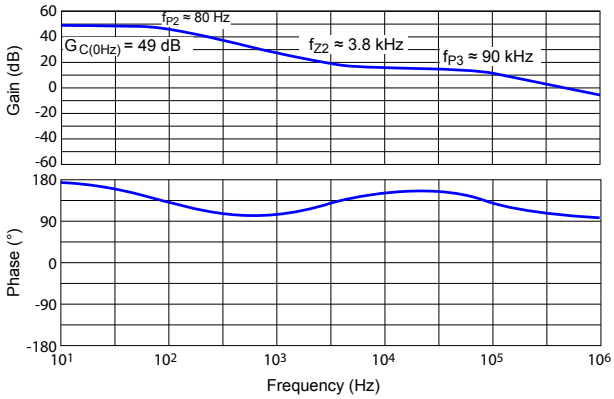


Figure 21: Type-II Compensated Error Amplifier

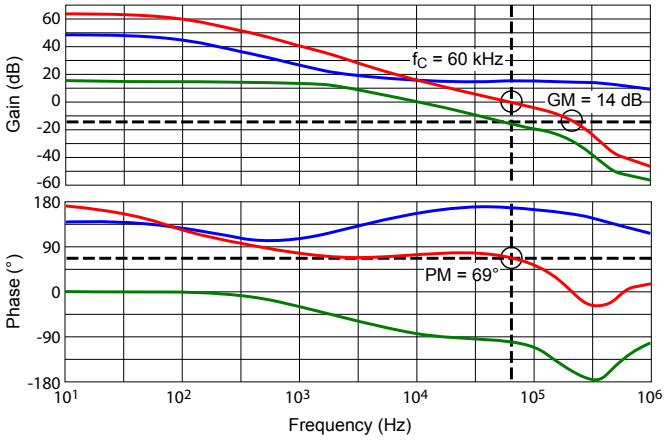


Figure 22: Bode Plot of the Complete System (red curves)

A Bode plot of the error amplifier and its compensation network is shown in Figure 21, f_{P2}, f_{P3}, and f_{Z2} are indicated on the magnitude plot. Notice that the zero (f_{Z2} at 3.8 kHz) has been placed so that it is just above the pole at f_{P1} previously shown in the control-to-output Bode plot (Figure 20) at 1.9 kHz. Placing f_{Z2} just above f_{P1} will result in excellent phase margin, but relatively slow transient recovery time, as will be shown later.

Finally, consider the combined Bode plot of both the control-to-output and the compensated error amplifier (Figure 22). Careful examination of this plot shows that the magnitude and phase of the entire system (red curve) are simply the sum of the error amplifier response (blue curve) and the control-to-output response (green curve). The bandwidth of this system (f_C) is 60 kHz, the phase margin is 69 degrees, and the gain margin is 14 dB.

Complete designs for several common output voltages, at f_{SW} of 425 kHz, 1 MHz, and 2 MHz are provided in Table 3 on page 34.

A GENERALIZED TUNING PROCEDURE

This section presents a methodology to systematically apply the design considerations provided above.

1. Choose the system bandwidth (f_C). This is the frequency at which the magnitude of the gain crosses 0 dB. Recommended values for f_C, based on the PWM switching frequency, are in the range $f_{SW} / 20 < f_C < f_{SW} / 7.5$. A higher value of f_C generally provides a better transient response, while a lower value of f_C generally makes it easier to obtain higher gain and phase margins.

2. Calculate the R_Z resistor value. This sets the system bandwidth (f_C):

$$R_Z = f_C \times \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times C_{OUT}}{g_{mPOWERx} \times g_m} \quad (34)$$

3. Determine the frequency of the pole (f_{P1}). This pole is formed by C_{OUT} and R_L. Use equation 28 (repeated here):

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

$$f_{P1} = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

4. Calculate a range of values for the C_Z capacitor. Use the following:

$$\frac{4}{2\pi \times R_Z \times f_C} < C_Z < \frac{1}{2\pi \times R_Z \times 1.5 \times f_{P1}} \qquad (35)$$

To maximize system stability (that is, to have the greatest gain margin), use a higher value of C_Z. To optimize transient recovery time, although at the expense of some phase margin, use a lower value of C_Z.

Figure 23 compares the output voltage recovery time due to a 1 A load transient for the system shown in Figure 22 (f_{Z2} = 3.8 kHz, 69° phase margin) and a system with f_{Z2} at $^1/_4$ the crossover frequency (15 kHz). The system with f_{Z2} at 15 kHz has 60° of phase margin, but recovers much faster (≈3×) than the other system.

5. Calculate the frequency of the ESR zero (f_{Z1}) formed by the output capacitor(s). Use equation 29 (repeated here):

$$f_{Z1} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

If f_{Z1} is at least one decade higher than the target crossover frequency (f_C) then f_{Z1} can be ignored. This is usually the case for a design using ceramic output capacitors. Use equation 33 to calculate the value of CP by setting f_{P3} to either 5 × f_C or f_{SW} / 2, whichever is higher.

Alternatively, if f_{Z1} is near or below the target crossover frequency (f_C), then use equation 33 to calculate the value of CP by setting f_{P3} equal to f_{Z1}. This is usually the case for a design using high ESR electrolytic output capacitors.

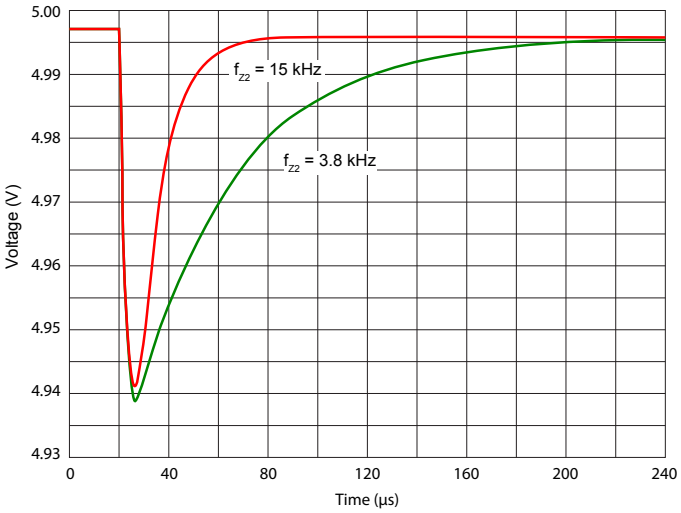


Figure 23: Transient Recovery Comparison for f_{Z2} at 3.8 kHz/69° and 15 kHz/60°

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 3: Recommended Component Values

V_{OUT} (V)	f_{SW} (MHz)	R_{FSET} (kΩ)	L_O (µH)	C_O[2] (µF)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	C_{FB} (pF)	$R_Z + C_Z // C_P$			BIAS Pin	Modes
								R_Z (kΩ)	C_Z (pF)	C_P (pF)		
1.5[1]	0.425	59.0	3.3	80	63.4 +3.83	76.8	N/A	24.3	560	15	3.3 V EXT	PWM and PFM
3.3			8.2	40	147	47.0	10	26.1	560	15	Connected to VOUT	PWM and PFM
5.0			10	50	221 + 0.499	42.2	8	49.9	270	8	Connected to VOUT	PWM and PFM
6.5			15	60	287 +6.5	41.2	6	78.7	180	4.7	3.3 V or 5.0 V LDO	PWM and PFM
3.3	1	23.7	3.3	20	147	47.0	10	18.2	560	15	Connected to VOUT	PWM and PFM
5.0			4.7	30	221 + 0.499	42.2	8	41.2	270	8	Connected to VOUT	PWM and PFM
6.5			6.8	40	287 +6.5	41.2	6	71.5	180	4.7	3.3 V or 5.0 V LDO	PWM and PFM
3.3	2	10.5	1.5	10	147	47.0	10	11.5	680	15	Connected to VOUT	PWM and PFM
5.0			2.2	15	221 + 0.499	42.2	8	26.1	330	8	Connected to VOUT	PWM and PFM
6.5			3.3	20	287 +6.5	41.2	6	45.3	180	4.7	3.3 V or 5.0 V LDO	PWM and PFM

[1]If BIAS is not connected to V_{OUT}, then the minimum external load must be ≥75 µA at all temperatures. No load operation is okay at approximately 25°C to 75°C only.
[2]Negative tolerance and DC-bias effect must be considered when choosing components to obtain C_O.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Power Dissipation and Thermal Calculations

The power dissipated in the A8589 is the sum of the power dissipated from the V_{IN} supply current (P_{IN}), the power dissipated due to the switching of the high-side power MOSFET (P_{SW}), the power dissipated due to the rms current being conducted by the high-side power MOSFET (P_{COND}), and the power dissipated by the gate driver (P_{DRIVER}).

The power dissipated from the V_{IN} supply current can be calculated using the following equation:

$$P_{IN} = V_{IN} \times I_Q + (V_{IN} - V_{GS}) \times Q_G \times f_{SW} \quad (36)$$

where

V_{IN} is the input voltage,

I_Q is the input quiescent current drawn by the A8589 (nominally 2.5 mA),

V_{GS} is the MOSFET gate drive voltage (typically 5 V),

Q_G is the MOSFET gate charge (approximately 2.5 nC), and

f_{SW} is the PWM switching frequency.

The power dissipated by the high-side MOSFET during PWM switching can be calculated using the following equation:

$$P_{SW} = \frac{V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}}{2} \quad (37)$$

where

V_{IN} is the input voltage,

I_{OUT} is the regulator output current,

f_{SW} is the PWM switching frequency, and

t_r and t_f are the rise and fall times measured at the SW node.

The exact rise and fall times at the SW node depend on the external components and PCB layout so each design should be measured at full load. Approximate values for both t_r and t_f range from 10 to 15 ns.

The power dissipated by the internal high-side MOSFET while it is conducting can be calculated using the following equation:

$$P_{COND} = I^2_{rms(FET)} \times R_{DS(on)HS} = \left(\frac{V_{OUT}+V_f}{V_{IN}+V_f}\right) \times \left(I^2_{OUT} + \frac{\Delta I_L^2}{12}\right) \times R_{DS(on)HS} \quad (38)$$

where

I_{OUT} is the regulator output current,

ΔI_L is the peak-to-peak inductor ripple current,

$R_{DS(on)HS}$ is the on-resistance of the high-side MOSFET, and

V_f is the forward voltage of the asynchronous diode.

The $R_{DS(on)}$of the high-side MOSFET has some initial tolerance plus an increase from self-heating and elevated ambient temperatures. A conservative design should accommodate an $R_{DS(on)}$ with at least a 15% initial tolerance plus 0.39%/°C increase due to temperature.

The sum of the power dissipated by the internal gate driver can be calculated using the following equation:

$$P_{DRIVER} = Q_G \times V_{GS} \times f_{SW} \quad (39)$$

where

V_{GS} is the gate drive voltage (typically 5 V),

Q_G is the gate charge to drive MOSFET to V_{GS} = 5 V (about 2.5 nC), and

f_{SW} is the PWM switching frequency.

Finally, the total power dissipated (P_{TOTAL}) is the sum of the previous equations:

$$P_{TOTAL} = P_{IN} + P_{SW} + P_{COND} + P_{DRIVER} \quad (40)$$

The average junction temperature can be calculated with the following equation:

$$T_J = P_{TOTAL} + R_{\theta JA} + T_A \quad (41)$$

where P_{TOTAL} is the total power dissipated as described in equation 40, $R_{\theta JA}$ is the junction-to-ambient thermal resistance (34°C/W on a 4-layer PCB), and T_A is the ambient temperature.

The maximum junction temperature will be dependent on how efficiently heat can be transferred from the PCB to ambient air. It is critical that the thermal pad on the bottom of the IC should be connected to a at least one ground plane using multiple vias.

As with any regulator, there are limits to the amount of heat that can be dissipated before risking thermal shutdown. There are tradeoffs between: ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, airflow, and other nearby heat sources. Even a small amount of airflow will reduce the junction temperature considerably.

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PCB Component Placement and Routing

A good PCB layout is critical if the A8589 is to provide clean, stable output voltages. Follow these guidelines to insure a good PCB layout. Figure 24 shows a typical buck converter schematic with the critical power paths/loops. Figure 25 shows an example PCB component placement and routing with the same critical power paths/loops as shown in the schematic.

1. By far, the highest di/dt in the asynchronous buck regulator occurs at the instant the high-side MOSFET turns on and the capacitance of the asynchronous Schottky diode (200 to 1000 pF) is quickly charged to V_{IN}. The ceramic input capacitors must deliver this fast, short pulse of current. Therefore, the loop, from the ceramic input capacitors through the high-side MOSFET and into the asynchronous diode to ground, must be minimized. Ideally these components are all connected using only the top metal layer (that is, do not use vias to other power/signal layers).

2. When the high-side MOSFET is on, current flows from the input supply and capacitors, through the high-side MOSFET, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces.

3. When the high-side MOSFET is off, free-wheeling current flows from ground, through the asynchronous diode, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces.

4. The voltage on the SW node transitions from 0 V to V_{IN} very quickly and is the root cause of many noise issues. It is best to place the asynchronous diode and output inductor close to the A8589 to minimize the size of the SW polygon. Also, keep low level analog signals (like FB and COMP) away from the SW polygon.

5. Place the feedback resistor divider (RFB1 and RFB2) very close to the FB pin. Ground this resistor divider as close as possible to the A8589.

6. To have the highest output voltage accuracy, the output voltage sense trace (from VOUT to RFB1) should be connected as close as possible to the load.

7. Place the compensation components (RZ, CZ, and CP) as close as possible to the COMP pin. Place vias to the GND plane as close as possible to these components.

8. Place the soft start capacitor (C_{SS}) as close as possible to the SS pin. Place a via to the GND plane as close as possible to this component.

9. Place the boot strap capacitor (CBOOT) near the BOOT pin and keep the routing from this capacitor to the SW polygon as short as possible.

10. When connecting the input and output ceramic capacitors, use multiple vias to GND and place the vias as close as possible to the pads of the components.

11. To minimize PCB losses and improve system efficiency, the input and output traces should be as wide as possible and be duplicated on multiple layers, if possible.

12. To improve thermal performance, place multiple vias to the GND plane around the anode of the asynchronous diode.

13. The thermal pad under the A8589 must connect to the GND plane using multiple vias. More vias will ensure the lowest junction temperature and highest efficiency.

14. EMI/EMC issues are always a concern. Allegro recommends having component locations for an RC snubber from SW to ground. The resistor should be 1206 size.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

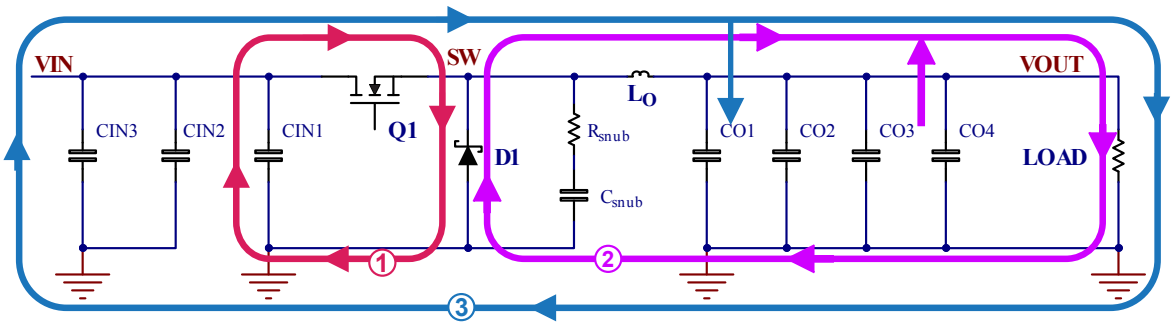


Figure 24: Typical Buck Converter with Critical Paths/Loops Shown

Loop 1 (red). At the instant Q1 turns on, Schottky diode D1, which is very capacitive, must be very quickly shut off (only 5 to 15 ns of charging time). This spike of charging current must come from the local input ceramic capacitor, CIN1. This spike of current is quite large and will be an EMI/EMC issue if loop 1 (red) is not minimized. Therefore, the input capacitor CIN1 and Schottky diode D1 must be placed be on the same (top) layer, be located near each other, and be grounded at virtually the same point on the PCB.

Loop 2 (magenta). When Q1 is off, free-wheeling inductor current must flow from ground through diode D1 (SW will be at $-V_f$), into the output inductor, out to the load and return via ground. While Q1 is off, the voltage on the output capacitors decreases. The output capacitors and Schottky diode D1 should be placed on the same (top) layer, be located near each other, and be sharing a good, low inductance ground connection.

Loop 3 (blue). When Q1 is on, current will flow from the input supply and input capacitors through the output inductor and into the load and the output capacitors. At this time, the voltage on the output capacitors increases.

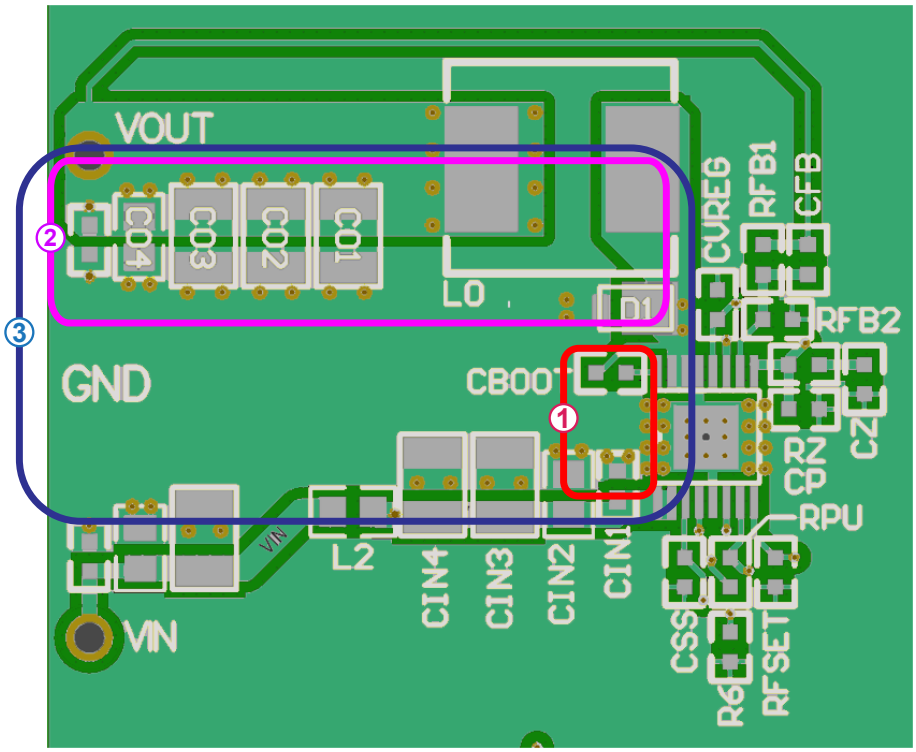


Figure 25: Example PCB Component Placement and Routing

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

TYPICAL APPLICATIONS SCHEMATICS

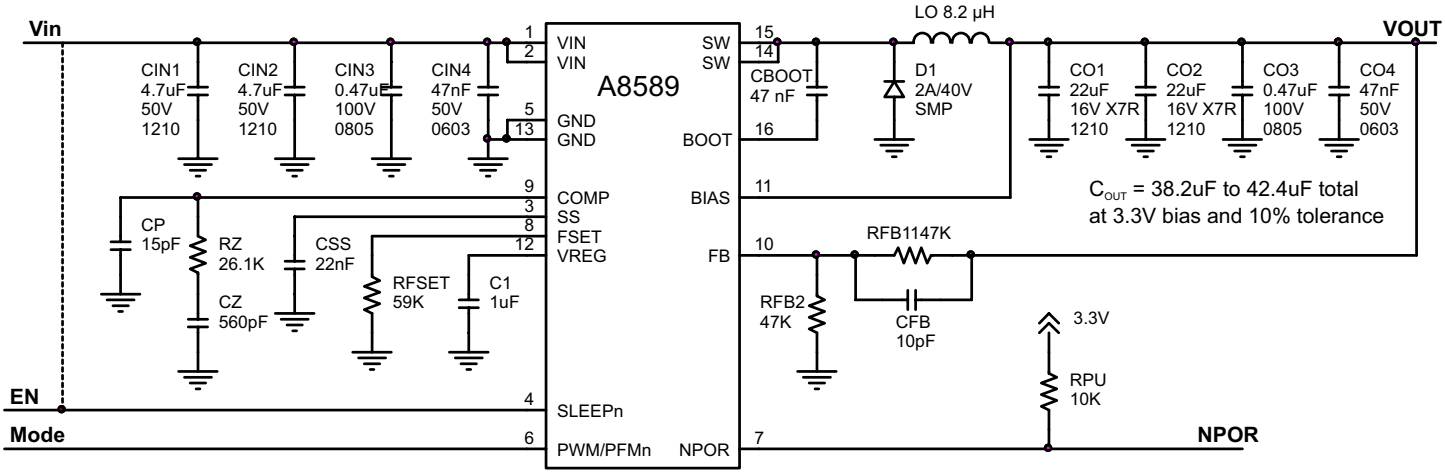


Figure 26: Typical Application Schematic A. Configuration for V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 2.5 A at 425 kHz

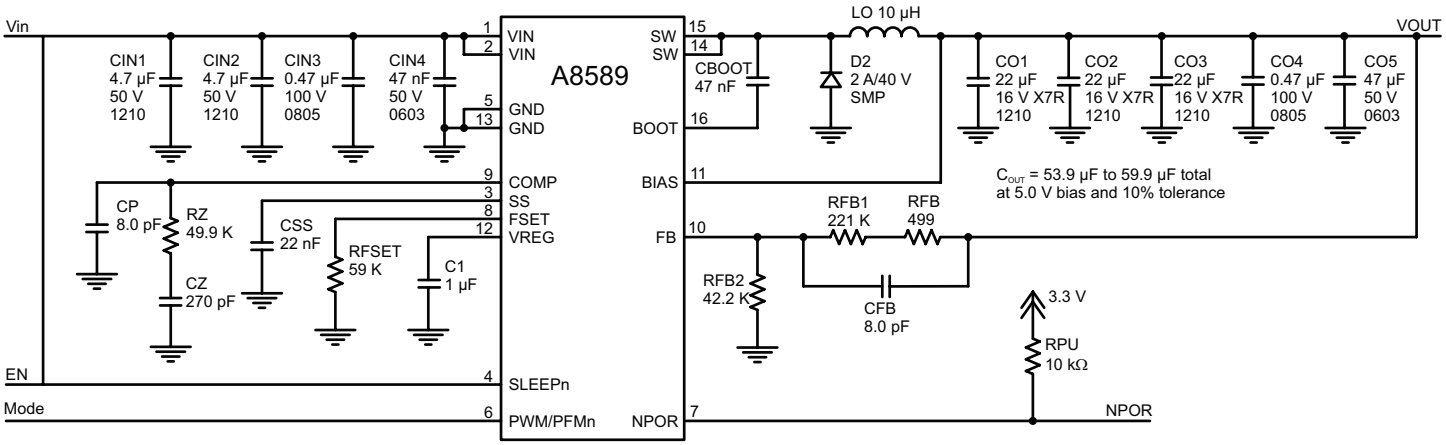


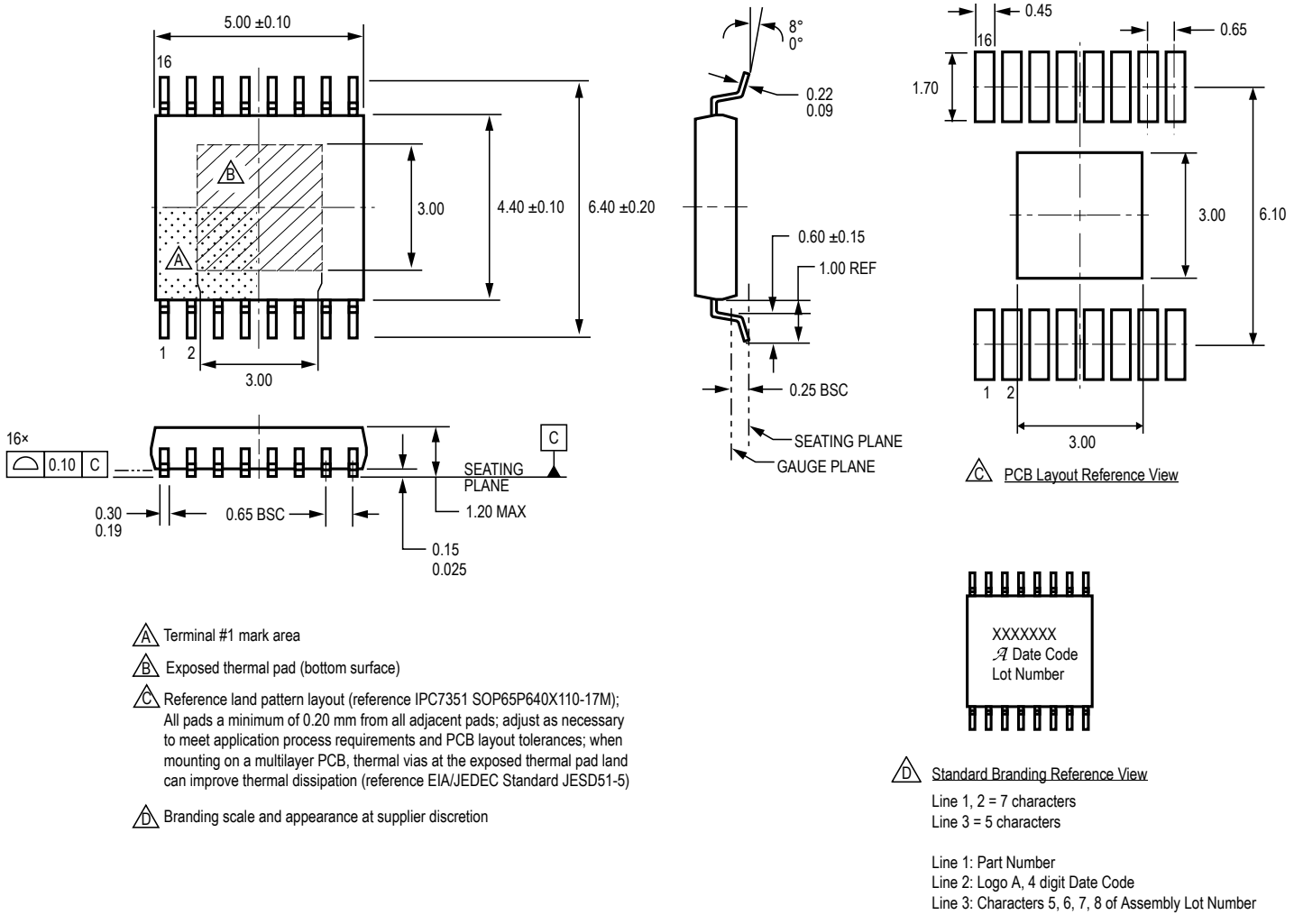
Figure 27: Typical Application Schematic B. Configured for V_{IN} = 12 V, V_{OUT} = 5.0 V, I_{OUT} = 2.5 A at 425 kHz

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Package Outline Drawing

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153 ABT; Allegro DWG-0000379, Rev. 3)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View

Line 1, 2 = 7 characters
Line 3 = 5 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 28: Package LP, 16-Pin TSSOP with Exposed Thermal Pad

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
1	September 9, 2014	Revised equation 8 on p. 26
2	February 11, 2015	Revised Table 2 and PWM Base Frequency section
3	May 4, 2020	Minor editorial updates
4	April 28, 2022	Updated package drawing (page 39)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com