Application Information

APS11900 Programming Guide

Introduction

The APS11900 is a two-wire programmable Hall-effect switch/latch IC. It is shipped in a unlocked state, allowing the end user to configure operation modes, switch points, and other settings. This document describes two approaches to programming the APS11900 and should be used as a companion to the product datasheet. The datasheet contains important device-specific information not contained within this guide.

Getting Started

Before programming and locking the APS11900 EEPROM, the user must determine how the sensor should be configured. The following six items should be defined before attempting to program the EEPROM. Reference the datasheet when choosing settings for items 1 through 5.

Available configuration settings:

1. Operation switch mode: Unipolar, Omnipolar, or Latch modes (refer to the datasheet for a complete description of each mode)
2. Magnetic Polarity: North or South Pole sensitive (not applicable for omnipolar mode)
3. Output Polarity: high or low asserted when B_{OP} threshold is reached
4. Output Low I_{CC} level: I1 or I2 range options (see datasheet for $I_{CC(L)}$ specifications)
5. Temperature Compensation (TC) determined by choice of magnetic material
6. Magnetic switch points, B_{OP}, B_{RP}, B_{HYS} (see "Using Shadow Registers to Tune Magnetic Switch Point Settings")

A flowchart outlining the sequence for programming the APS11900 is provided in Figure 1.

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For parameters not listed in this programming guide, refer to the product datasheet (APS11900). In the event of a conflict between this document and the datasheet, the datasheet takes precedence.

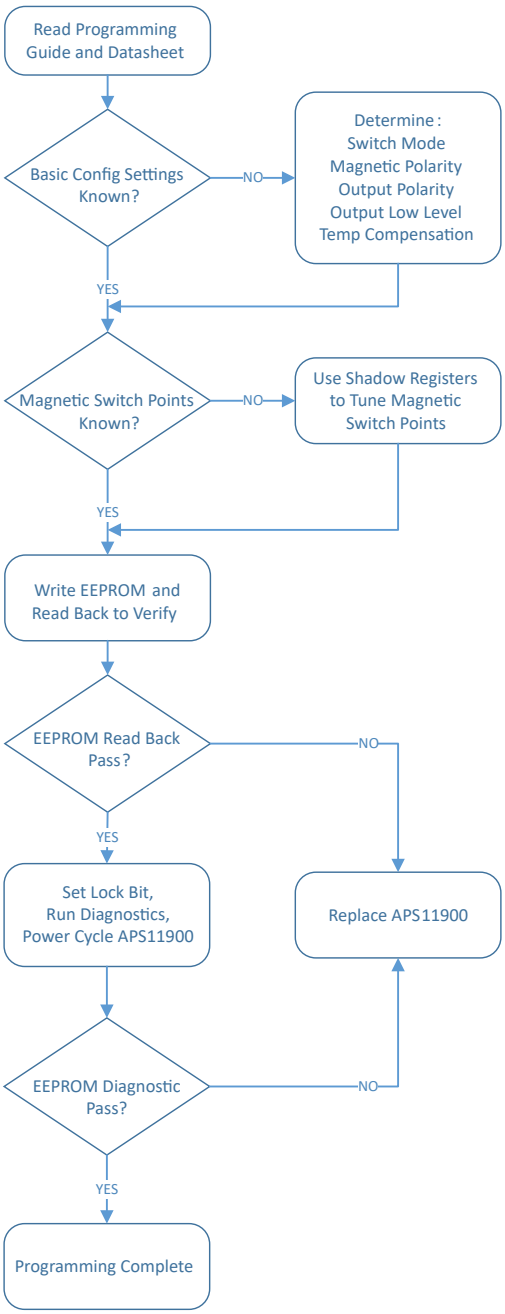

Figure 1: APS11900 Programming Flowchart

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Programming Overview

The APS11900 family allows the user to write to volatile configuration registers, called “Shadow” registers, to “Try” the configuration; then the device configuration can be written to nonvolatile EEPROM memory. “Shadow” registers are reset to default values by cycling the supply voltage. The APS11900 EEPROM allows for a maximum of 100 write cycles and for this reason it is recommended to first use the shadow registers to determine the correct device configuration prior to writing to the EEPROM. After the desired device configuration has been determined, write the values into the device EEPROM and set the lock bit to prevent further access to the EEPROM.

There are two available approaches for programming the APS11900. The first is to use the Allegro Sensor Evaluation Kit (ASEK-20) which includes both hardware and software needed to quickly and easily program the APS11900. This approach is ideal for lab evaluation and prototyping new designs; however, this approach may not be suitable for production volume programming. The second approach is to create custom hardware drivers and hardware for programming the APS11900. The second approach is not practical for device evaluation or prototyping, but may be preferred for in-line production programming where throughput and efficiency are essential. This programming guide covers both of these methods.

Whether using the ASEK-20 or a custom manufacturing solution, programming is accomplished by sending a series of input voltage pulses serially through the VCC pin of the device. A unique combination of different voltage pulses control the internal programming logic of the device to select a desired programmable parameter and change its value. There are four voltage levels used for programming. These levels are referred to as high (V_{PH}), mid (V_{PM}), low (V_{PL}), and an EEPROM writing pulse voltage (V_{PP}). A summary description of the available programming operations described in this document is provided in Table 1 below.

Table 1: Programming Operations

Function	Description
Shadow Register Write	Write volatile configuration registers in “Try” Mode.
Shadow Register Read	Read volatile configuration registers in “Try” Mode.
Shadow Register Increment BOP	This mode allows the user to increment BOPSEL each time a PH pulse is sent.
Shadow Register Decrement BOP	This mode allows the user to decrement BOPSEL each time a PH pulse is sent.
Shadow Register Increment HYS	This mode allows the user to increment the HYS code by one bit each time a PH pulse is sent.
Shadow Register Decrement HYS	This mode allows the user to decrement the HYS code by one bit each time a PH pulse is sent.
EEPROM Register Write	Write configuration to nonvolatile memory (EEPROM). Note that EEPROM has limited write cycles as described in the Absolute Maximum Specifications table.
EEPROM Register Read	Read nonvolatile configuration registers (EEPROM).
EEPROM Margining	Procedure to validate that the EEPROM bank was written successfully.

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Volatile “Shadow” Register Map

The APS11900 contains volatile shadow registers which allow the user to try different settings to determine the correct configuration before writing the final value to the EEPROM. Reading or writing Shadow registers is only possible prior to locking the device. The customer-accessible Shadow registers are shown below in Table 2. Each register is 16 bits wide and contains multiple fields.

Table 2: Volatile “Shadow” Register Map

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHADOW 0x0C	x*	x*	x*	x*	x*	x*	TCSEL		BOPSEL							
SHADOW 0x0D	x*	x*	x*	x*	x*	x*	ICCL	BOPPOL	UNI	LATCH	POL	HYS				

* Grayed out “x” bits are restricted to Allegro internal use only; these bits should always be written as digital 0s; on readback, these bits might appear as either digital 0s or 1s.

Nonvolatile EEPROM Register Map

This table describes the programmable bits within the three customer-accessible nonvolatile EEPROM registers. Each register is 16 bits wide and contains several fields.

Table 3: Nonvolatile EEPROM Register Map

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EEPROM 0x04	x*	x*	x*	x*	x*	LOCK	TCSEL		BOPSEL							
EEPROM 0x05	x*	x*	x*	x*	x*	x*	ICCL	BOPPOL	UNI	LATCH	POL	HYS				
EEPROM 0x06	x*	x*	x*	x*	x*	x*	CUSTID									

* Grayed out “x” bits are restricted to Allegro internal use only; these bits should always be written as digital 0s; on readback, these bits might appear as either digital 0s or 1s.

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Register Field Descriptions

The following table provides a description of each of the defined register fields accessible in both volatile and nonvolatile device memory locations.

Table 4: Detailed Register Field Descriptions

<table>
<tr><th>Register</th><th>Register Description</th><th># of Bits</th><th>Programmable Options</th></tr>
<tr><td>BOPSEL</td><td>Sets the operating point, B_{OP}</td><td>8</td><td>Decimal 0 = B_{OP} (≤ ±10) and decimal 255 = B_{OP} (≥ ±600). Threshold is adjusted with an average of 3 G per bit.</td></tr>
<tr><td>TCSEL</td><td>Select the TC</td><td>2</td><td>00: Flat
01: SmCo
10: NdFeB
11: Ferrite</td></tr>
<tr><td>LOCK</td><td>Permanently lock registers 0x04, 0x05, and 0x06</td><td>1</td><td>Set this bit after the device configuration has been written to EEPROM. If this bit is set, communication (EEPROM and shadow) with the APS11900 is disabled after the next power-on reset. Once locked, the APS11900 cannot be unlocked; for this reason, it is important to keep the APS11900 powered with 5 V or greater while validating the configuration is correct through readback and the auto-margining diagnostic processes.</td></tr>
<tr><td>HYS</td><td>Set the hysteresis, B_{HYS}.
Note: In Latch mode, this configuration is not used (B_{RP} = –B_{OP})</td><td>5</td><td>Decimal 0 = HYS (≤ 15 G) and decimal 255 = HYS (≥ 70 G). Hysteresis is adjusted with an average of 3 G per bit.</td></tr>
<tr><td>POL</td><td>Sets the polarity of the output current</td><td>1</td><td>0: $I_{CC(L)}$ when B_{OP} threshold exceeded (default)
1: $I_{CC(H)}$ when B_{OP} threshold exceeded</td></tr>
<tr><td>LATCH</td><td>Sets device in latch mode</td><td>1</td><td rowspan="2"><table><tr><th colspan="2">Bit</th><th rowspan="2">Description</th></tr><tr><th>UNI</th><th>LATCH</th></tr><tr><td>0</td><td>X</td><td>Omnipolar Switch</td></tr><tr><td>1</td><td>0</td><td>Unipolar Switch (default)</td></tr><tr><td>1</td><td>1</td><td>Latch</td></tr></table></td></tr>
<tr><td>UNI</td><td>Sets device in unipolar mode</td><td>1</td></tr>
<tr><td>BOPPOL</td><td>Sets magnetic polarity</td><td>1</td><td>0: South Polarity (default)
1: North Polarity</td></tr>
<tr><td>ICCL</td><td>Selects Output Current Low level</td><td>1</td><td>0: ICCL = ICCL2
1: ICCL = ICCL1 (default)</td></tr>
</table>

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Using Shadow Registers to Tune Magnetic Switch Point Settings

After choosing sensor configuration settings 1 through 5, use the following steps to determine the magnetic switch points in the target application.

1. At room temperature, present the magnetic field level at the desired polarity to the sensor.
2. With the B field present, increment or decrement the default B_{OP} value using the shadow register ("Try" mode) until the output switches to the defined on state and take note of the resultant register value for B_{OP}.
3. Determine the desired B_{HYS} based on the application needs and magnetic characteristics.
4. With the B field present, increment or decrement the HYS setting until the desired performance is achieved and take note of the final HYS register value.
5. B_{RP} is automatically determined by the sensor using the following relationship: $B_{RP} = (B_{OP} – B_{HYS})$ value.

Once these steps are completed, record the chosen volatile Shadow register values in preparation for programming the EEPROM. The following sections explain the mechanics of how to read and program the Shadow memory.

Note: As an alternative to the procedure outlined, devices can be blind-blown to a fixed B_{OP} code so that programming can be achieved quickly and without the presence of a magnetic field. This method requires the user to perform a statistical analysis to determine the fixed code, due to the code-to-field level variability from part to part, and to validate appropriate function at end of line. This method will also result in the widest switch point variability.

Volatile "Shadow" Memory Programming Procedure

1. Power on device with V_{CC} = 5 V.
2. Configure the APS11900 as unipolar north, unipolar south, or omnipolar switch or latch, $I_{CC(L)}$ value, output polarity in Shadow Register 0x0D, following the sequence described in Writing Shadow Registers section.
3. Configure temperature coefficient in Shadow Register 0x0C, following the sequence described in Writing Shadow Registers section.
4. If the target switch point is higher than the APS11900 default B_{OP} (see datasheet), then write the new value into BOPSEL. The final value can be tuned for the application using the Increment and Decrement BOP modes as described in the Increment BOP Test Mode and Decrement BOP Test Mode sections.
5. If target hysteresis is outside the default range specified in the APS11900 datasheet, then write a new HYS value to Shadow Register 0x0C. Note that this can be trimmed for the application using Increment and Decrement Hysteresis modes if desired as described in the Increment HYS Test Mode and Decrement HYS Test Mode sections.

Nonvolatile EEPROM Memory Programming Procedure

1. First complete steps 1 through 5 as outlined in the section Volatile "Shadow" Memory Programming Procedure to determine optimal switching points and corresponding register settings.
2. Without removing power, duplicate the volatile register settings in EEPROM.
   A. Write value from Shadow Register 0x0D to EEPROM 0x05 as described in the Writing to EEPROM section.
   B. Write value from Shadow Register 0x0C to EEPROM 0x04 as described in the Writing to EEPROM section.
   C. Read back EEPROM 0x04 and 0x05 and confirm the values are correct as described in the Reading EEPROM section.
3. Confirm switch points are as desired for the application.
4. Write the LOCK bit in EEPROM register 0x04. (Take current EEPROM 0x04 value and logically OR 0x0400 and write EEPROM 0x04) as described in the Writing to EEPROM section. Read back EEPROM 0x04 and 0x05 and confirm the values are correct as described in the Reading EEPROM section.
5. Run the onboard EEPROM diagnostic to verify adequate voltage pulses were used during the writing process by following the procedure outlined in the EEPROM Auto-Margining section.
6. Power cycle so that V_{CC} = 0 V and then V_{CC} is raised to 5 V.
7. Confirm EEPROM cannot be read back by performing an EEPROM Read operation as described in the Reading EEPROM section.

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Interpreting the Auto-Margining Diagnostic results

The results of the EEPROM margining can be interpreted as shown in Table 5:

Table 5: EEPROM Margining Results Key

Bit 4	Bit 3	Status	Recommended Action
0	0	N/A	N/A
0	1	Pass	Set the LOCK bit and power cycle the APS11900.
1	0	Fail	Verify programming pulse voltages and repeat Write Programming sequence. If still returning fail after second attempt, replace with new APS11900 and repeat programming sequence.
1	1	Running	Diagnostic still running. Re-check results until Pass or Fail returned (Figure 23).

Once the final EEPROM margining results are complete and passing, the LOCK bit can be set. The APS11900 LOCK bit is set in EEPROM register 0x04. Once this bit is set, communication with the APS11900 will be disabled following the next power-on reset. For this reason, it is important to keep the APS11900 powered with 5 V or greater if the LOCK bit is set while validating the configuration is correct. Before powering down the DUT to 0 V, the user should read back the EEPROM registers and then run auto-margining to ensure the EEPROM configuration is valid.

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Programming using the Allegro ASEK-20

The ASEK-20 is a complete hardware and software package that can be used to quickly program the APS11900 and is ideally suited for engineering evaluation and system prototyping. The ASEK-20 includes a hardware interface board and a software GUI to quickly and easily read and write any of the available fields in both the volatile and nonvolatile registers of the APS11900. To order the ASEK-20 hardware, contact your local Allegro Sales representative for more information. Follow the link below to download the ASEK-20 user guide and software from Allegro's website.

https://www.allegromicro.com/en/Sample-And-Buy/Demo-Boards/ASEK-20-Sensor-Evaluation-Kit.aspx

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Building a Custom Programming Solution

Programming Protocol

The programming protocol for the APS11900 is a quick addressing system that uses commands comprised of medium and high voltage pulses. Portions of the programming sequence include binary-encoded words made up of PM pulses representing digital 0s and PH pulses representing digital 1s. The APS11900 has nine different programming modes as outlined in Table 1: Programming Operations. To configure the APS11900 for operation in any of these modes, a coded series of voltage pulses must be provided through the VCC pin. These voltage pulses are used to set bit fields in onboard Shadow and EEPROM registers. As long as the device remains unlocked, all user-accessible registers can be changed.

Note: Allegro can provide reference source code to facilitate creation of a device driver. A nondisclosure agreement must be signed. See your Allegro representative for details.

Programming Voltages

Four voltage levels are used in programming the device: a low-level voltage (V_{PL}), a mid-level voltage (V_{PM}), a high-level voltage (V_{PH}), and an EEPROM writing pulse voltage (V_{PP}). A fifth voltage level (V_{CL}, 0 V), is used to clear the registers and reset the sensor. Finally, a sixth voltage level (V_{MN}) is used for EEPROM margining. All pulse types and values are described in Table 6: Programming Voltage Characteristics and shown in Figure 2: Pulse Amplitudes and Durations.

Every programming pulse must be preceded and followed by a low voltage pulse V_{PL} to be recognized by the sensor. For example, to send a mid-level V_{PM} representing '0', followed by a high pulse VPH representing '1', the following must be supplied at the sensor VCC pin: 5 V → 12 V → 5 V → 19 V → 5 V. When programing the Shadow registers, it is important to know that these are volatile registers and will only retain information from a programming sequence as long as the device remains powered on.

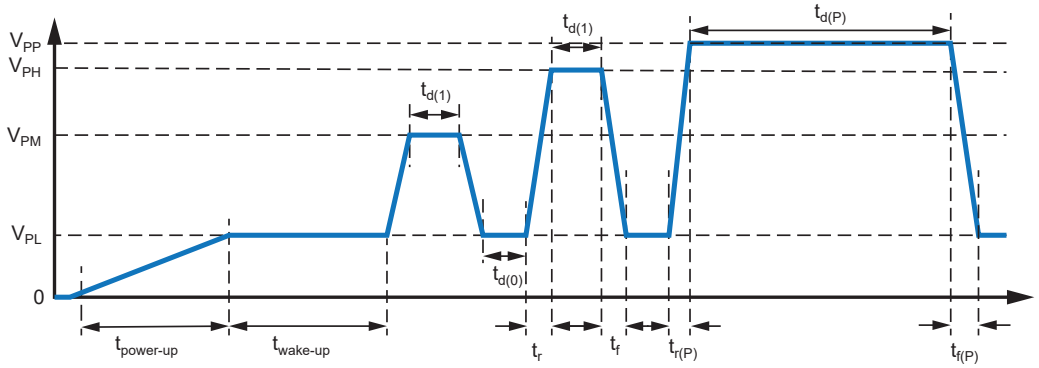

Figure 2: Pulse Amplitudes and Durations

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If a series resistor is used for current sensing, the resistor values should be kept as low as possible to reduce the voltage drop seen by the sensor. When programming the sensor in a system with a current sense resistor, the supply voltage amplitude must be increased to compensate for the voltage drop to ensure that the supply voltage provided to the sensor is within the values specified in Table 6: Programming Voltage Characteristics. In its general form, this relationship can be expressed as:

$$\Delta V_{CC} = R_{SERIES} \times I_{CC}, \text{ where } I_{CC} \text{ is defined by the output state of the sensor.}$$

If the sensor is being programmed in the presence of a magnetic field and the sensor is configured to output $I_{CC(H)}$ in this state, then $I_{CC(H)}$ max should be used in the above equation. Conversely, if the sensor is programmed without a magnetic field present, then $I_{CC(L)}$ max should be used in the equation. If using the UC package option, the internal 68 Ω must be added to the external current sense resistor when calculating ΔV_{CC}. To verify that the correct voltage levels are applied, refer to Figure 3: V_{PULSE} measurement location for each package type.

Finally, a bypass capacitor (C_{BYPASS}) with a minimum capacitance of 100 nF should be connected from VCC to GND of the device. The UC package option integrates this bypass capacitor, therefore the user does not need to add one.

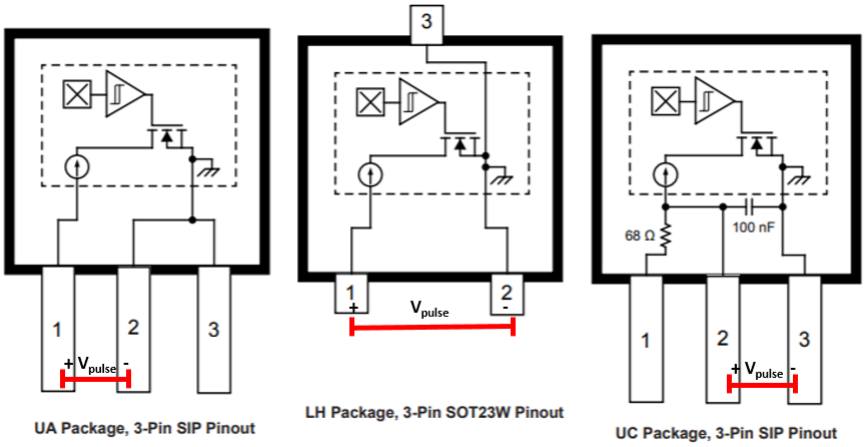

Figure 3: V_{PULSE} measurement location for each package type

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Table 6: Programming Voltage Characteristics

Characteristics	Symbol	Comment	Min.	Typ.	Max.	Unit
EEPROM Write Programming Voltage	V_{PP}	Measured at VCC pin of sensor IC (UA/LH) Measured at VINT pin of sensor IC (UC)	18.5	19	19.5	V
EEPROM Margining Voltage	V_{MN}	Measured at VCC pin of sensor IC	17.5	18	18.5	V
High Programming Voltage	V_{PH}	Measured at VCC pin of sensor IC	18.5	19	19.5	V
Mid Programming Voltage	V_{PM}	Measured at VCC pin of sensor IC	11.5	12	12.5	V
Low Programming Voltage *	V_{PL}	Measured at VCC pin of sensor IC	4.5	5.0	5.5	V
Pulse Width Off	$t_{d(0)}$	Off time between programming pulses	50	100	–	µs
Pulse Width On	$t_{d(1)}$	Pulse duration (on time) of programming pulses	50	100	–	µs
Pulse Rise Time	t_r	VPL-to-VPM and VPL-to-VPH	5	20	100	µs
Pulse Fall Time	t_f	VPM-to-VPL and VPH-to-VPL	5	20	100	µs
Pulse Width EEPROM Write	$t_{d(P)}$	Pulse duration (on time) of EEPROM write programming pulses	10	–	12	ms
Pulse Rise Time EEPROM Write	$t_{r(P)}$	VPL-to-VPP	500	–	2000	µs
Pulse Fall Time EEPROM Write	$t_{f(P)}$	VPP-to-VPL	100	–	1000	µs
Pulse Width EEPROM Margin	$t_{d(MN)}$	Pulse duration (on time) of EEPROM Margin pulse	1	–	2	ms
Power-Up Time	$t_{power-up}$	Time from 0 V to $V_{PL(min)}$	1	–	1000	µs
Wake-Up Time	$t_{wake-up}$	Time for device to initialize	1	–	–	ms

* V_{PL} represents the continuous low voltage level for device supply voltage; this level must be maintained during programming or else the programming sequence could be interrupted and/or volatile registers will become corrupted/cleared.

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Reading Volatile Shadow Registers

To read the Shadow registers, they must be first configured to be in read mode. Once the Shadow register has been put in read mode, individual registers can be addressed and read. The complete sequence is shown in Figure 4, Figure 5, and Figure 6. Figure 4 shows the pulse sequence used to configure the Shadow registers for read mode.

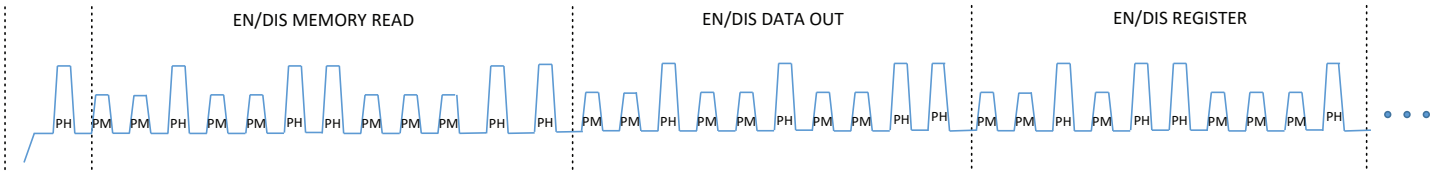

Figure 4: VCC Pulse Sequence to enter Volatile Shadow Registers Readback Mode

For the next step, use the pulse sequence in Figure 5 to address and read out data from individual registers. After each PH pulse is applied to VCC by the user, the APS11900 will send out one bit to be read. The data is sent as encoded current pulses on the output where digital 0s are represented by $I_{CC(L)}$ and digital 1s are represented by $I_{CC(H)}$. Reference the product datasheet for the specified $I_{CC(L)}$ and $I_{CC(H)}$ ranges.

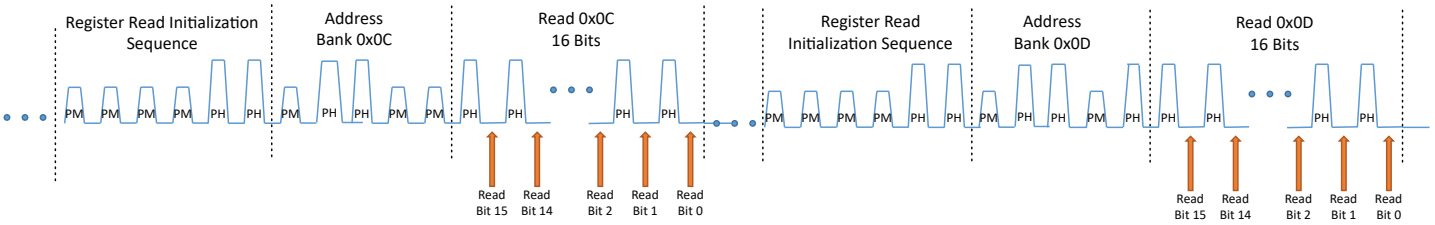

Figure 5: VCC Pulse Sequence to read back Shadow Register Data while in Readback Mode

Figure 6 shows the pulse sequence needed to exit readback mode. Alternatively, power cycling the sensor will also result in the sensor returning to default operation mode (as well as reset the Shadow register).

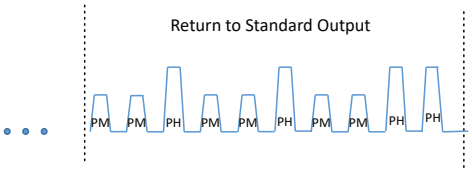

Figure 6: VCC Pulse Sequence to exit Shadow Register Readback Mode

Additional Information About Reading Shadow Registers

"EN/DIS MEMORY READ", "EN/DIS DATA OUT", and "EN/DIS REGISTER" can be thought of as functional toggle switches. When the device is sent, each of these pulse sequences reacts by toggling its state. After sending these three commands shown in Figure 4, the device is configured in Read mode. The device stays in Read mode until toggled OFF. When reading multiple registers sequentially, the pulse sequences shown in Figure 4 should only be sent one time. Figure 5 can be repeated for additional register reads. Read mode can be toggled OFF by resending the "EN/DIS MEMORY READ" sequence or by restarting the part.

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Writing Shadow Registers

The Shadow register write procedure consists of first enabling the register as shown in Figure 7, followed by write initialization, address and write pulses as shown in Figure 8. To write bits into the Shadow registers, an entire bank of 16 bits must be written at once. To perform the write, a sequence of initialization and addressing pulses must be applied to the VCC pin of the device and then the 16 desired bits must be entered into the device as a series of high-voltage (PH) and medium-voltage (PM) pulses, with PH pulses representing digital 1s and PM pulses representing digital 0s. Note all PM and PH pulses must be separated by a PL pulse to be recognized by the APS11900. The Re-Power pulse is only required after a power cycle; successive pulse sequences are permitted and do not require the Re-Power PH pulse if device power has been maintained throughout programming.

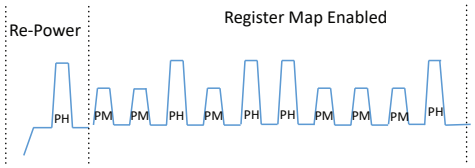

Figure 7: VCC Pulse Sequence to enable Shadow Registers

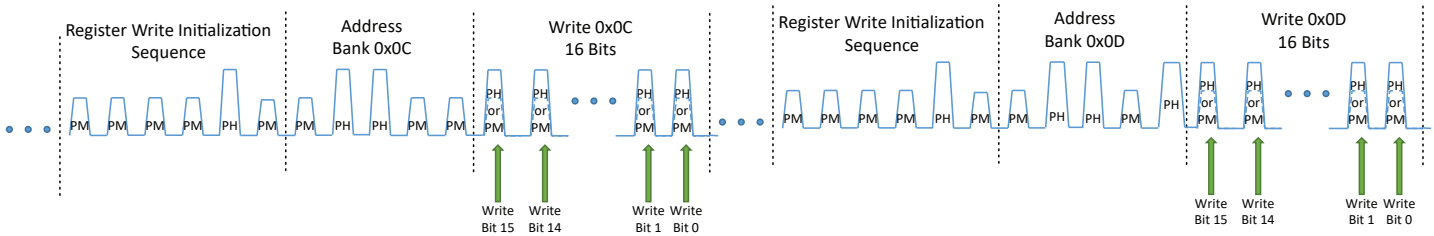

Figure 8: VCC Pulse Sequence to write data to Shadow Registers

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BOPSEL and HYS Tuning Modes

The APS11900 has tuning modes for the BOPSEL and HYS registers to facilitate fine tuning of the BOPSEL and HYS levels. This feature can be used during the prototyping phase to optimize switching thresholds prior to setting final codes. It can also be used during end-of-line production testing for applications that require each complete system to be custom tuned. The following sections describe the mechanics of how to fine tune the BOPSEL and HYS thresholds one LSB at a time.

HOW THE TUNING MODES FUNCTION

"Enable Increment" only needs to be turned on once after a Read or a device restart. After being toggled ON, it stays ON until toggled OFF. It can be toggled OFF by resending the "Enable Increment" sequence, restarting the part, or by performing a Read.

"Enable HYS Mode" mode only needs to be turned on once per device startup or following a device read. It can be toggled OFF by resending the "Enable HYS Mode" sequence, restarting the part, or by performing a Read. After initially toggling the "Enable HYS Mode" ON, the user can "Execute Increment/Decrement" and "Tuning Pules" as many times as needed until this mode is toggled OFF.

"Execute Increment/Decrement" will always increment or decrement the sensor depending on the state of the Enable Increment toggle switch.

The "Tuning Pulses" are a quick way of telling the APS11900 to repeat Increment or Decrement; however, they only work when immediately following the "Execute Increment/Decrement" sequence. This means that the first increment or decrement must always be from an "Execute Increment/Decrement" sequence.

Decrement BOPSEL Tuning Mode

The Decrement BOPSEL Tuning Mode decreases the BOPSEL register every time the "Execute Increment/Decrement" sequence is sent and additionally each time a subsequent "Tuning Pulse" is sent. At power-on, the APS11900 loads the EEPROM Bank 0x04 into 0x0C, setting the BOPSEL starting point. The example shown in Figure 9 starts after the APS11900 is powered on; thus a PH pulse is initially required. To start from a known BOPSEL, first follow the writing shadow register sequence given in Figure 7 and Figure 8, and then the sequence given in Figure 10. Note the only difference between Figure 9 and Figure 10 is that in Figure 9, the registers must be first enabled before moving into Tuning mode, whereas in Figure 10, it is assumed this first step was already performed when writing an initial value to the BOPSEL register.

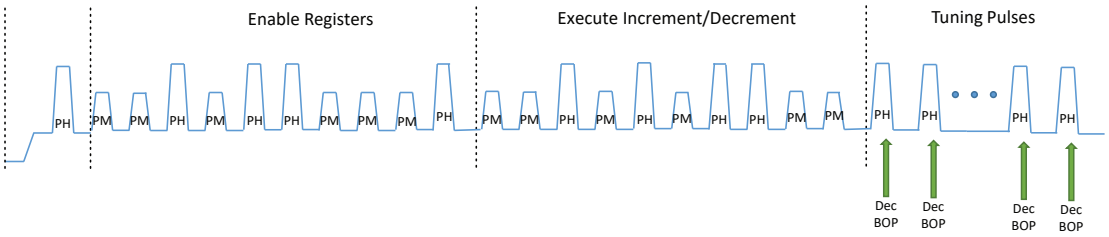

Figure 9: VCC Pulse Sequence to Decrement BOPSEL after Power Up

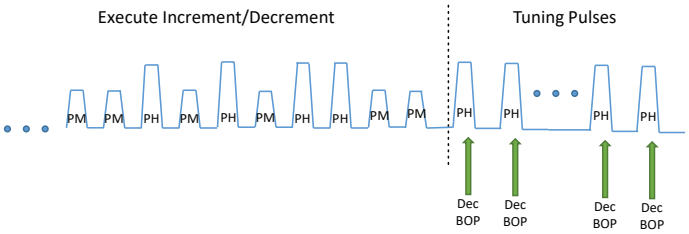

Figure 10: VCC Pulse Sequence to Decrement BOPSEL after Writing Shadow Registers

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Increment BOPSEL Register Tuning Mode

The Increment BOPSEL Tuning Mode increases the BOPSEL register every time the “Execute Increment/Decrement” sequence is sent and additionally each time a subsequent “Tuning Pulse” is sent. At power-on, the APS11900 loads the EEPROM Bank 0x04 into 0x0C, setting the BOPSEL starting point. The example shown in Figure 11 starts after the APS11900 is powered on. In the case where the device maintains power from a previous read/write command, the Re-Power PH pulse is not required and the sequence may begin with the enable registers command sequence.

To start from a specified BOPSEL level, first follow the sequence given in Figure 7 and Figure 8 to write in a value and then follow the sequence shown in Figure 12. Note the only difference between Figure 11 and 12 is that in Figure 11, the registers must be first enabled before moving into Increment and Tuning modes, whereas in Figure 12, it is assumed this first step was already performed when writing an initial value to the BOPSEL register.

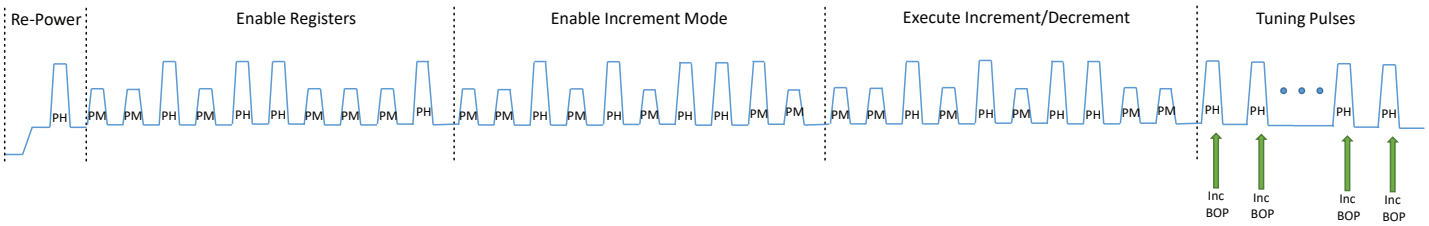

Figure 11: VCC Pulse Sequence to Increment BOPSEL after Power Up

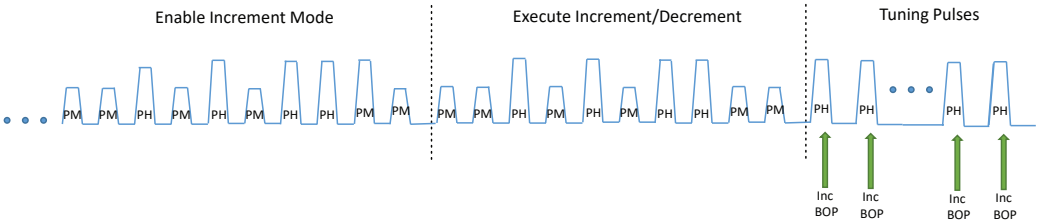

Figure 12: VCC Pulse Sequence to Increment BOPSEL after Writing Shadow Registers

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Decrement HYS Register Tuning Mode

The Decrement HYS Tuning Mode decreases the HYS register every time the “Execute Increment/Decrement” sequence is sent and additionally each time a subsequent “Tuning Pulse” is sent. At power-on, the APS11900 loads the EEPROM Bank 0x05 into 0x0D, setting the HYS starting point. The example shown in Figure 13 starts after the APS11900 is powered on as noted by the inclusion of an initial PH pulse. To start from a known HYS setting, first follow the sequence given in Figure 7 and Figure 8, and then the sequence given in Figure 14. Note the only difference between Figure 13 and Figure 14 is that in Figure 13, the registers must be first enabled before moving into Increment and Tuning modes, whereas in Figure 14, it is assumed this first step was already performed when writing an initial value to the HYS register.

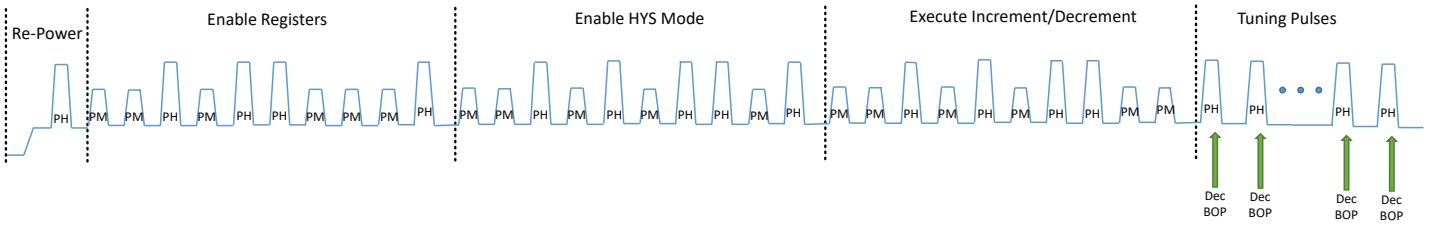

Figure 13: VCC Pulse Sequence to Decrement HYS after Power Up

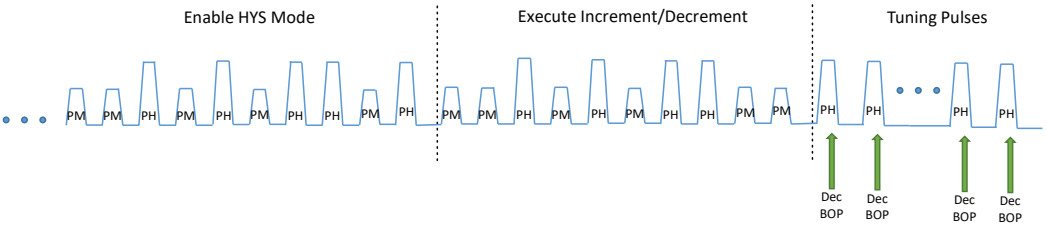

Figure 14: VCC Pulse Sequence to Decrement HYS after Writing Shadow Registers

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Increment HYS Tuning Mode

The Increment HYS Tuning Mode increases the HYS register every time the “Execute Increment/Decrement” sequence is sent and additionally each time a subsequent “Tuning Pulse” is sent. At power-on, the APS11900 loads the EEPROM Bank 0x05 into 0x0D, setting the HSY starting point. The example shown in Figure 15 starts after the APS11900 is powered on. To start from a known HYS setting, first follow the sequence given in Figure 7 and Figure 8, and then the sequence given in Figure 16. Note the only difference between Figure 15 and Figure 16 is that in Figure 15, the registers must be first enabled before moving into Increment and Tuning modes, whereas in Figure 16, it is assumed this first step was already performed when writing an initial value to the HYS register.

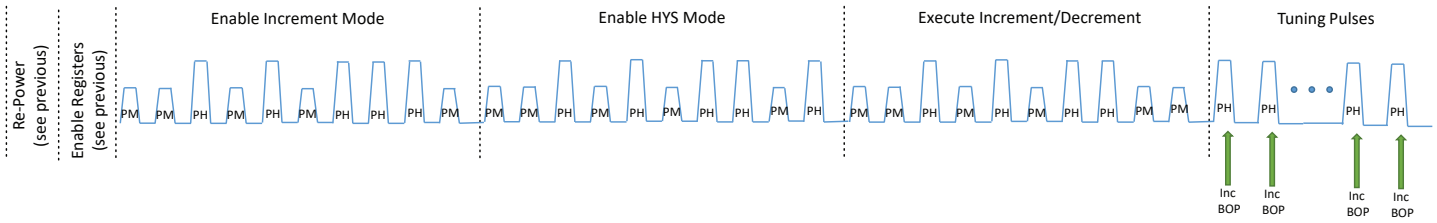

Figure 15: VCC Pulse Sequence to Increment HYS after Power Up

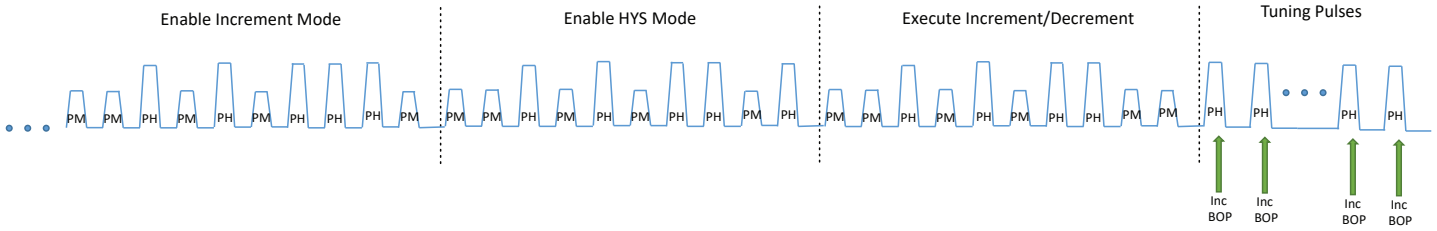

Figure 16: VCC Pulse Sequence to Increment HYS after Writing Shadow Registers

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Reading EEPROM

To read back bits from EEPROM registers, a sequence of initialization and addressing pulses must be applied to the VCC pin of the device and then the 16 bits must be sequenced out as current pulses between high-voltage (PH) pulses. The programming sequence required to read the 0x04 EEPROM bank after a re-power, including the initialization sequence, is shown below in Figure 17. Entering readback mode without having power-cycled the device, such as after completing an EEPROM write, is achieved by skipping the initial Re-Power PH pulse. Figure 17 and Figure 18 show the sequence to read the EEPROM addresses 0x05 and 0x06 following the initialization sequence shown in Figure 17. After each PH pulse is applied to VCC by the user, the APS11900 will send out one bit to be read. Digital 0s are represented by $I_{CC(L)}$ and digital 1s are represented by $I_{CC(H)}$. Reference the product datasheet for the specified $I_{CC(L)}$ and $I_{CC(H)}$ ranges. This process is illustrated in Figure 18.

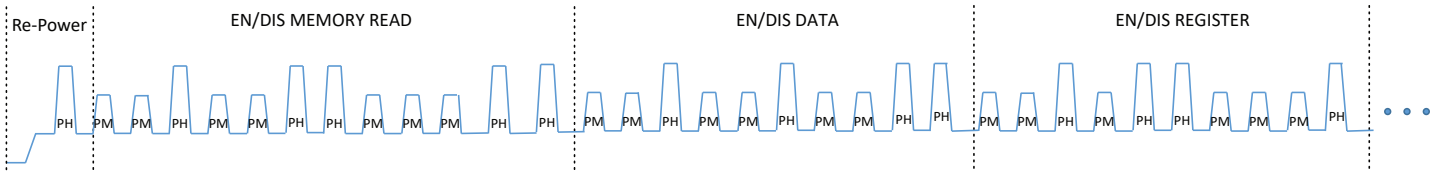

Figure 17: VCC Pulse Sequence to enter EEPROM Readback Mode

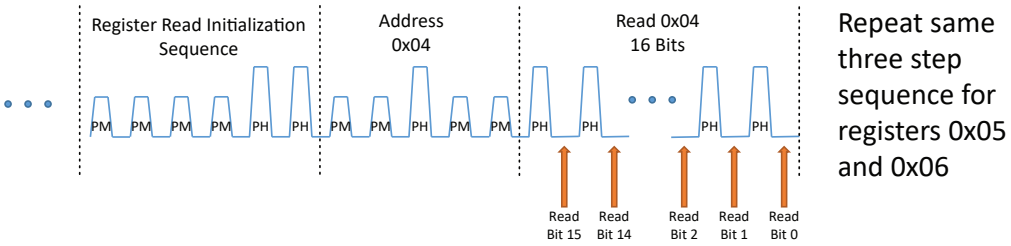

Figure 18: VCC Pulse Sequence to Read back EEPROM while in Readback Mode

There are two ways to exit EEPROM read mode to return the output back to standard mode where I_{CC} is used to indicate the presence of a magnetic field. The first method shown in Figure 19 is a pulse sequence; alternatively, power cycling the sensor will also result in the sensor returning to default operation mode.

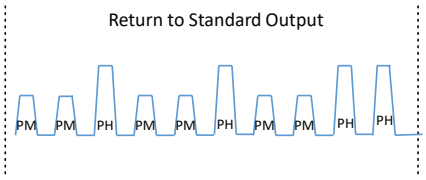

Figure 19: VCC Pulse Sequence to exit EEPROM Readback Mode

Additional Information About Reading EEPROM Registers

"EN/DIS MEMORY READ", "EN/DIS DATA OUT", and "EN/DIS REGISTER" can be thought of as functional toggle switches. When the device is sent each of these pulse sequences, it reacts by toggling its state. After sending these three commands shown in Figure 17, the device is configured in Read mode. The device stays in read mode until toggled OFF. When reading multiple registers sequentially, the pulse sequences shown in Figure 17 should only be sent one time. Figure 18 can be repeated for additional register reads. Read mode can be toggled OFF by resending the "EN/DIS MEMORY READ" sequence or by restarting the part.

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Writing to EEPROM

To write bits into the EEPROM registers, an entire bank of 16 bits must be written at once. To perform the write, a sequence of initialization and addressing pulses must be applied to the VCC pin of the device and then the 16 desired bits must be entered into the device as a series of high-voltage (PH) and medium-voltage (PM) pulses, with PH pulses representing digital 1s and PM pulses representing digital 0s. The programming sequence required to write to EEPROM bank 0x04 after a re-power is shown below in Figure 20. Writing subsequent registers repeats the same pattern without the need to repower or re-enable the register map. Figure 21 shows the sequence to write the EEPROM addresses 0x05 and 0x06 after following the initialization sequence shown in Figure 20. Entering EEPROM write mode without having power-cycled the device, such as after completing a shadow write, is achieved by skipping the initial Re-Power PH pulse. The 16-bit sequence from each bank must be established based on the information in Table 3 and Table 4. Once the lock bit in EEPROM bank 0x04 is set to 1, no further programming can occur. Therefore, EEPROM bank 0x05 and 0x06 must be written before the final write of bank 0x04.

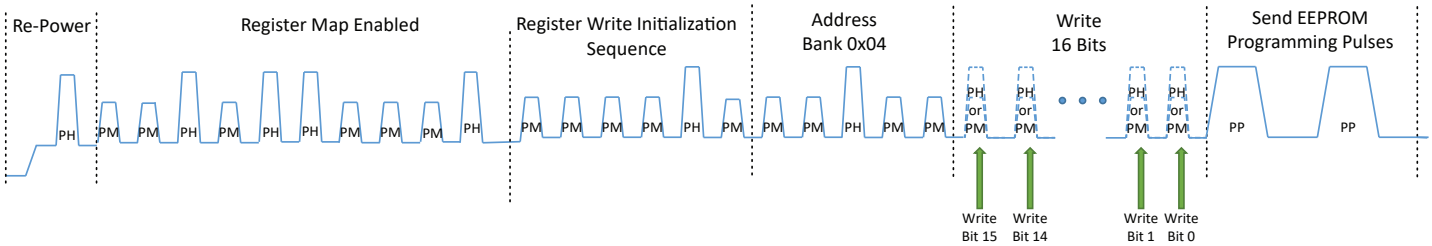

Figure 20: VCC Pulse Sequence to write data to 0x04 EEPROM Register

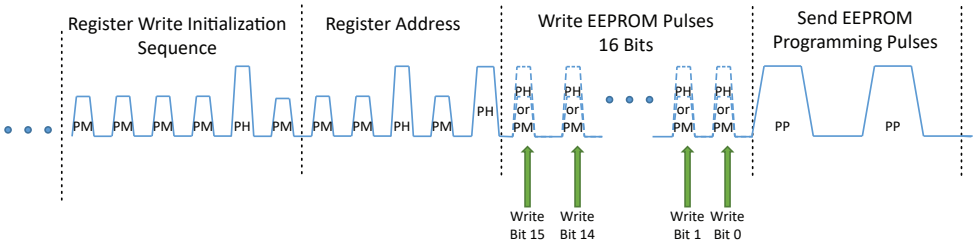

Figure 21: VCC Pulse Sequence to write data to 0x05 and 0x06 EEPROM Registers after Enabling Register Map

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EEPROM Auto-Margining Diagnostic

The APS11900 has a built-in diagnostic tool to validate that the EEPROM programming pulses were adequate to ensure correct operation over all specified operating conditions. After writing the EEPROM and reading the EEPROM back to validate the value is correct, and before setting the “lock” bit, the following procedure (Figure 22 and Figure 23) is used to validate that the internal voltages on the EEPROM cells are correct. It is important to note the following:

1. The MN (EEPROM Margin Pulse) is different from PH pulse; see Table 6.
2. If the APS11900 has been power-cycled since the last Read or Write to EEPROM, then the register map must first be enabled using that portion of the sequence shown in Figure 20.

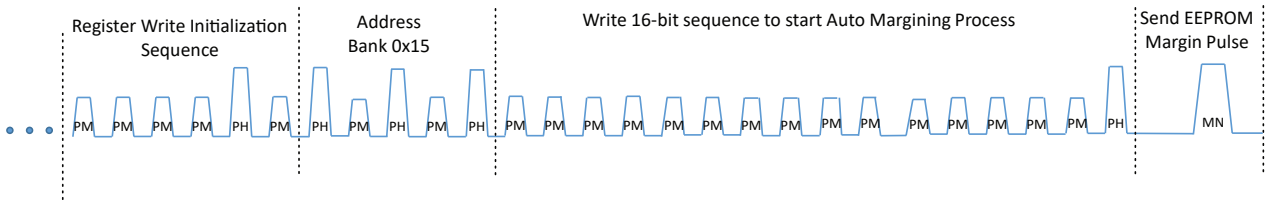

Figure 22: EEPROM Margining Pulse Sequence

After sending the EEPROM Margining sequence (Figure 22), the final step is to read out the results of the diagnostic test. Figure 23 outlines the pulse sequence needed to check the EEPROM margining results. When reading Margining Results, pulse stream bits 3 and 4 are used to determine success or failure of the previous Write to EEPROM sequences.

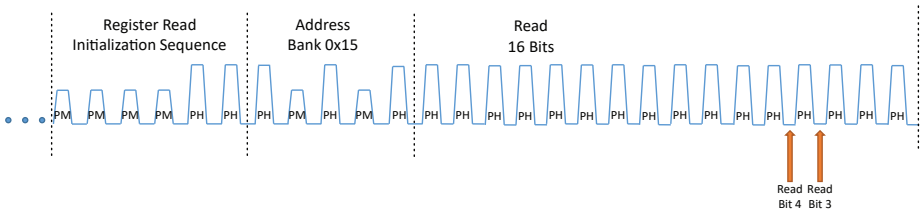

Figure 23: Checking EEPROM Margining Results Pulse Sequence

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Revision History

Number	Date	Description
–	July 16, 2018	Initial release
1	July 30, 2019	Updated Writing Shadow Registers section (page 13), Decrement BOPSEL Tuning Mode section (page 14), Increment BOPSEL Register Tuning Mode section (page 15), Decrement HYS Register Tuning Mode section (page 16), Reading EEPROM section (page 18), Writing to EEPROM section (page 19), and minor editorial updates
2	October 9, 2019	Updated BOPSEL and HYS Tuning Modes and Decrement BOPSEL Tuning Mode section (page 14), Increment BOPSEL Register Tuning Mode section (page 15), Decrement HYS Register Tuning Mode (page 16), and Increment HYS Test Mode (page 17)
3	July 8, 2020	Updated Reading Volatile Shadow Registers section (page 12), BOPSEL and HYS Tuning Modes section (page 14), Increment HYS Tuning section (page 17), and Reading EEPROM section (page 18)

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