CT41X/CT42X DESIGN CONSIDERATIONS

By Allegro MicroSystems

DESCRIPTION

The objective of this document is to help design engineers implement and use the new Allegro MicroSystems XtremeSense™ TMR-technology-based CT41x and CT42x integrated contact current sensors in their designs. The application note provides circuit and printed circuit board (PCB) layout recommendations, as well as other recommendations and tips.

SUMMARY

The following topics are discussed in this document:

- Package and Pinout
- Schematic Recommendations
- Layout Recommendations
- Isolation
- Filtering
- Thermal Considerations
- Stray Magnetic Field Reduction
- Reflow Conditions

INTRODUCTION

The CT41x/CT42x family is a coreless current sensor featuring 1 MHz bandwidth, 3.5 kV isolation, stray field magnetic rejection, and total error of less than 1% full-scale (FS) over the full –40°C to 125°C operational temperature range.

For the full performance details of the CT41x/CT42x refer to refer to the 43x Performance Overview application note (AN131) on the Allegro website. [1]

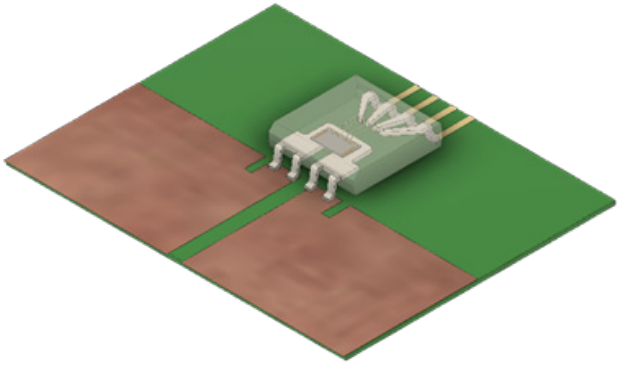


Figure 1: Overview of CT41x/CT42x in SOICW-8 package on a PCB with a current trace.

[1] https://www.allegromicro.com/-/media/files/application-notes/an131-ct43x-performance-overview.pdf?sc_lang=en

NONRATIOMETRIC VOLTAGE OUTPUT

The CT41x/CT42x is designed to produce the same offset and sensitivity as long as the supply voltage is within the operating range.

While ratiometry can mitigate some errors when the supply voltage is variable, it cannot be relied on to provide the high-accuracy figures CT41x/CT42x achieves. This is mainly due to ratiometric scaling mismatch. The CT41x/CT42x with its nonratiometric design, offers high offset/sensitivity precision, supply-voltage noise immunity, and design flexibility.

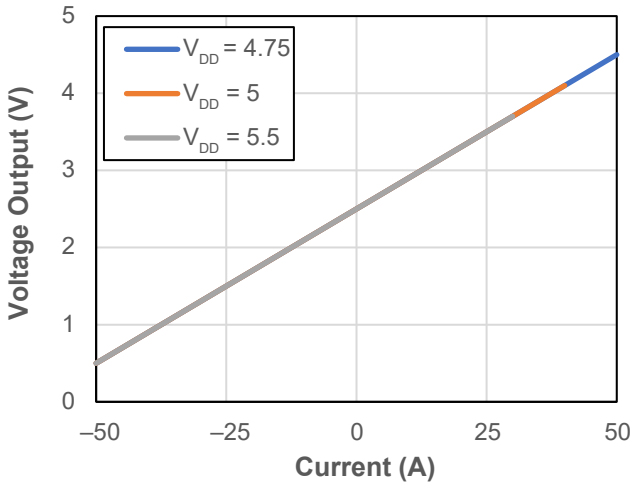
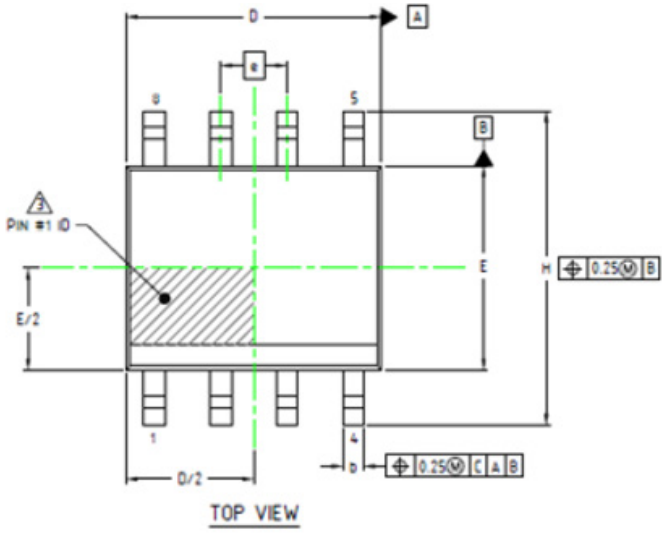
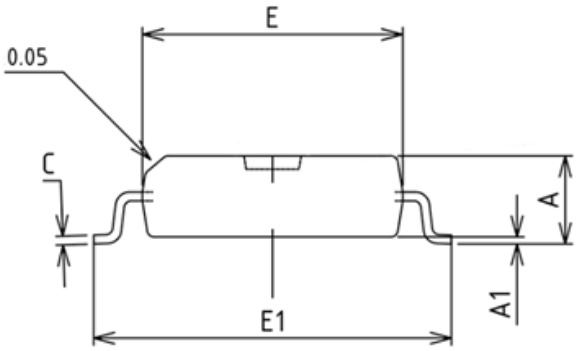


Figure 2: The CT41x/CT42x output voltage gain and offset do not vary with a varying voltage supply on the VCC pin.

SOICW-8 PACKAGE

The CT41x/CT42x is packaged in an industry-standard SOICW-8 with a custom internal lead frame. This package offers 4 mm of creepage and clearance.

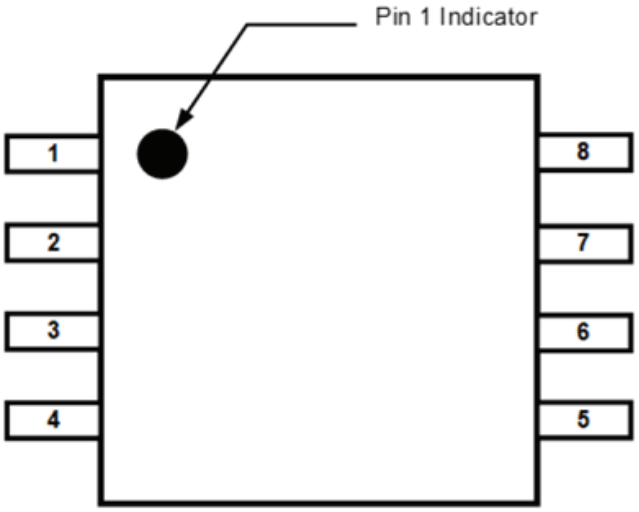




Symbol	Dimension (mm)
A	1.62
A1	0.18
b	0.41
C	0.22
D	4.89
E	3.90
H	6.00
e	1.27

PINOUT

Pin names and functions of the CT41x/CT42x are as follows:



Pin #	Name	Function
1, 2	IP+	Input current
3, 4	IP–	Output current
5	GND	Ground
6	FLT/FILTER	Fault-detection output/filter pin
7	OUT	Voltage output
8	VCC	Supply voltage

SCHEMATIC RECOMMENDATIONS

Decoupling Capacitor

A 1 µF capacitor located as close as practical to the VDD pin is highly recommended. If V_{DD} reduces suddenly, use of decoupling capacitors avoids undervoltage lockout (UVLO) and provides a relatively clean voltage supply that is free of voltage ripple.

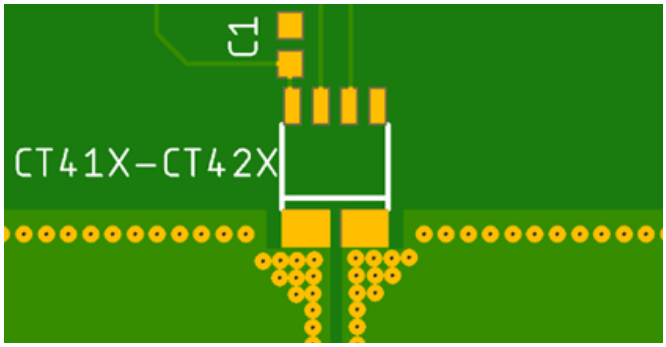


Figure 3: CT41x/CT42x footprint along with a decoupling capacitor, C1.

Single-Ended ADC

The CT41x/CT42x features a nonratiometric voltage output (V_{OUT}). The OUT pin can be connected directly to a single-ended analog-to-digital converter (ADC) input with a precise internal or external reference voltage, which is typically available in MCU-integrated ADCs.

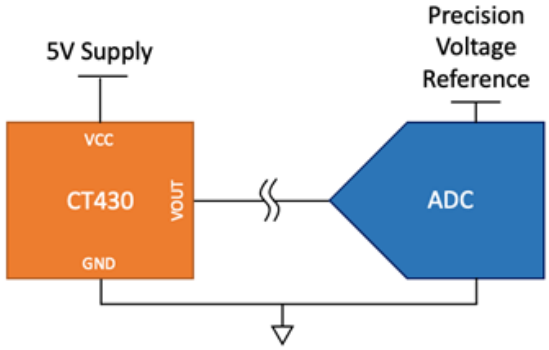


Figure 4: CT41x/CT42x connected to a single-ended ADC.

Fault Pin

The fault (FLT) pin is an open-drain output that can sink up to 20 mA. When active, the FLT pin is pulled low by CT41x/CT42x; otherwise, it assumes a high-impedance (high-Z) value. Depending on the design requirements, a pull-up resistor can be used.

The FLT pin must be grounded if not used.

PCB LAYOUT RECOMMENDATION

Footprint

The recommended footprint for the CT41x/CT42x is detailed in Figure 5.

NOTE: This footprint is able to achieve 4 mm creepage between the pins carrying the primary current (pins 1 to 4) and the signal pins.

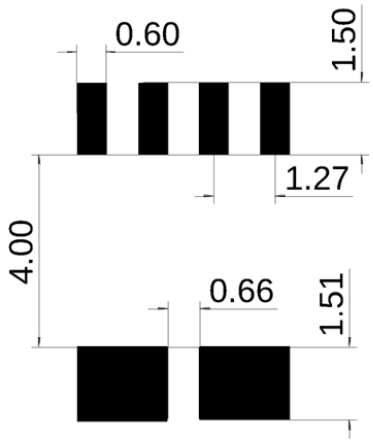


Figure 5: CT41x/CT42x SOICW-8 recommended footprint.

Current-Carrying Trace

The current trace design is very important because it impacts different aspects of the overall performance of the current-sensing system:

- **Heating**

  To minimize heat generation, the following implementations are recommended:

  - Use at least a 70 µm (2 oz) copper thickness
  - Use a board with at least four layers
  - Add thermal vias close to the primary current pins.

- **Magnetic Coupling**

  To reduce any magnetic interference generated by the current trace:

  - The orientation of the current traces is important. Ideally, the current traces should not originate from behind the sensor.
  - The current trace should not be extended below the package.

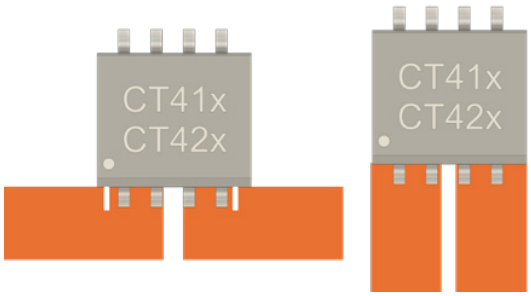


Figure 6: Recommended layouts of the current-carrying trace.

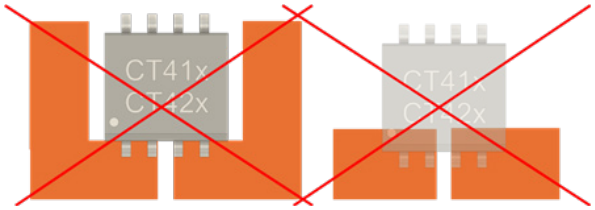
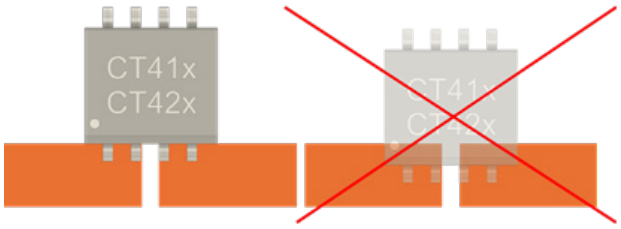


Figure 7: Not recommended.

- **Isolation**

  The distance between the current trace and the signal pins needs to be maximized.

  Hence, extending the current trace below the package or behind the sensor leads to shorter distances between the current trace and signal traces, thereby reducing the isolation specification.



(a) (b)

Figure 8: CT41x/CT42x layouts: recommended (a); and not recommended (b).

Signal Traces

To avoid electrical noise from external capacitive coupling, all signal paths on the PCB should be as wide and short as practical. Signal pins are numbered 5 to 8.

ISOLATION

The package of the CT41x/CT42x is compliant with safety standard UL61800-5-1. The clearance and creepage between the primary conductor and the signal paths is more than 4 mm.

If the creepage is shorter than the design requirement, it is possible to increase it more than 4 mm by adding a slit in the board, as shown in Figure 9.

In terms of safety, the CT41x/CT42x is certified as IEC/UL 62368-1 and UL1577 compliant.

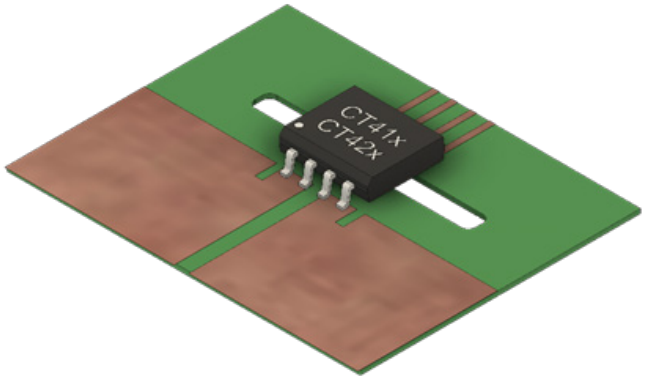


Figure 9: CT41x/CT42x PCB with a slit to increase creepage.

FILTERING

In applications where design constraints do not require the full 1 MHz bandwidth of the CT41x/CT42x, the filter pin allows the user to implement a low-pass filter that reduces bandwidth. This provides benefits in terms of noise and resolution. The filter pin is included in the CT415, CT416, CT425, and CT426 devices.

A single capacitor is used to implement a low-pass filter thanks to the integrated 15 kΩ resistor already in the chip (see Figure 10, top).

The recommended capacitor values are shown in Table 1 along with the obtained bandwidths.

In the CT417, CT418, CT427, and CT428 devices, pin 6 is the fault pin. Because it is an open-drain active-low pin, it requires a pull-up network (see Figure 10, bottom). The FLT pin must be grounded if not used.

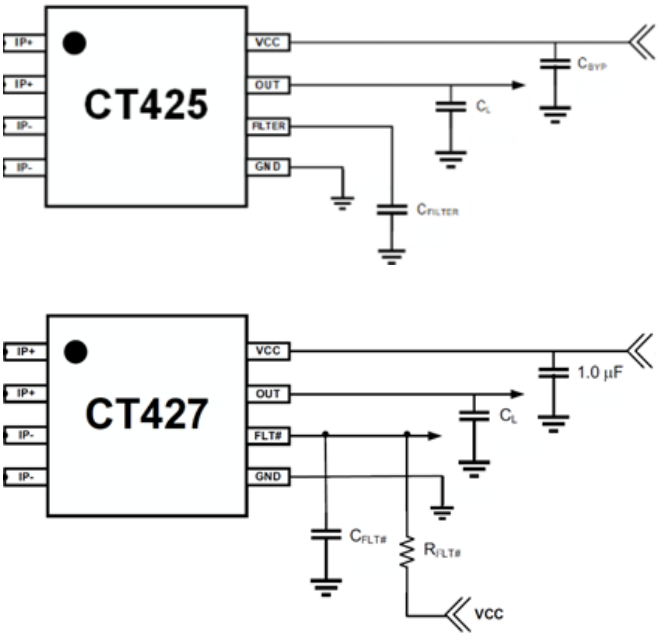


Figure 10: External circuit for the filter pin in CT415/ CT416/ CT425/ CT426 (top) and Fault (FLT) pin in CT417/ CT418/ CT427/ CT428.

Table 1: Recommended Capacitor Values and Obtained Bandwidths

C (pF)	BW (kHz)	Noise (mA rms)
5	1,000	15
10	500	12
20	250	11
47	100	9

THERMAL CONSIDERATIONS

The CT41x/CT42x is capable of supporting up to 50 A rms continuous current at room temperature and even larger current for short bursts.

The limiting factor is the junction temperature, which must remain at less than 130°C. The main parameters that contribute to the junction temperature are:

- Ambient temperature
- PCB layout and characteristics
- Primary current

The junction temperature can be estimated by measuring temperature at the location of the red dot shown in Figure 11.

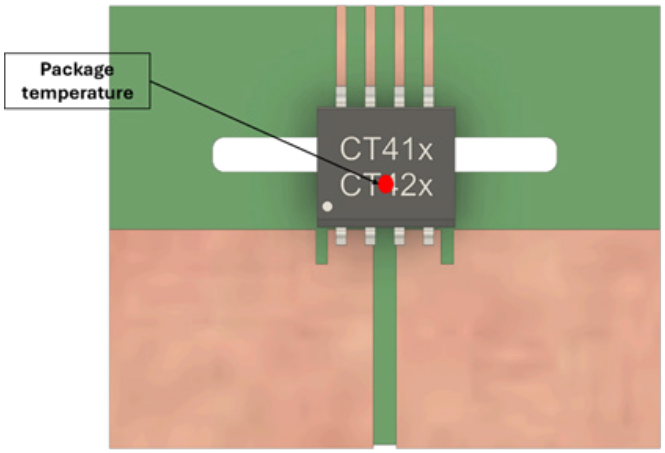


Figure 11: CT41x/CT42x SOICW-8 with a red dot showing the relative hottest point on the package.

STRAY MAGNETIC FIELD REDUCTION

When it comes to common-mode field rejection (CMFR), the CT41x/CT42x benefits from advantages relating to two aspects—axis of sensitivity and differential sensing.

Axis of Sensitivity

XtremeSense TMR has a planar axis of sensitivity as opposed to the perpendicular orientation of sensitivity employed in Hall-effect devices. The CT41x/CT42x is thus better suited to handle the magnetic fields of crosstalk generated by adjacent current-carrying conductors. The magnetic field generated by a nearby conductor is mainly perpendicular, as shown in Figure 12.

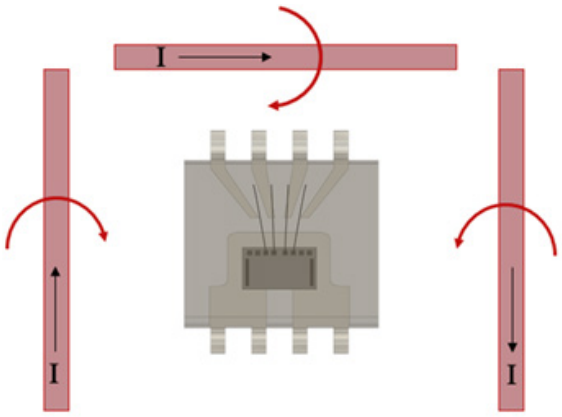


Figure 12: CT41x/CT42x along with three adjacent current-carrying conductors pictured in red.

Differential Sensing

CT41x/CT42x uses two full-bridge XtremeSense TMR sensors to achieve differential sensing capability, which allows CMFR. This is similar to the Allegro CT43x device; a detailed analysis of the CT4xx CMFR is available in the 43x Performance Overview application note (AN131) on the Allegro website. [1] The CT41x/CT42x family is intended for use in magnetically noisy environments and in designs containing multiple current paths.

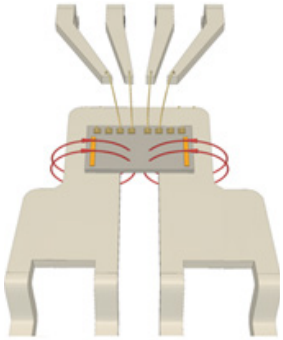


Figure 13: CT41x/CT42x SOICW-8 lead frame approximation showing the internal U-shape that enables the differential sensing capability.

REFLOW CONDITIONS

The recommended reflow temperature profile is outlined in Figure 14 and Table 2. For more details, refer to the Lead-Free Solder Temperature Reflow Profile application note (AN125) on the Allegro website.

OTHER INFORMATION

For additional documentation, visit the Allegro website at allegromicro.com.

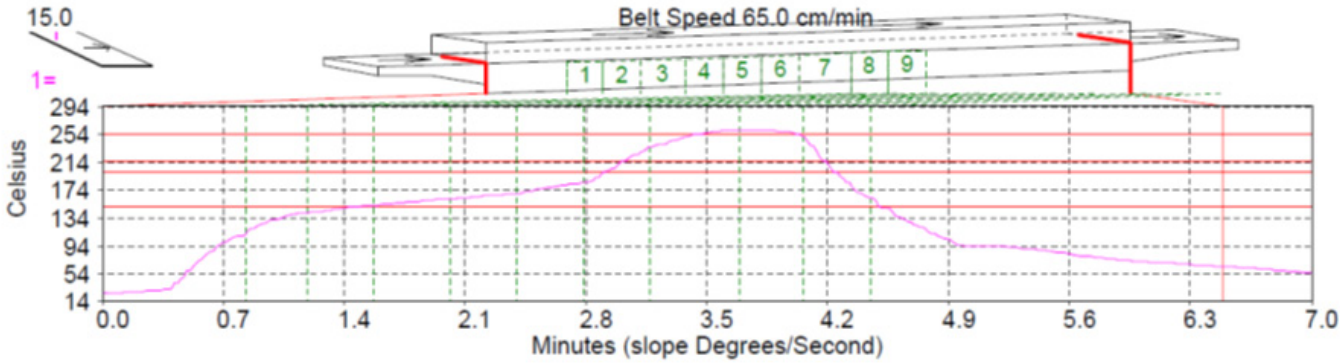


Figure 14: Lead-free solder temperature profile and belt speed for Allegro TMR products.

Table 2: Recommended Reflow Temperature Profile

Parameter	1	TC Mean	TC Range
Peak Temperature	261.4°C	261.4°C	0
Rising Temperature Between 150°C and 200°C	87. 31 s	87. 31 s	0
Total Time at > 217°C	69.88 s	69.88 s	0
Total Time at > 255°C	36.61 s	36.61 s	0

Revision History

Number	Date	Description
–	September 10, 2024	Initial release

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