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MINIMIZING PCB PARASITIC EFFECTS WITH OPTIMUM LAYOUT OF THE GATE DRIVER LOOP APPLICABLE TO AHV85110 AND AHV85111 GATE DRIVERS

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INTRODUCTION

In order to reduce circuit size and increase density, the switching frequency of high-power converters is ever-increasing. It is not uncommon to see switching frequencies above 500 kHz and even beyond 1 MHz in higher power converter applications. This increase is further supported by the introduction of high-power, low $R_{DS(ON)}$ and low gate capacitance MOSFETs and GaNFETs.

To facilitate this high-frequency operation, Allegro has developed a new range of FET drivers to maximize the effectiveness of these FET switches.

Faster switching edges both in the gate drive loop and the commutation loop are a continuous design challenge. The effects of PCB parasitic parameters can play a significant role in circuit operation. This application note focuses on optimization of the gate drive loop for minimum parasitics using the Allegro AHV85110KNHTR isolated gate driver.

PCB tracking and layout are fundamental parts of the operation of an electronic circuit. The PCB tracks themselves introduce inductances and capacitances into the circuit which can often be overlooked. In power switching circuits, these parasitic components can introduce voltage and current ringing on circuit nodes which can greatly inhibit circuit performance and introduce undesired effects such as poor circuit operation and increased EMI.

A solution is often to add, after the fact, components such as snubbers and filters. A better approach is to eliminate or minimize the effects through good PCB layout practices.

This application note discusses some of these effects and shows how to minimize PCB parasitic effects with optimum layout of the gate driver loop.

REVIEW OF FUNDAMENTALS

In order to understand the effects of PCB parasitic inductances and capacitances, it may be useful to review some fundamental concepts.

Inductance

Estimating the inductance of a PCB track is very difficult and made even more so given the high-frequency effects on current flow such as eddy currents and skin effect. However, a review of a fundamental formula for inductance shows how it can be minimized.

$$L = \frac{N^2 \mu A}{le}$$

Where:

N = number of turns

μ = permeability

le = magnetic path length

A = cross-section area

For an electronic circuit, the number of turns, N, is normally equal to one; that is the go and return path of the current in question. The cross-section area, A, is the area encompassed by this current and is one parameter controllable through good PCB layout practices.

Figure 1: Reducing cross-sectional loop area reduces inductance

Capacitance

As with the inductance of PCB tracks, calculating the capacitance between two areas of PCB copper is very difficult. Again, looking at a fundamental formula for the capacitance between two conductors can show what parameters are controllable in PCB design.

$$C = \epsilon \frac{A}{d}$$

Where:

ε = permittivity

A = common area of the pates

d = distance between the plates

Permittivity is a function of the PCB material—normally FR4 with a permittivity of 4.7. 'd' is the distance between the overlapping copper as is defined by the PCB stack up. 'A' is the common area or area of overlap of the conductors.

It is normal practice to use wide and large areas of copper, such as ground planes, to reduce trace impedance. However, it should be remembered that such large areas can add significant capacitance to a sensitive circuit node and the effect of this capacitance must be considered.

Vias

Calculating the inductance of a PCB via is very difficult. A good rule of thumb is 1 nH per via. This rule must be considered when deciding if it is better to use vias to an internal layer or keep the go and return traces on the same layer.

Voltage and current formulae

$$v(t) = L\frac{di}{dt} \qquad i(t) = C\frac{dv}{dt}$$

In the case of an inductor, a rapidly changing current, even if that current is small in amplitude, can result in a large voltage drop across the inductor (or PCB trace). A current of 10 mA switching in 1 ns will result in the same voltage drop as a current of 10 A switching in 1 µs.

In the case of capacitors, a rapidly changing voltage across the capacitor can result in a very large current. This current must always return to its source and, if not managed correctly with good PCB layout, can result in unwanted EMI interference.

With power converter circuits, the trend towards higher powers and higher switching frequencies can mean switching tens or hundreds of volts or amps with rise and fall times of sub 10 ns. With these levels of switching speeds, every nanohenry or picofarad can have a significant effect on circuit performance.

GATE DRIVER CIRCUIT

The AHV85110KNHTR is a driver module for driving GaNFETs. The AHV85111KNHTR driver range is excellent for driving MOSFET switches.

Allegro drivers have the unique advantage in that they require the minimum of external components, particularly on the output side, which is the most critical from a PCB layout point of view. The drivers do not require a separate isolated or bootstrap diode—all of that functionality is included in the drivers using the device's unique Power-thru technology.

The pinout of the device has been carefully designed for ease of PCB layout and optimum performance.

Good quality decoupling capacitors should be used for decoupling the primary, V_{DRV}, and secondary, C_{SEC}, voltages. As stated, the AHV85110KNHTR pinout has been designed for the optimum positioning of these capacitors.

The OUTPU (FET drive on) and OUTPD (FET drive off) can be used directly to the FET gate or with series resistors to control the FET rise and fall times. Having these functions separated but adjacent on the module allows for independent control of the turn on and off times without the need for external parallel diode or transistors circuits while still allowing the driver to be as close as possible to the driven FET.

The gate drive current return to the module is through the OUTSS pins and these have been positioned to allow for the minimum loop area for the gate current.

The example PCB layout in Figure 2 shows the AHV85110KNHTR used with a GaN Systems GS66516T FET and follows the recommended layout for the GS66516T and the principles described above.

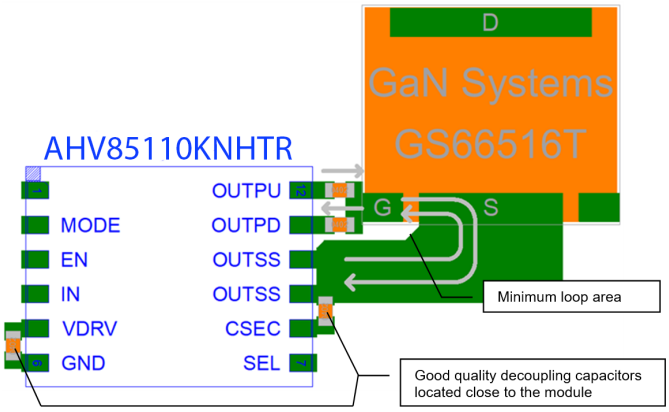

Figure 2: AHV85110KNHTR PCB layout with GaN Systems GS66516T

CONCLUSION

The ever-increasing switching frequencies of power converters results in faster voltage and current transition edges—higher dv/dt and di/dt. This puts more emphasis on the PCB layout. Good PCB layout practices can significantly reduce second order effects such as EMI and can reduce or eliminate the need for circuits such as snubbers or filters required to manage these phenomena. The AHV85110KNHTR and AHV85111KNHTR isolated GaN and MOSFET drivers have been designed to make this process easier, resulting in more effective gate drive applications.

Revision History

Number	Date	Description	Responsibility
–	August 30, 2022	Initial release	Tyler Hendrigan

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