INNOVATION WITH PURPOSE
ALLEGRO microsystems

AHV85111 DESIGN AND APPLICATION GUIDE

By Sonal Singh
Allegro MicroSystems

ABSTRACT

This application note will describe how to choose components and their placement when designing with the AHV85111 isolated gate driver.

INTRODUCTION

The AHV85111 is a self-powered isolated gate driver. Allegro's patented Power-Thru technology allows the transfer of both PWM signal and gate power across a single transformer-based isolation barrier. This eliminates the need to provide an isolated bias supply to power the isolated side of the driver, greatly simplifying the system design. Only an external decoupling capacitor is required on the isolated side.

The AHV85111 driver has been optimized for driving the gate of typical Schottky-gate enhancement-mode (E-mode) GaN FETs, such as those available from GaN Systems, Innoscience, ST, Nexperia, GaN Power International, Taiwan Semiconductor, Rohm, and others. In addition, some Transphorm cascode-GaN devices can also be driven, where low-voltage logic-level MOS devices are used inside the cascode. An online FET selection tool can be downloaded from the Allegro website to assist system designers with checking the compatibility of various FET devices with the driver.

The isolated V_{SECP} positive bias rail is locally regulated using an external resistor divider connect to the FB pin. The balance of the secondary bias voltage becomes the unregulated negative rail V_{SECN}. The V_{SECX} rails regulate quite well versus PWM switching frequency f_{SW} at the IN pin for a given fixed V_{DRV} level and for a fixed load C_{OUT} at the OUTx drive pins. This is because the charge delivered per PWM cycle naturally increases in tandem with the charge consumed by the FET gate, so there is a good charge balance across a wide frequency range.

However, the V_{SEC} rails do vary with effective loading of the gate of the FET being driven; as V_{SEC} levels fall, more charge is available to be delivered to the secondary side, while the charge consumed by the FET gate decreases with falling V_{SEC} levels. Therefore, the V_{SEC} rails will droop as far as needed until the charge delivered matches the charge consumed. For this reason, it is also very important to minimize the amount of charge diverted into any external loads. For example, a very low-bias power external circuit can be powered using V_{SEC}, but the consumption should be minimal in order to minimize the charge diverted away from the gate of the FET. Similarly, if a gate-source pull-down resistor is desired on the load FET (to prevent false turn-on in the case of a manufacturing fault, such as an open-circuit gate turn-on resistor), the resistor value should be as large as possible. The recommended value is 100 kΩ, to minimize DC loading on V_{SEC}. Since DC load current converts to equivalent charge as $\boldsymbol{Q = I \times t}$, DC loading effects will become significantly more pronounced at lower PWM frequency, as the time duration $\boldsymbol{t}$ gets longer. In particular, it should be noted that the driver will attempt to regulate the positive rail V_{SECP} as priority, with the balance of charge diverted to create the negative rail V_{SECN}. In certain situations, such as low V_{DRV}, high-load FET Q_G, excessive external loading of V_{SEC}, high-load FET gate leakage current I_{GSS}, or a combination of these, there may be insufficient charge available to create a sufficient or even any negative V_{SECN}.

Since there is just a single magnetic isolation barrier to transfer both PWM signal and gate power, this also greatly reduces the total parasitic capacitance between the primary-side and isolated-side, to typically < 1 pF total for both signal and power channels. This is much less than the typical total parasitic capacitance value for a solution using a conventional isolated gate driver with a separate isolated DC-DC bias supply, where the capacitance contribution from the DC-DC isolation transformer could be as high as 10 pF or more. This reduction in isolation capacitance greatly reduces the level of noise injected back into the low-voltage control circuit by the high-voltage and high dv/dt switching nodes in the power stage half-bridge legs, reduces system level common-mode (CM) EMI, and saves on power loss that occurs through repetitive charging and discharging of this parasitic capacitance between the high bus voltage level and ground.

PIN-BY-PIN DESCRIPTION

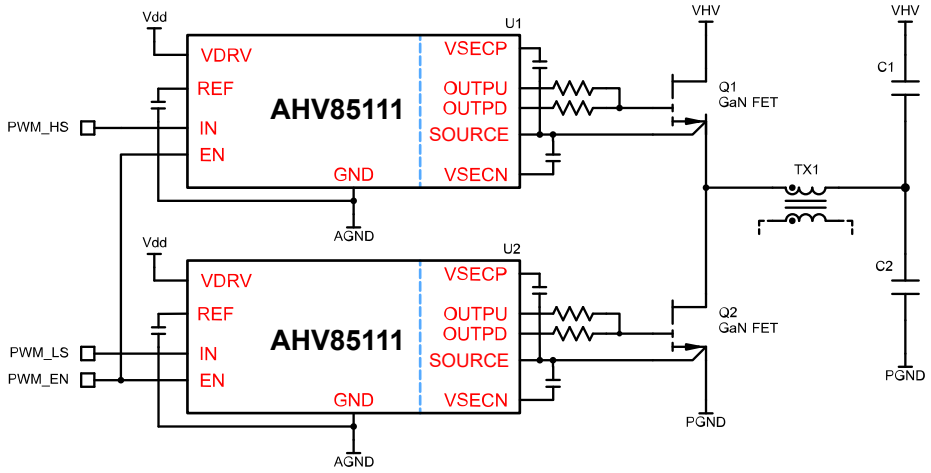


Figure 1: AHV85111 Block Diagram

Pin Table

Number	Name	Function
Input Pins		
1	SEL	Selection pin. Internal use only. This pin MUST be tied to VDRV.
2	EN	Bidirectional enable pin. This pin requires an external resistor pull-up to the VDRV pin. The EN pin should never be left floating. When pulled low through an external open-drain pull-down, the driver is disabled and goes into a low power standby mode.
3	IN	PWM Input referenced to GND. It is recommended to add a low-pass RC filter with a small time constant to filter out any noise coupled to the input. The IN pin can be driven by standard 5 V or 3.3 V logic levels but is also compatible with higher-voltage logic signals since it is rated up to VDRV voltage levels. This allows the IN pin to be interfaced directly to 12 V PWM signals, such as the outputs of typical analog PWM controllers.
4	VDRV	Primary side 12 V bias supply voltage, referenced to GND. VDRV is rated to operate at a drive voltage within over 10.5 V to 13.2 V range. A good quality ceramic decoupling capacitor is required between VDRV and GND. It is recommended to use a 1 µF capacitor, located as close to the device as possible, and connected directly between pins 5 and 6.
6	GND	Primary side ground reference, internally connected to GND net. Note that PIN 6 is the main GND pin, and must always be connected to the system ground. Thermal performance of the package can be improved by connecting the GND pins to a large ground plane, and by adding thermal vias to inner ground plane layers.
Output Pins		
5	REF	Reference pin. Connect an external decoupling capacitor for internal REF rail. The REF pin should not be left floating. REF pin can be used to power external low current loads up to 2 mA. There should be 3.3 V on pin 5 under steady state.
7	FB	Feedback pin to adjust the regulated VSECP level. Connect PIN 7 to the midpoint of a resistor divider to set output voltage between VSECP and SOURCE pins. Refer to the VSECP Voltage Setpoint section of the datasheet.
8	VSECP	This is the positive regulated isolated gate drive bias rail, which is internally generated. An external decoupling capacitor is required from this pin to SOURCE. It is recommended to place the capacitor directly between VSECP and SOURCE, located as close to the device as possible.
9	VSECN	This is the negative regulated isolated gate drive bias rail, which is internally generated. An external decoupling capacitor is required from this pin to SOURCE. It is recommended to place the capacitor directly between VSECN and SOURCE, located as close to the device as possible.
10	SOURCE	Isolated output return pin. These pins are internally connected to the SOURCE net. Note that pin 10 is the main OUTSS pin and must always be connected to the isolated system ground. Thermal performance of the package can be improved by connecting the SOURCE pins to a large ground plane, and by adding thermal vias to inner ground plane layers.
11	OUTPD	Isolated output drive pull-down pin; place a resistor between the OUTPD and FET gate input to control the turn-off speed of the transistor. Ensure that these resistors are high-power rated and have high power surge withstanding capability. See Component Selection section.
12	OUTPU	Isolated output drive pull-up pin; Place a resistor between the OUTPU and FET gate input to control the turn-on speed of the transistor. Ensure that these resistors are high-power rated and have high power surge withstanding capability. See Component Selection section.

DESIGN EXAMPLE

Figure 2 shows a typical application for driving a GaN transistor APEK85111KNH-02-T-MH with a bipolar drive arrangement.

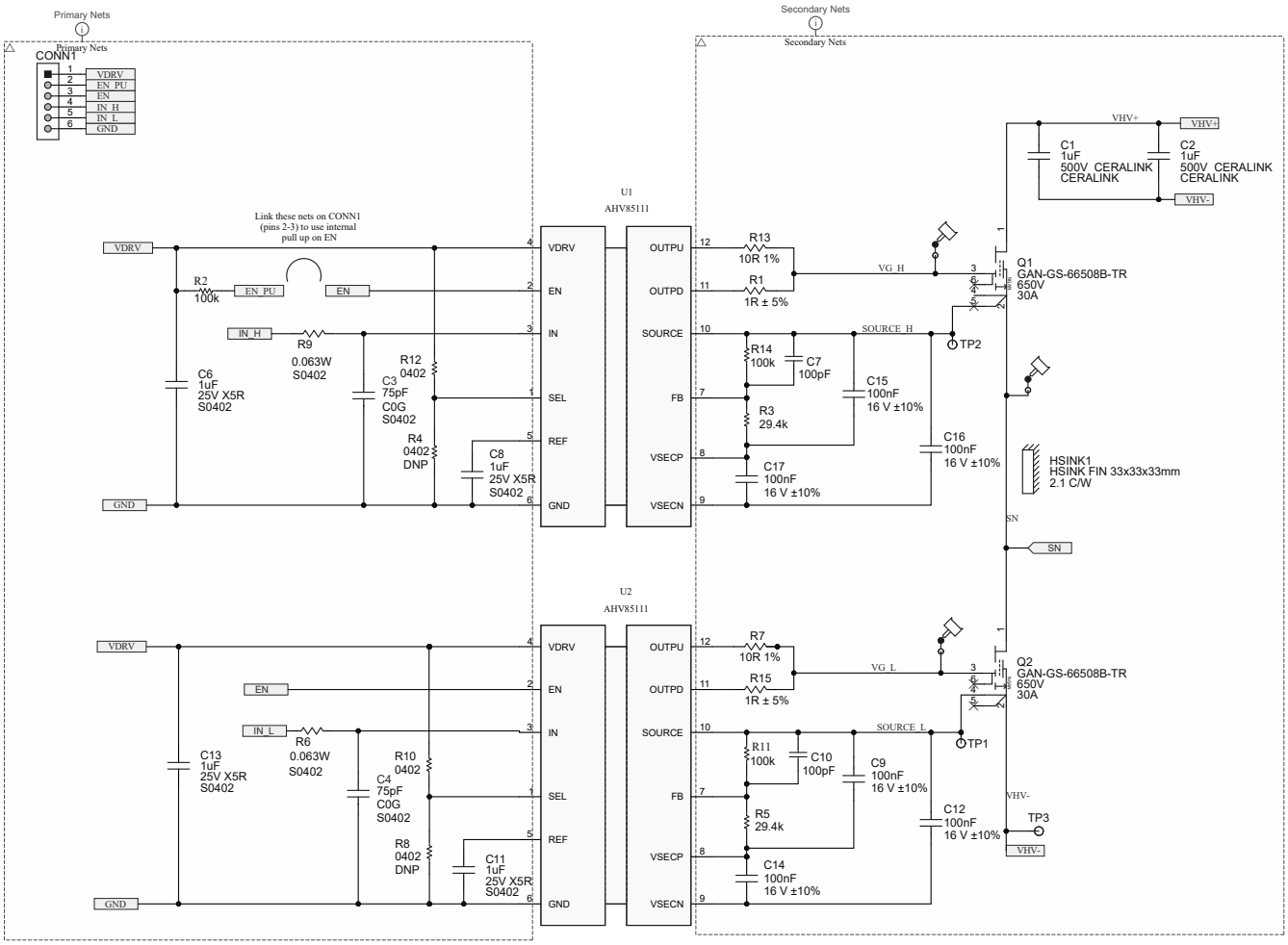


Figure 2: APEK85111KNH-02-T-MH Typical Application

Table 1: Design Parameters

Parameter	Symbol	Value	Unit
Drive Supply Voltage	V_{DRV}	10.8–13.2	V
Maximum Switching Frequency	f_{SW}	1000 [1]	kHz
VSEC Pin Capacitor CSEC	$C_{SEC(NET)}$	50	nF
VSECP Voltage	V_{SECP}	5.4	V
VSEC Pin Voltage Ripple	V_{SEC_RIPPLE}	5–10	%

[1] Frequency depends on factors like heat sinking, temperature, high-voltage decoupling capacitance and IN PWM duty cycle range.

Component Selection

Input Filter for VDRV

In high-voltage switching applications, the dV/dt of the half-bridge switch nodes can be very high. Switching noise can be coupled into other circuit nodes due to the parasitic inductances and coupled capacitances around the driver, and can be made worse as a result of poor PCB layout.

It is important to place decoupling capacitors very close to both VDRV and VSEC pins. They must be connected directly between VDRV/GND and VSEC/OUTSS, respectively, with the shortest possible low-inductance loop.

Input Filter for IN

Some filtering at the IN pin is recommended to filter out high-frequency noise. In the application example, there is a small filter with resistor and capacitor.

EN

Place a 100 kΩ pull-up resistor between the EN pin and VDRV. In the application example, there is a provision to use the EN-PU signal to control the driver enable functionality externally.

REF

REF is an output which supplies a well-regulated reference voltage to circuits within the AHV85111 driver as well as serving as a limited current source for external circuits. This pin must be bypassed to GND with a low-impedance 1 µF capacitor to primary GND placed as close to the REF and GND pins as possible. The current drawn from the REF pin should not exceed 2 mA.

OUTPU and OUTPD resistor

The AHV85111 driver splits the gate outputs OUTPU and OUTPD to allow use of separate pull-up (turn-on) and pull-down (turn-off) resistors. This allows for independent control of the turn-on and turn-off speeds of the transistor. These resistors determine the peak source and sink current by the equations below:

$$I_{source\_pk} = \frac{V_{SEC}}{R_{PU} + R_{PUint}}$$

where $R_{PUint} = 2.8\ \Omega$

$$I_{sink\_pk} = \frac{V_{SEC}}{R_{PD} + R_{PDint}}$$

where $R_{PDint} = 1\ \Omega$

In the application example, $R_{PU} = 10\ \Omega$ and $R_{PD} = 1\ \Omega$, which will give the following calculations:

$$I_{source\_pk} = \frac{V_{SEC}}{R_{PU} + R_{PUint}} = \frac{6.2}{10 + 2.8} = 485\ mA$$

$$I_{sink\_pk} = \frac{V_{SEC}}{R_{PD} + R_{PDint}} = \frac{6.2}{1 + 1} = 3.1\ A$$

Ensure that the resistors can withstand these high peak currents while choosing components.

Note that these resistors are not mandatory; only if the design require control of the switching turn-on and turn-off speed, then it is possible to use these resistors based on the equations above. Ensure that the resistors can withstand these peak currents while choosing components.

Feedback Circuit

As shown in Figure 3, the feedback (FB) pin is used in conjunction with two resistors RFB1 and RFB2 to set the regulated output voltage between VSECP and SOURCE pins.

Decoupling capacitors CSECP and CSECN are connected from VSECP to SOURCE and VSECN to SOURCE respectively, to supply the peak gate charge and discharge currents. In addition, a capacitor CSECPN should be connected directly from VSECP to VSECN to ensure stability of the internal LDO—a value of 100 nF is recommended. A small noise filter capacitor is also recommended to be placed from FB to SOURCE to improve V_{SECP} regulation robustness to noise. Typically, 100 pF is recommended for RFB2 = 100 kΩ.

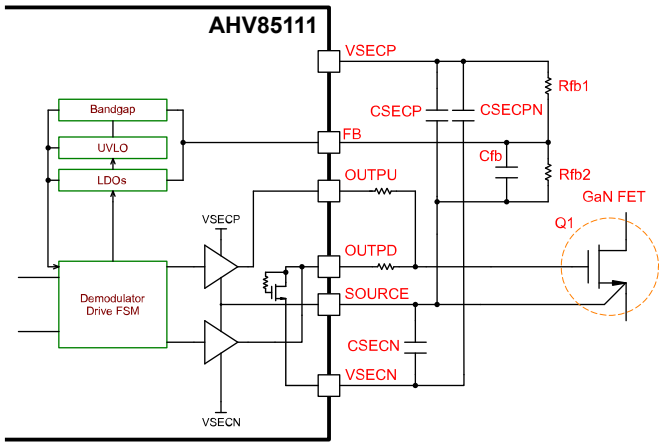


Figure 3: Rfb1 and Rfb2 used to set the desired VSECP-to-SOURCE positive bias rail regulation level

In the APEK85111KNH-02-T-MH, VSECP to SOURCE voltage is set to 5.4 V, with a R_{FB2} = 100 kΩ and V_{FB} = 1.225 V; the RFB1 voltage can be calculated as:

$$R_{FB1} = \frac{R_{FB2}}{\frac{V_{SESCP}}{V_{FB}} - 1} = \frac{100\ k\Omega}{\frac{5.4}{1.225} - 1} = 29.4\ k\Omega$$

The positive output voltage is regulated on-chip with respect to the SOURCE pin, at the level set by choice of RFB2, assuming that the V_{DRV} level is sufficient to allow regulation at the target

V_{SECP} level. The remaining voltage overhead, unregulated, is the negative voltage drive (stored on CSECN).

Figure 4 shows curves of the typical positive output voltage range as a function of the input voltage V_{DRV}. Note that if the V_{DRV} level is too low to allow V_{SECP} to achieve regulation, V_{SECN} will be clamped to zero. Once the V_{DRV} level is sufficient to allow V_{SECP} to regulate, excess secondary bias voltage will then appear on the negative rail VSECN.

PCB layout is critical for the correct performance of power switching circuits. The AHV85111 driver pinout easily facilitates this bipolar drive circuit without compromising on the key PCB layout guidelines.

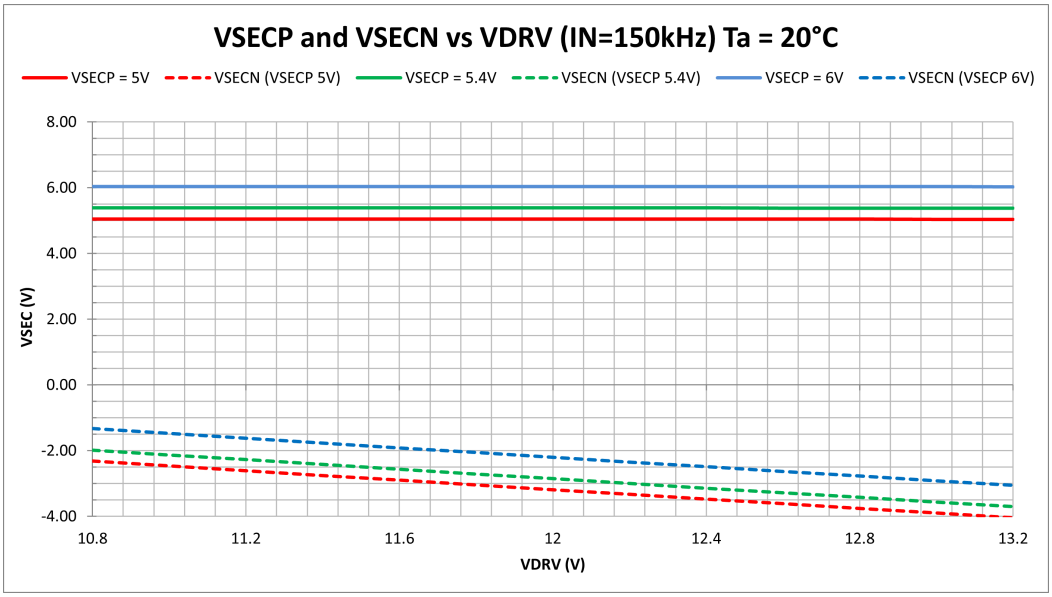
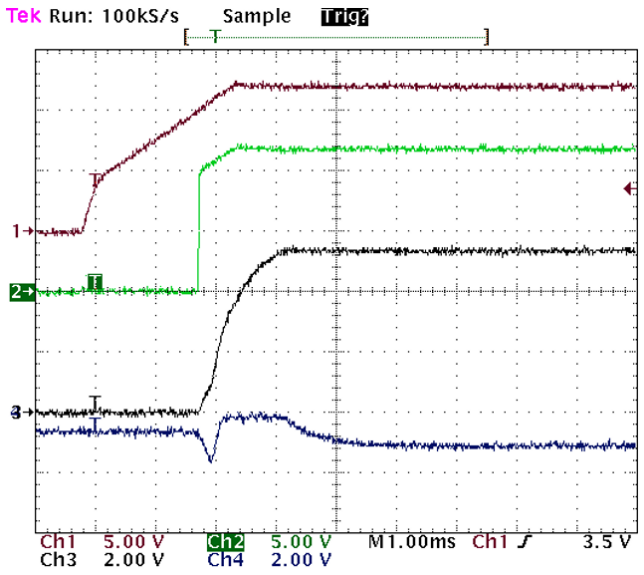


Figure 4: Positive and negative output voltage vs. input V_{DRV} Conditions: f_{IN} = 150 kHz, D = 50%, $C_{SECtotal} = 20 \times C_{OUT}$

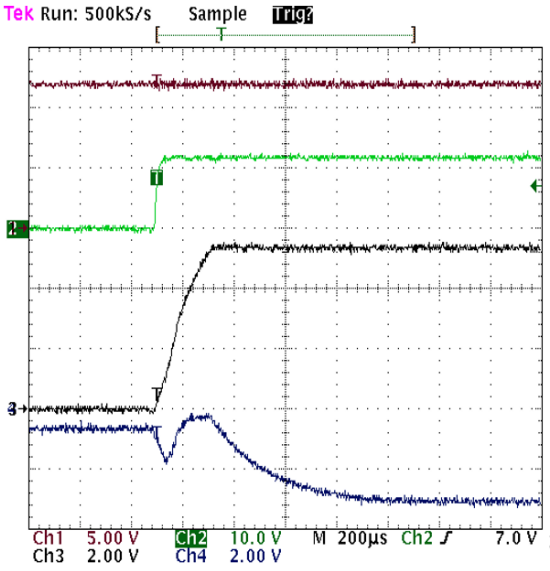
EVALUATION BOARD CHARACTERISTICS

IN = 0, V_{DRV} = 12 V, C_{GATE} = 1 nF, $C_{SEC(NET)}$ = 47 nF
Startup Behavior



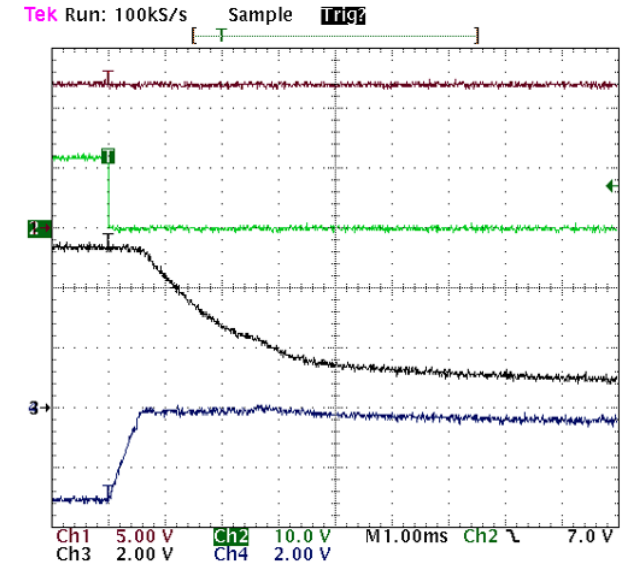
CH1 (Red): VDRV
CH2 (Green): EN
CH3 (Black): VSECP
CH4 (Blue): VSECN

IN = PWM @ 100 kHz, V_{DRV} = 12 V, C_{GATE} = 1 nF, $C_{SEC(NET)}$ = 47 nF
Startup Behavior VSEC



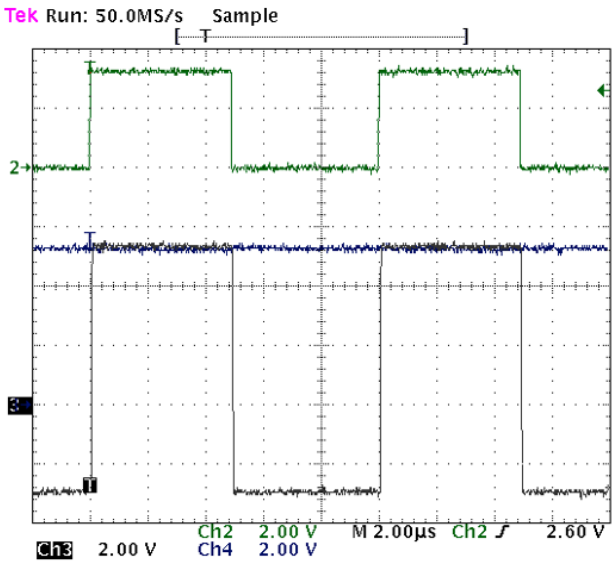
CH1 (Red): VDRV
CH2 (Green): EN
CH3 (Black): VSECP
CH4 (Blue) : VSECN

IN = PWM @ 100 kHz, V_{DRV} = 12 V, C_{GATE} = 1 nF, $C_{SEC(NET)}$ = 47 nF
Shutdown Behavior VSEC



CH1 (Red): VDRV
CH2 (Green): EN
CH3 (Black): VSECP
CH4 (Blue): VSECN

IN = PWM @ 100 kHz, V_{DRV} = 12 V, C_{GATE} = 1 nF, $C_{SEC(NET)}$ = 47 nF
Steady State

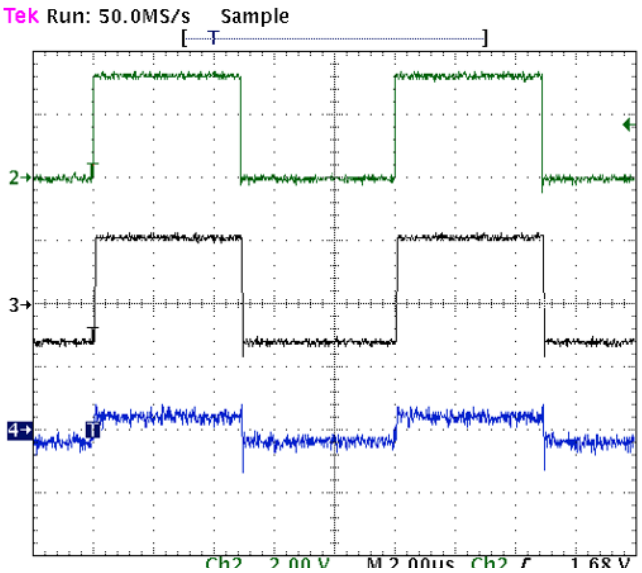


CH2 (Green) : Driver Input
CH3 (Black): Driver Output
CH4 (Blue): VSECP

For further information, reference APEK85111KNH-02-T-MH .

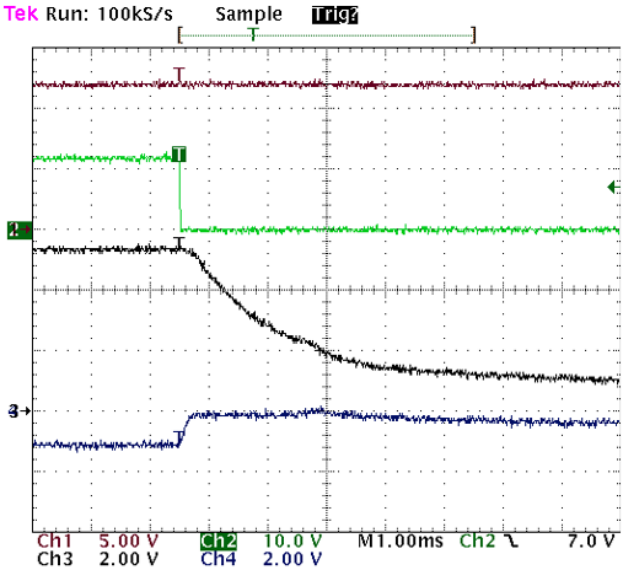
EVALUATION BOARD CHARACTERISTICS (continued)

IN = PWM @ 100 kHz, V_{DRV} = 12 V, C_{GATE} = 1 nF, $C_{SEC(NET)}$ = 47 nF
Steady State Ripple



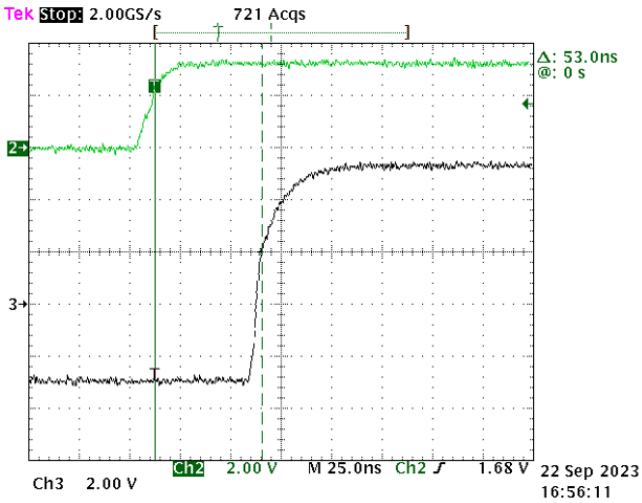
CH2 (Green): Driver Input
CH3 (Black): Driver Output
CH4 (Blue): VSECP ripple (AC Coupled)

IN = PWM @ 0 kHz, V_{DRV} = 12 V, C_{GATE} = 1 nF, $C_{SEC(NET)}$ = 47 nF
EN Toggle 1 to 0



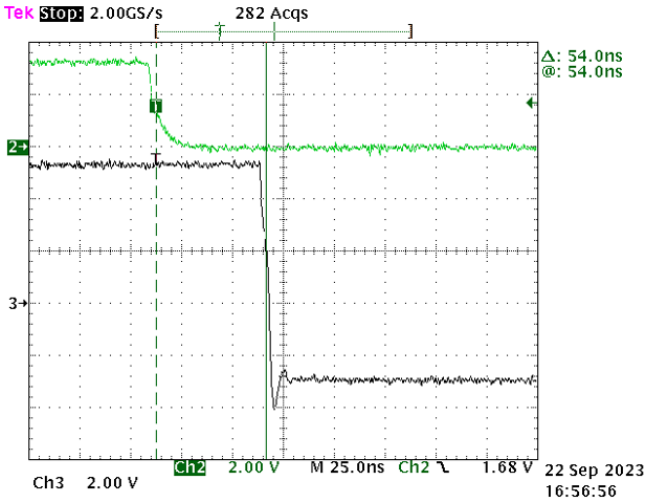
CH1 (Red): VDRV
CH2 (Green): EN
CH3 (Black): VSECP
CH4 (Blue): VSECN

IN = PWM @ 100 kHz, V_{DRV} = 12 V, C_{GATE} = 1 nF, $C_{SEC(NET)}$ = 47 nF
Typical propagation delay



CH2 (Green): Driver Input
CH3 (Black): Driver Output

IN = PWM @ 100 kHz, V_{DRV} = 12 V, C_{GATE} = 1 nF, $C_{SEC(NET)}$ = 47 nF
Typical propagation delay



CH2 (Green): Driver Input
CH3 (Black): Driver Output

For further information, reference APEK85111KNH-02-T-MH .

PCB LAYOUT RECOMMENDATIONS

Since the Power-Thru drivers use an internal miniature transformer to magnetically couple both PWM signal and gate bias power, precautions must be exercised in the system design and PCB layout to minimize unwanted coupling of stray magnetic fields.

These stray fields can be generated by explicit magnetic components in the systems, such as PFC chokes, EMI filter chokes, LLC resonant inductors, and power stage transformers. Since these unwanted stray fields also can cause EMI issues, it makes good design sense to carefully partition these magnetic components from each other, from the EMI filter, etc. These types of magnetic components should also be carefully placed as far as possible with respect to the isolated drivers, to minimize unwanted stray field coupling.

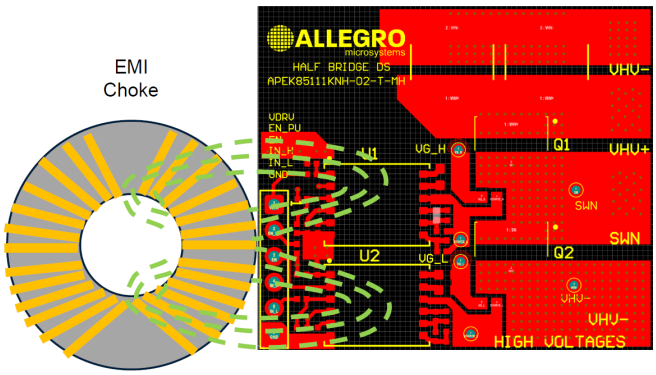


Figure 5: Example of unwanted magnetic coupling due to poor placement of EMI filter choke—too close to the isolated gate drivers

Besides the explicit inductive component sources of stray magnetic fields, there can also be unintended sources. These can arise when high currents flow in large loops in PCB traces, board-to-board interconnect, and system wiring. It is important to minimize the loop area of these high-current loops by routing the out and return traces close together. This ideally occurs on adjacent PCB layer-pairs, right on top of each other.

In particular, avoid routing high-current PCB traces adjacent to or around the isolated gate drivers, to minimize unintended stray magnetic field coupling to the driver. Since the area right under the driver must be kept free of copper traces to meet isolation requirements, it is recommended to keep all other layers under the driver also free of copper traces in order to minimize risk of generating stray fields due to high currents flowing in internal power planes.

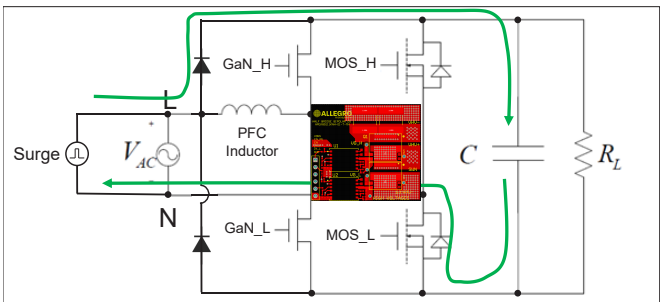


Figure 6: Example of unwanted magnetic coupling due to poor routing of high-current loop under the isolated gate drivers

SYSTEM SURGE MANAGEMENT

During various system-level events, large transient currents can flow for short periods. Examples of this include lightning surge testing to IEC61000-4-5, and system-level ESD testing to IEC61000-4-2. During these events, the large transient currents that flow can also create large stray magnetic fields, and these can also couple unintentionally to the isolated gate driver.

Careful system-level design and PCB layout are of course always important to make sure that the system can pass these required tests. In all cases, defined low-impedance paths must be provided in the PCB design and system wiring to ensure that the surge currents follow defined conduction paths, and are kept away from any sensitive or low-voltage circuits, to prevent malfunction or damage.

For similar reasons, careful system design should be deployed to also steer these large transient surge currents away from the isolated gate driver, to minimize coupling of stray magnetic fields generated by the surge current flow.

For example, in the case of a lightning surge event per IEC61000-4-5, a low-impedance path is often provided via bypass diodes, to conduct the surge current from live/neutral lines directly to the power-factor-correction (PFC) bus capacitor, to avoid having this current flow through the PFC choke and power stage switches. Similarly, inrush current surges at startup would follow the same path directly to the bus capacitor, avoiding potential saturation of the PFC choke and potential damage to the power devices. This is particularly important for GaN power switches, which have a high source-drain voltage-drop when conducting in the third quadrant (compared to MOSFET, assuming the GaN FET is not explicitly turned on during reverse conduction). It is important to carefully place these bypass diodes and route the traces as far away as possible from the isolated gate driver to minimize the risk of coupling the transient magnetic field that will be generated by the flow of high surge current to the bus capacitor.

In many systems designs, circuitry and software to detect and react to surge events may already be implemented and used to activate a system-level protection inhibit signal. For example, such an inhibit signal may be used to temporarily disable the PWM signals to power stages, to temporarily halt the switching activity under high-voltage transient conditions in order to reduce the risk of power switch over-stress.

For increased system robustness, the same surge-detection-inhibit signal should additionally be used to disable the isolated gate driver enable (EN) pins. Since the EN pins are open-drain with an external pull-up resistor, the EN pins of several drivers can be connected to create a shared single-line EN, which can then be pulled low via an open-drain pull-down, driven by the system-level surge-detection-inhibit signal.

An example of the use of this surge-detection-inhibit architecture is shown in Figure 7, for a Totem-Pole PFC power stage. When the surge event is detected, the system controller inhibits the PWM gate drive signal to both GaN and MOS legs and also pulls down the open-drain Enable (EN) lines to all drivers. This ensures a robust response to the surge event.

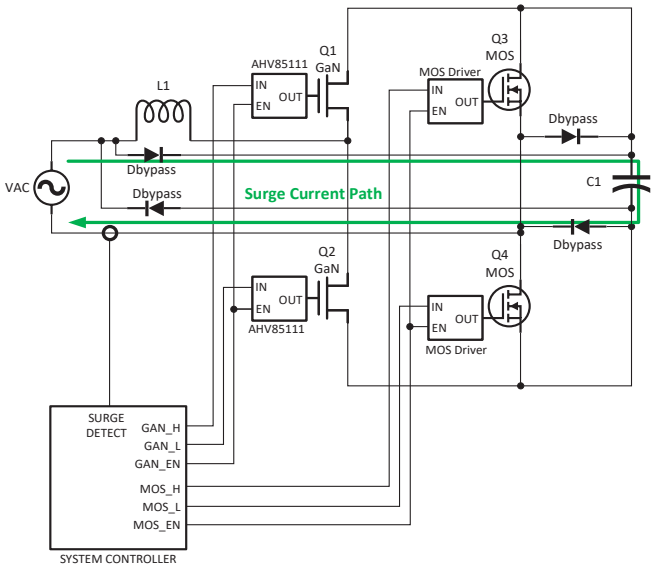


Figure 7: Block diagram of system level surge-detection inhibit signal used to disable isolated gate drivers using the EN pins

The waveforms in Figure 8 show the operation of the inhibit protection, and Figure 9 shows example measurement waveforms taken in the lab.

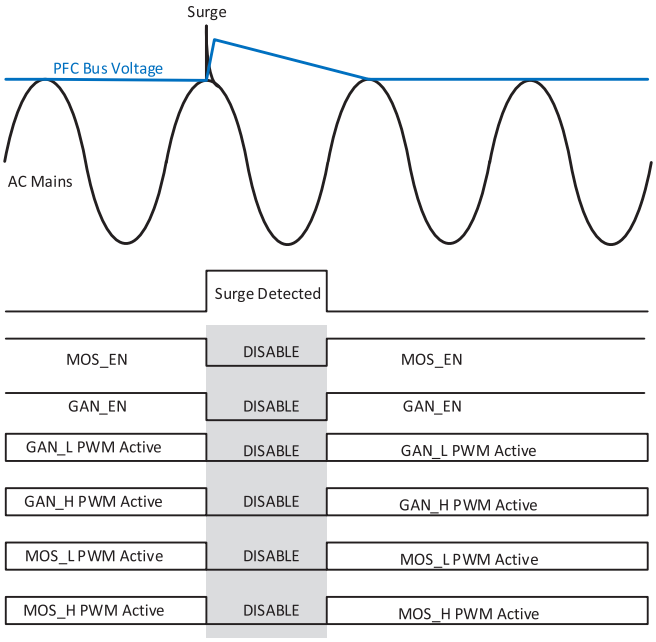


Figure 8: Timing diagram showing use of EN pins to disable isolated gate drivers

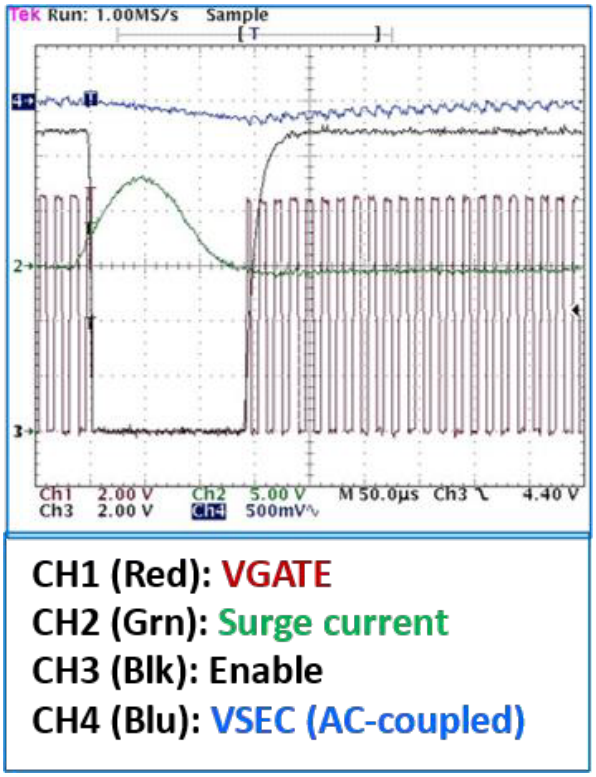


Figure 9: Bench measurement of surge event, showing use of EN pins to disable isolated gate drivers

PCB LAYOUT

Layout Guidelines

The following are some key points to consider while doing the PCB layout for the best performance with AHV85111:

- Place the AHV85111 gate driver as close as possible to the transistor. This is necessary to minimize the path of the high peak currents. This arrangement will also minimize the loop inductance and noise injection on the gate signals.

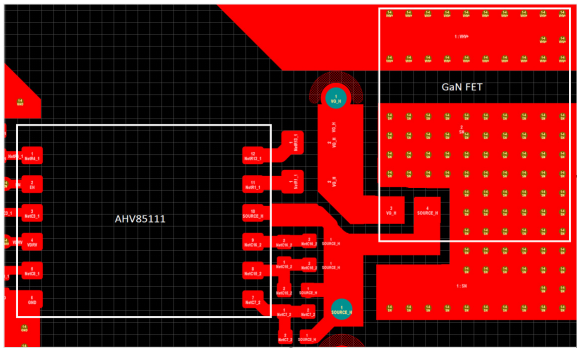


Figure 10: AHV85111 placement

- Ensure that the resistors connected between the isolated output drive pins to the gate of the transistor are high-power rated and have high power surge withstanding capability.
- Decoupling capacitors must be connected close to the VDRV/GND and VSEC/OUTSS pin-pairs.

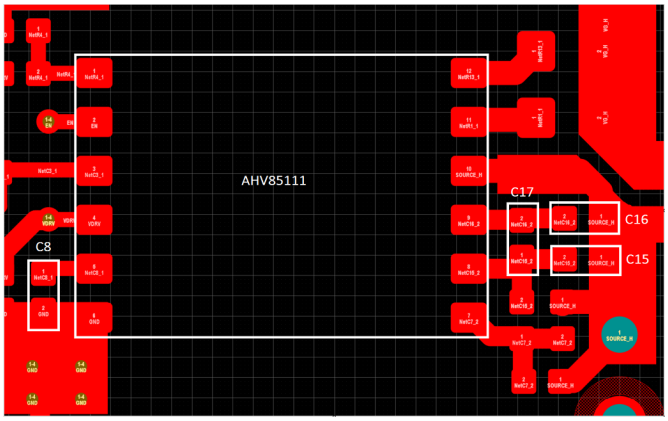


Figure 11: Decoupling capacitor placement

- The path connecting to the source of the transistor should be minimized to avoid large parasitic inductances.

The layout should have good thermal relief to help dissipate heat from the gate driver to the PCB. It is recommended to use vias to maximize thermal conductivity.

LAYOUT EXAMPLE

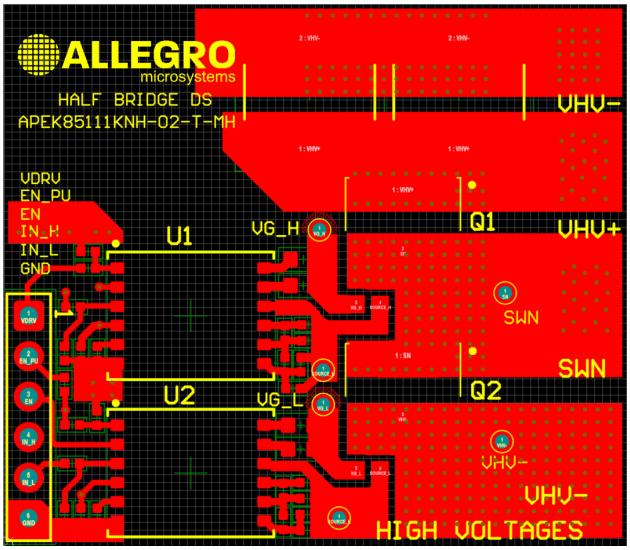


Figure 12 : Layout example

PCB Layers

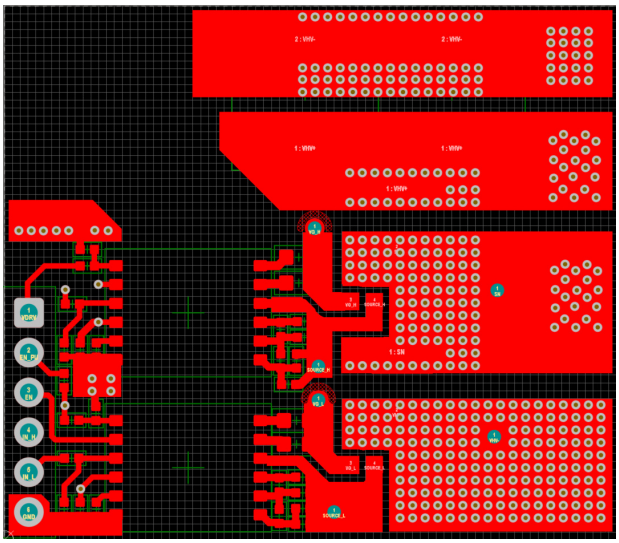


Figure 13: PCB Top Layer

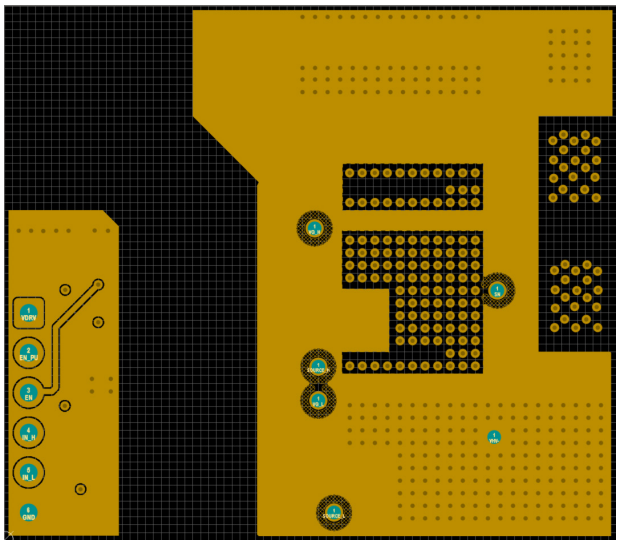


Figure 14: PCB Mid Layer 1

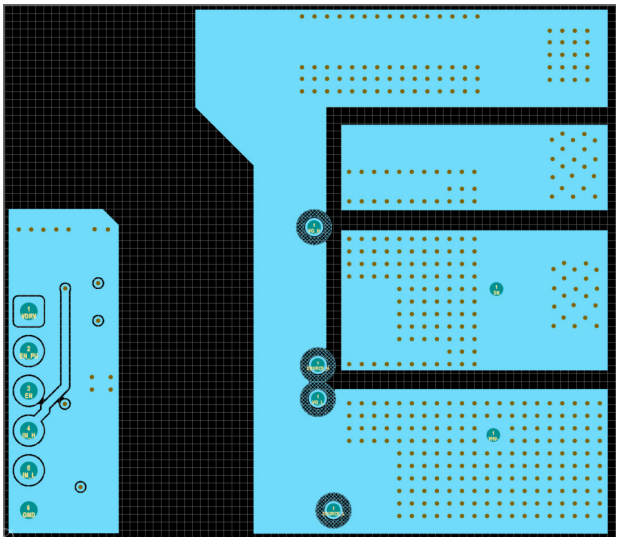


Figure 15: PCB Mid Layer 2

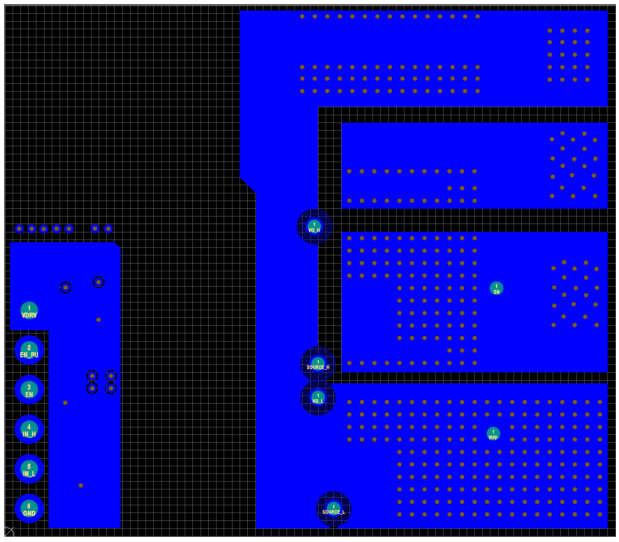


Figure 16: PCB Bottom Layer

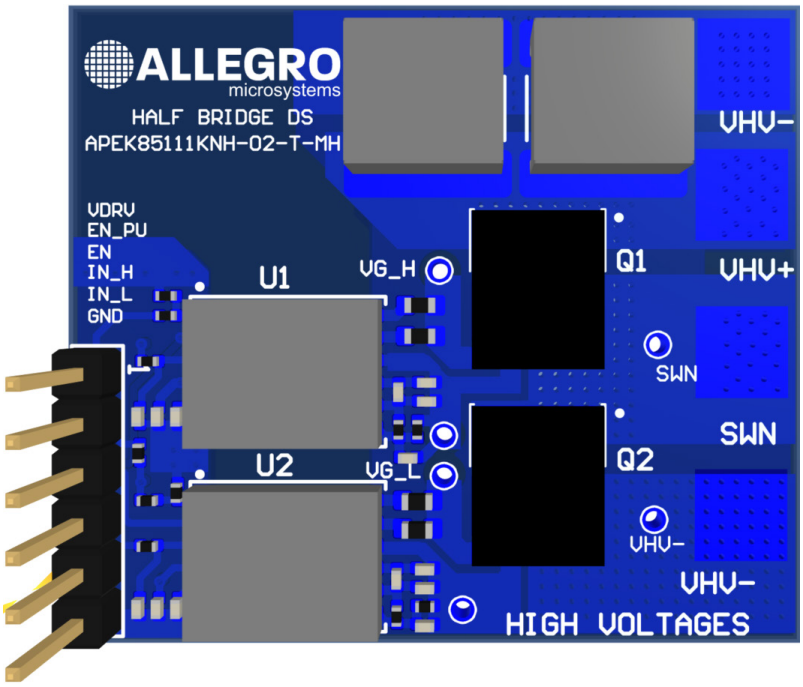


Figure 17: 3D view of PCB layout

Bill of Materials

Table 2: APEK85111KNH-02-T-MH Bill of Materials

Designator	Comment	Description	Quantity	Manufacturer	Manufacturer Part Number
C1, C2	1 uF		2	TDK	B58031U5105M062
C3, C4	75 pF		2	Murata	GCM1555C1H750FA16
C6, C8, C11, C13	1 uF		4	Murata	GRM155R61E105KA12D
C7, C10	100 pF		2	Kyoceraavx	04023A101KAT2A
C9, C12, C14, C15, C16, C17	100 nF	[NoValue], SMD Multilayer Ceramic Capacitor, 0.1 µF, 16 V, 0402 [1005 Metric], ±10%, X7R, CC Series	6	Yageo	CC0402KRX7R7BB104
CONN1	61300611121	THT Vertical Pin Header WR-PHD, Pitch 2.54 mm, Single Row, 6 pins	1	Wurth Elektronik	61300611121
Q1, Q2	GAN-GS-GS66508-B	GaN Systems GS-GS66508 650 V 30 A 50 mΩ	2	Mouser	499-GS66508B-MR
R1, R15	1 Ω ±5%	SMD Chip Resistor, 1 Ω, ± 5%, 250 mW, 0603 [1608 Metric], Thick Film, Anti-Surge	2	Rohm	ESR03EZPJ1R0
R2, R11, R14	100 kΩ	RES 100 kΩ 1% 1/16 W 0402, [NoValue]	3	Yageo	RC0402FR-07100KL
R3, R5	29.4 kΩ		2	Panasonic	ERJ-2RKF2942X
R6, R9	49.9 Ω 1%		2	Vishay	CRCW040249R9FKED
R7, R13	10 Ω 1%		2	Bourns	CMP0603AFX-10R0ELF
R4,R8,R10, R12	0 Ω 1%		2	Multicomp	MCWR04X3601FTL
U1, U2	AHV85111	Single Channel Isolated GaN FET Driver	2		

PCB Material

Use a standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability characteristics.

CONCLUSION

For applications that require high power density or higher switching frequency, the AHV85111 is a perfectly easy-to-use isolated driver solution designed specifically for E-mode GaN FETs. With the advantage of a built-in isolated bias supply for the gate, the AHV85111 eliminates extra circuitry and allows for a compact solution.

Revision History

Number	Date	Description	Responsibility
–	September 25, 2023	Initial release	Sonal Singh
1	July 23, 2024	Updated Introduction (page 1); removed Maximum Gate Charge Capability section (page 3); updated Figure 4 (page 4).	Dermot Dobbyn

955 PERIMETER ROAD • MANCHESTER, NH 03103 • USA
+1-603-626-2300 • FAX: +1-603-641-5336 • ALLEGROMICRO.COM