INNOVATION WITH PURPOSE

SMART RELAY COMMON DRAIN APPLICATION BOARD

By Imhotep Baptiste
Allegro MicroSystems

INTRODUCTION

The A89103 is an N-channel power MOSFET driver capable of both supply and phase isolation. An application board has been developed to replicate the behavior of in-circuit operation.

This board is designed to conduct system-level testing involving isolating a three-phase load from a three-phase inverter.

The AMT49100 is used as the gate driver. Figure 2 depicts the assumed system architecture for the application board.

This application note describes the components of the application board and outlines how it can be configured for normal operation. This document references the application board schematic which can be found in Figure 3.

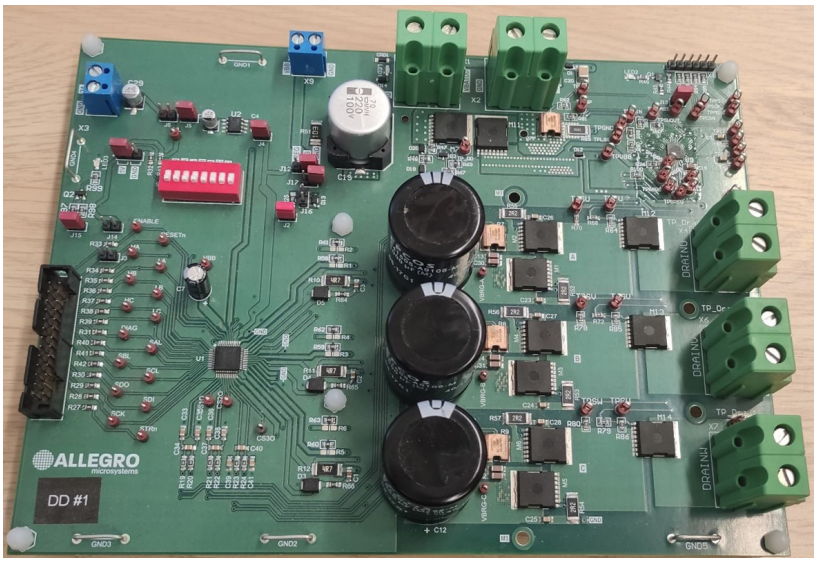

Figure 1: A89103 application board

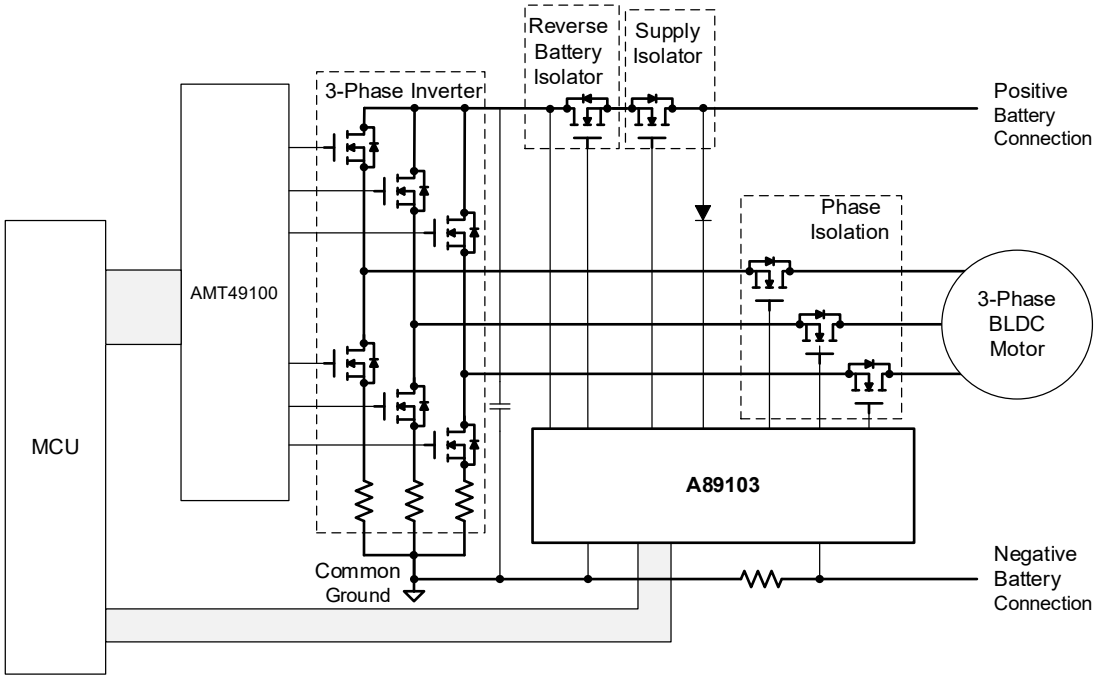

Figure 2: Assumed system architecture

POWER SUPPLIES

This board contains four terminals to allow the connection of power supplies. These are the VBAT supply, the VBB supply, the VL supply, and the VL1 supply. Each supply terminal has an accompanying ground return. The VBAT supply has a separate ground reference to the board, therefore care must be taken when connecting the supplies.

VBAT Supply

The VBAT terminal connects directly to the main battery providing power to the application board. This supply provides the main power to both the A89103 and the AMT49100. The diodes D1 and D13 protect the VBB pins from negative transients by ensuring unidirectional current flow. D13 can be bypassed by connecting jumper J16.

There are three connection options for energizing VBRG of the AMT49100:

1. Common VBB, VBRG: Connect power to X1, remove J17 and fit J12 in position 1, (no external power connection to X9). In this configuration, the AMT49100 is energized from the bridge terminal, and is only energized when both M7 and M11 are turned on as seen in the following figure.

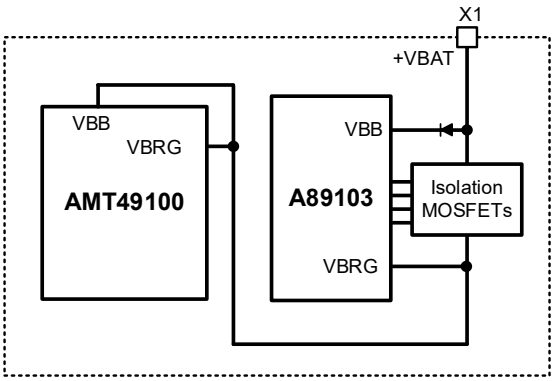

Figure 3: Connection option 1

2. VBB is supplied separately from VBRG. The supply for VBB is sourced from the VBB terminal of the A89103: connect power to X1, remove J12, and fit J17 (no external power connection to X9).

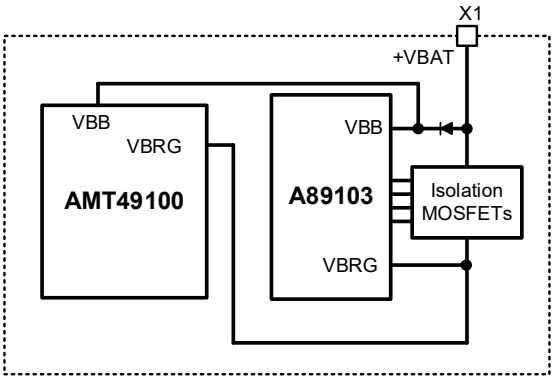

Figure 4: Connection option 2

3. VBB is supplied by a separate supply from the A89103: connect power to X1, remove J12 and J17 (external power connection to X9).

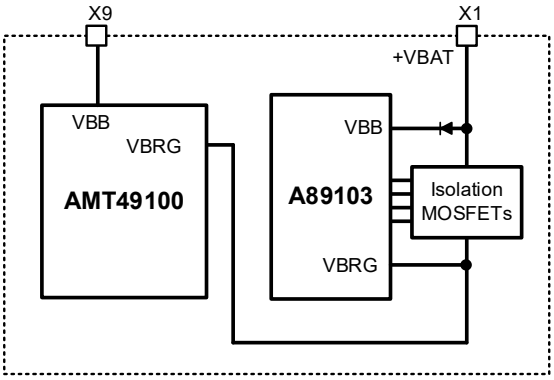

Figure 5: Connection option 3

VBB Supply

Using the VBB supply allows the A89103 and AMT49100 to be energized separately. The bridge supply is still common to both devices. Setting up the VBB supply is described in option 3 above.

VL Supply

This supply provides power to the control logic (HA, HB, HC, LA, LB, LC), the ENABLE pin and the DIAG status LED (LED3). Since this is a logic supply, its maximum voltage is dependent on the product variant (3.3 V or 5 V).

VL may be generated from VREG via linear regulator U2 (J4 and J5 connected), or a suitable external supply may be connected via connector X3 (J6 connected)

The linear regulator U2 is fitted on both the 5 V and 3.3 V boards. Although this is a 5 V regulator, the AMT49100-3 logic inputs are tolerant to this voltage level, operate correctly, and do not suffer any damage. However, care should be taken to ensure that any 3V3 devices connected to ENABLE, Hx, or Lx does not suffer damage; therefore, 1 kΩ buffer resistors are placed in series to provide a level of protection to devices connected to X5.

VL1 Supply

The VL1 supply provides power to the DIAG status LED for the A89103. This 5 V supply can be powered from the FTDI cable.

Communication Ports

The application board contains two communication ports. The IDC 26-way Ribbon Header (X5) is used for communicating with the AMT49100, and the six pin socket header (X8) is used for communicating with the A89103. Both headers are required to communicate with the devices.

The serial interface pins on the X5 header (SDO, SDI, SCK, STRN) are arranged such that they can be driven by an SPI cable.

Switches

The DIL 8-way switch actuator (S1) contains seven active switches. Table 1 describes the operation of these switches.

All the control pins in Table 1 contain an internal pull-down resistor such that when left floating, they are pulled to logic low. If the jumper J1 is moved from its default position (5 V) to GND, the gate drive control pins (HA, LA, HB, LB, HC, LC) is pulled to ground when their respective switches are placed in the on state.

Table 1: A89103 Evaluation Board Switch Operation

Switch	Control State	On State	Off State
S1	ENABLE	ENABLE Connected to VS	ENABLE Floating
S2	HA	HA Connected to VS	HA Floating
S3	LA	LA Connected to VS	LA Floating
S4	HB	HB Connected to VS	HB Floating
S5	LB	LB Connected to VS	LB Floating
S6	HC	HC Connected to VS	HC Floating
S7	LC	LC Connected to VS	LC Floating

OUTPUT TERMINALS

The A89103 contains three output terminals. These are drainU, drainV, and drainW. These terminals are designed to connect to a three-phase load. Each terminal is rated at 60 A; therefore, it is assumed that the RMS phase current of the load is not expected to exceed 60 A for extended periods of time.

JUMPERS

The application board contains twelve jumpers:

- J1 is used to switch between pulling the gate drive control pins to VL or GND. In the default state, J1 is connected to the 5 V supply.
- J2 pulls RESETn of the AMT49100 high when it is connected. If this jumper is removed, RESETn is pulled low due to the internal pulldown resistance. The AMT49100 then goes to sleep.
- J3 connects RESETn to the IDC 26-way Ribbon Header allowing the AMT49100 to be put to sleep digitally.
- J4 connects VREG to the supply of the on-board regulator. This jumper must be engaged if VL is being supplied from the regulator.
- J5 connects the output of the on-board regulator to VL.
- J6 connects the external 5 V supply to VL.
- J12 toggles between shorting VBB, VBRG, and VREG pins of the AMT49100. In the default position, VBB is shorted to VBRG. In the second position, VREG is shorted to VBB, and VBRG is independently energized.
- J13 connects the DIAG pin of the A89103 to the DIAG2 LED.
- J14 connects VL to the IDC 26-way Ribbon Header.
- J15 connects the DIAG pin of the AMT49100 to the DIAG LED circuit.
- J16 is used to bypass the VBB protection diode of the AMT49100.
- J17 shorts both VBB pins together. When this option is selected, ensure that J12 is not in its default position because this results in the VBB and VBRG pins of the A89103 also being shorted.

LEDS

The application board contains three red LEDs. Each LED is used as a different indicator.

- LED1 is connected between VBAT and ground through a current source and is used to indicate when the VBAT terminal is energized when it is illuminated.
- LED2 is connected to DIAG2, and it turns on when the DIAG pin of the A89103 goes low. This LED therefore displays when the A89103 has a fault in the diagnostic register when it is illuminated.
- LED3 is connected to DIAG, and it turns on when the DIAG pin of the AMT49100 goes low. This LED therefore displays when the AMT49100 has a fault in the diagnostic register when it is illuminated.

COMMON DRAIN/COMMON SOURCE CONFIGURATION

There are two configurations of the application board: common drain and common source. These configurations represent the connection of the bridge and reverse MOSFETs to the A89103 as seen in Figure 6. This application note covers the common drain configuration. The full application board schematic can be seen in Figure 7.

The choice of configuration is dependent on the system application.

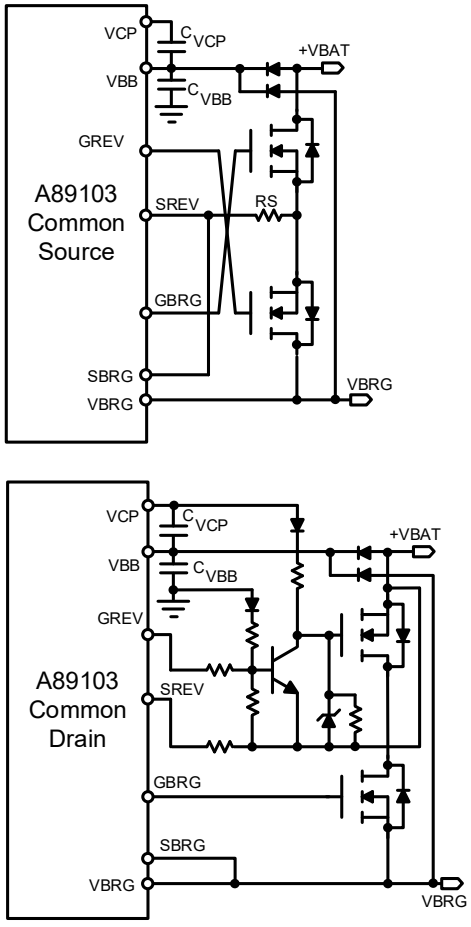

Figure 6: A89103 Common Source and Common Drain Configurations

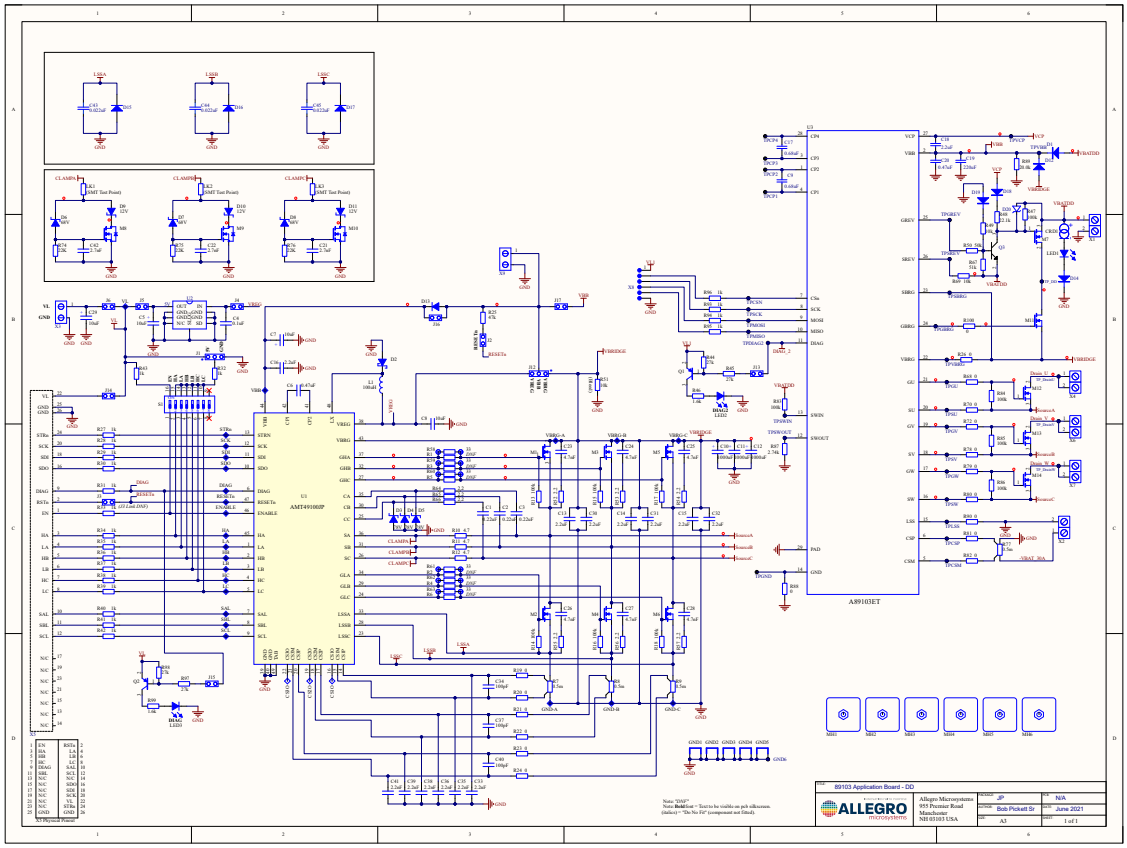

Figure 7: A89103 Application Board Schematic

QUICK STARTUP SEQUENCE

The following procedure describes a startup sequence that can be used to ensure that the board is in an operational mode.

1. Connect the desired three-phase load to the output terminals.
2. Remove jumpers J3, J6, J14, J16, J17. All other jumpers remain in their sockets or in their default positions.
3. Set EN on. All other switches remain off.
4. Connect the FTDI FT232RL to X5 and the FTDI C232HM cable to X8.
5. Connect a 20 V_{DC} supply across +VBAT and -VBAT terminals.
6. Using the A89103 GUI, clear all A89103 startup faults.
7. Configure the A89103 to common drain mode by writing 1 to the SDCFG bit.
8. Turn on all MOSFET drivers by writing 1 to the bits: ENU, ENV, ENW, ENREV, ENBRG and 0 to DISU, DISV, DISW, DISREV, DISBRG bits in the Enable/disable_0 register.
9. Open the AMT49100 GUI and clear all startup faults.

PWM signals can now be connected to the Hx and Lx inputs of the A89103.

CONCLUSION

This application note described the components of the smart relay application board and presented a procedure to safely start up the board.

Revision History

Number	Date	Description
–	January 9, 2024	Initial release
1	November 20, 2024	Updated Quick Startup Sequence and minor editorial updates

955 PERIMETER ROAD • MANCHESTER, NH 03103 • USA
+1-603-626-2300 • FAX: +1-603-641-5336 • ALLEGROMICRO.COM