

## CMTI COMPARISON FOR ALLEGRO INTEGRATED CONDUCTOR CURRENT SENSORS

Integrated Conductor Current Sensor Systems Engineering Allegro MicroSystems

## **CMTI OVERVIEW**

Common-mode transient immunity (CMTI) test injects transient voltages with high slew rates across the isolation barrier of the current sensor. During the transient event, the output stability of the device is observed. The output signal becomes disrupted due to capacitive coupling across the isolation barrier between the leadframe and the signal pins.

This test is important in applications with fast switching with high-frequency transients and demonstrates how well Allegro devices can withstand such events. Allegro integrates an on-chip shield that protects the circuitry by shunting transient disturbances away from the IC circuit, reducing the effects of common-mode transients. See Figure 1.



Figure 1: Diagram of Shielding in Allegro Integrated Current Sensor Packages

## **CMTI TEST METHOD**

For the Allegro integrated current sensors, the transient voltage is applied from the input current pins (IP) to the device GND, and VOUT is monitored. Allegro integrated current sensors under recommended load conditions (depicted in the Typical Application Circuits section) were injected with 1000 V pulses of varying slew rates across the isolation barrier. Slew rate is the 1000 V step divided by the rise time of the transient in V/ns.

The high-performance parallel-interface (HPPI) pulse generator is a charged cable-type pulser. It charges an external length of cable to the desired voltage and, under program control, it dumps the cable charge to the output. The internal power supply determines the pulse voltage, and the length of the cable determines the pulse width. The system has a 50  $\Omega$  output impedance, and the control software is written to reflect the output voltage into a large impedance.

A variety of impedances can be presented at the output, producing different combinations of voltage and current. Discharge into an effective short is useful for surge testing, discharge into a 50  $\Omega$  load is desirable if the signal must be attenuated for read back, and discharge into a high impedance could be used for maximizing the applied voltage. Other combinations can be used and analyzed with simple Ohm's law calculations.

Setting [V]	Impedance [Ω]	Output voltage [V]	Output Current [A]
1000	>1 Meg	1000	~0
1000	50	500	10
1000	<1	~0	20

The connection to the Allegro current sensor and scope is illustrated Figure 2. This allows the scope to be directly connected to the pulse. The primary attenuator is supplied with the scope to allow dissipation of power; the subsequent attenuators and terminator can handle the residual power with standard BNC components. This setup is only usable for high-impedance device-under-test (DUT) connections.



Figure 2: Pulser Connection to Device and Scope

The DUT output is monitored through an optical probe shown in Figure 3. This allows the output to be pseudo differentially monitored. The output monitor can be connected such that it rides along with the high side of the pulser voltage, or the ground side. If the high side of the CMTI pulse is connected to the output side of the DUT board, then the power source must be unreferenced, such as a battery. If the pulse is applied to the current-loop side of a sensor, a bench supply can be used for the DUT power source. When testing nonsensor devices, care must be taken to provide battery power when appropriate.



Figure 3: DUT Output Monitor Connection

## **CMTI RESULTS**

CMTI results in a disturbance at the output. This disturbance can be quantified in two ways: 1) voltage deviation of the output; and 2) output settling time. Refer to Figure 4. Voltage deviation is the maximum voltage overshoot or undershoot of the device output after injection of the defined transient pulse. Settling time is the time it takes for the device output to settle within <100 mV of the initial value.

The images from an oscilloscope, included in this application note, show the voltage disturbances for both positive and negative 1000 V injected pulses. Slew rates used for the positive pulses include [200, 142, 108, 76, 39] ns. Slew rates used for the negative pulses include [-215, -155, -123, -86, -46] ns. The output waveforms during and after the transient disturbances are shown in the following pages of this document.

One way to tabularize the CMTI waveforms is by the minimum slew rate that results in an output with a particular voltage disturbance that settles within a particular time. This method is common in the industry. The typical and minimum slew rate for settling within 100 mV within 0.3  $\mu$ s is shown in Table 1. One way to think about the minimum slew rate is that any transient with a slew rate less than the minimum causes a disturbance of less than 100 mV on the output, with settling time of less than 0.3  $\mu$ s.

Table 2:	Typical	and	Maximum	Slew	Rates
----------	---------	-----	---------	------	-------

Device	Package	Minimum (V/ns)	Typical (V/ns)
ACS733	LA	100	200
	MA	100	150
ACS37002	MA	75	115
	MC	75	115
ACS37010	LZ	100	150
CT432/3	SOICW-16	100	200
CT4327/8	SOICW-8	100	200

Another way to view the CMTI waveforms is by the time it takes to settle to its original value within a particular voltage range. Pulses of 1000 V with slew rates of 140 V/ns were injected into each device to determine the settling time to within 100 mV and within 200 mV, as noted in Table 3.

Device	Package	Time to <100 mV [ns]	Time to <200 mV [ns]
ACS733	LA	150	125
	MA	300	250
ACS37002	MA	50	Never exceeded
	MC	50	Never exceeded
ACS37010	LZ	150	125
CT432/3	SOICW-16	500	400
CT427/8	SOICW-8	30	50



Figure 4: Example Showing Definitions of Voltage Disturbance, Recovery Time, and Slew Rate

## **CMTI PLOTS**

## ACS733KLA

## **Positive Pulse**





## ACS733KMA

#### **Positive Pulse**





## ACS37002LMA

#### **Positive Pulse**





#### ACS37002LMC







## ACS37010LLZ







## CT432/3

#### Positive Pulse





## CT427/8

#### **Positive Pulse**





# TYPICAL APPLICATION CIRCUITS ACS733LA



## ACS733MA



## ACS37002MA



## ACS37002MC



## ACS37010LZ



CT432/3



CT427/8



#### **Revision History**

Number	Date	Description
-	June 14, 2024	Initial release

#### Copyright 2024, Allegro MicroSystems.

The information contained in this document does not constitute any representation, warranty, assurance, guaranty, or inducement by Allegro to the customer with respect to the subject matter of this document. The information being provided does not guarantee that a process based on this information will be reliable, or that Allegro has explored all of the possible failure modes. It is the customer's responsibility to do sufficient qualification testing of the final product to insure that it is reliable and meets all design requirements.

Copies of this document are considered uncontrolled documents.

