INNOVATION WITH PURPOSE

UNDERSTANDING AND MINIMIZING SENSITIVITY SHIFTS DUE TO PCB LAYOUT AND SOLDER VARIABILITY FOR THE ACS37220 IN EZ PACKAGE

Current Sensors System Engineering
Allegro MicroSystems

INTRODUCTION

The ACS37220 is an integrated Hall-effect current sensor capable of measuring high currents of up to 200 A in a small 4 mm × 4 mm footprint. The IC package achieves extremely low electrical resistance and excellent thermal dissipation by using a leadframe with a short current conduction path, large solder pads, and direct soldering to the PCB without standoffs or leads (Figure 1). This construction, however, makes the ACS37220 inherently more susceptible to shifts in sensitivity caused by the PCB layout and PCB soldering, compared to traditional leaded current sensors.

The ACS37220 is factory-calibrated to achieve the specified typical sensitivity (refer to the device datasheet for additional information) when placed on the ACSEVB-EZ7 evaluation board, which is the reference PCB layout (Figure 2). Placing the sensor on a PCB that has a substantially different layout or layer stack-up, compared to ACSEVB-EZ7, can lead to systemic sensitivity shifts of up to ±5% from the typical sensitivity value specified in the datasheet.

CAUSES OF SENSITIVITY SHIFT

There are four important factors causing shifts of the typical sensitivity that must be considered when designing with the ACS37220:

1. The number of PCB layers used for conducting the measured current.
2. The in-plane PCB direction at which the measured current enters and exits the package.
3. The thickness of the solder layer underneath the sensor.
4. Voids in the solder layer at the current input and output pads.

Factors 1 and 2 cause systemic shifts that would be identical for all ACS37220 parts in the specific application PCB. Once the magnitude of these two factors has been characterized during the design phase, the used typical sensitivity value for the application can be corrected. Mitigating factors 3 and 4 might require additional control of the PCB assembly process and might lead to part-to-part variation that contributes to the sensitivity error in the application.

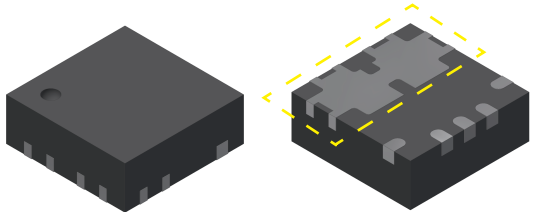

Figure 1: The Allegro EZ integrated current sensor package: a compact 4 mm × 4 mm QFN with 2 pins for the measured current and 5 additional signal pins (not to scale). The leadframe section for the measured current is highlighted by the dashed yellow rectangle.

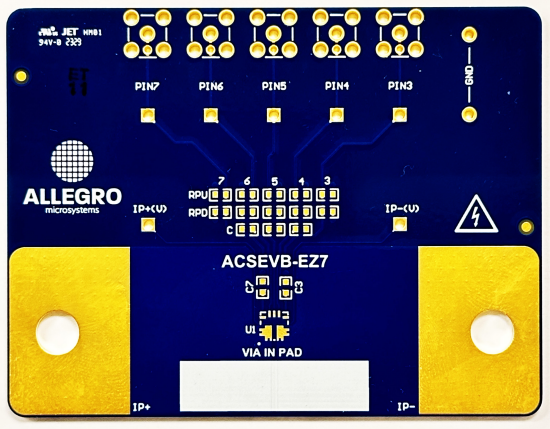

Figure 2: The Allegro ACSEVB-EZ7 bare evaluation board.

Number of PCB Layers

The ACSEVB-EZ7 evaluation PCB uses sixlayers with 2-ounce copper connected by filled in-pad vias for conducting the measured current. This minimizes the PCB trace resistance, maximizes heat dissipation, and also means that the current is effectively distributed along the entire thickness of the PCB before entering the package (Figure 3). If, for example, the same current was to flow only through the top copper layer, the current would be concentrated closer to the sensor's Hall transducers. This leads to a small positive shift in sensitivity when using only the top-most layer, because the Hall transducers inadvertently also couple to magnetic field generated by the current outside the package.

The positive shift in sensitivity versus the number of used layers (counting 1 as the top layer) is plotted in Figure 4. Using only the top-most layer causes a sensitivity shift of around +3.5% from the typical value specified in the datasheet. The shift decreases as the number of copper layers increases. It is therefore recommended to distribute the measured current evenly throughout the entire PCB thickness and to account for systemic shifts when using a PCB stack-up with only one or two copper layers. Heat dissipation from the sensor to the PCB is also strongly dependent on the amount of copper in the PCB near the package, and it therefore recommended to maximize the number of copper layers and connect them with in-pad vias.

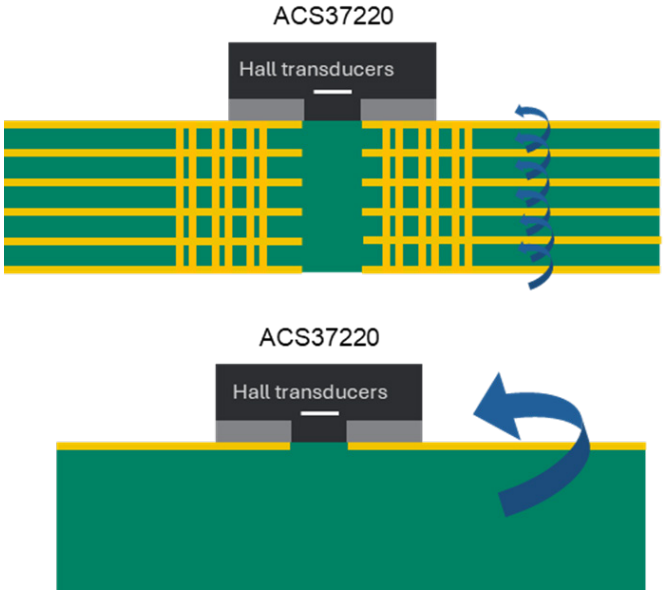

Figure 3: Schematic of the effect of using six versus one copper layer; using only the top layer concentrates the current close to the Hall transducers and causes a positive sensitivity shift.

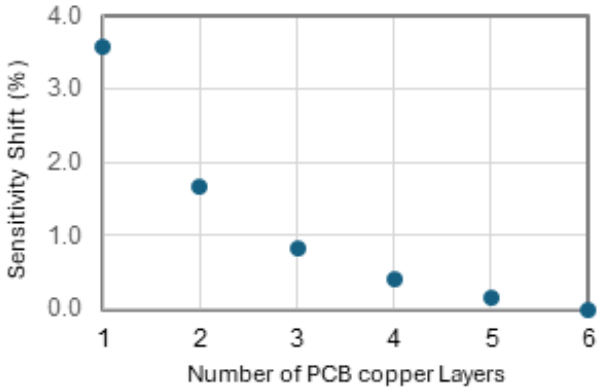

Figure 4: Sensitivity shift of ACS37220 versus the number of copper layers, with 1 being the topmost layer.

Layout and Current In-Plane Direction

The ACS37220 package is susceptible to systemic sensitivity shifts caused by the PCB trace layout geometry. In conventional leaded packages, the protruding leads carry the current away from the PCB traces, concentrate it around the field transducers inside the package, and make the current distribution in the leadframe independent of the PCB traces. In the ACS37220, the PCB traces are within fractions of a millimeter of the Hall transducers. Therefore, the current distribution in the ACS37220 leadframe is affected by the PCB trace layout and by the direction at which current enters and exits the package.

On the ACSEVB-EZ7 evaluation board, the current enters and exits the ACS37220 from the sides of the sensor and flows in a straight line through the package (Figure 5a). If, for example, the layout is such that the current enters the package from the front side and makes a loop (Figure 5b), the typical sensitivity shifts by around +0.4%. And if the layout is designed such that the traces are narrower and force the current through a 180° loop (Figure 5c), the sensitivity can shift by about 1.2%.

To minimize layout-induced shifts, it is recommended to use the general layout of the ACSEVB-EZ7 evaliation board. The measured current is intended to enter the package from the sides and not at an angle, and the ACS37220 should be placed in the middle of traces that extend symmetrically on all sides. When the layout is space-constrained, it is recommended to keep the same general shape and reduce the dimensions proportionally on all sides (Figure 6). Note that reducing the amount of copper around the ACS37220 will also reduce the heat dissipation capability of the PCB and degrade thermal performance.

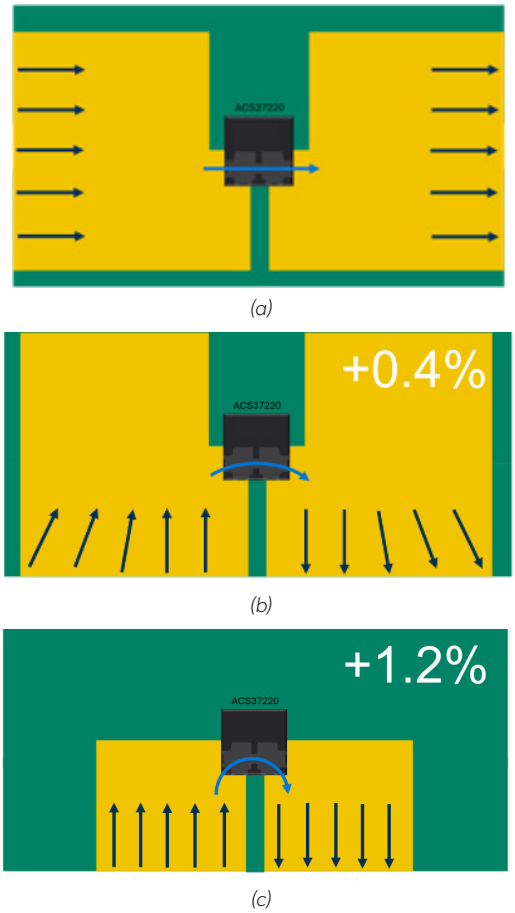

Figure 5: a) The recommended trace layout with current passing in a straight line and the package placed in the middle of the traces. b) A layout with current entering the package at an angle that can result in around +0.4% shift in typical sensitivity. c) A layout with narrow traces and a 180° loop in the current that leads to around +1.2% sensitivity shift.

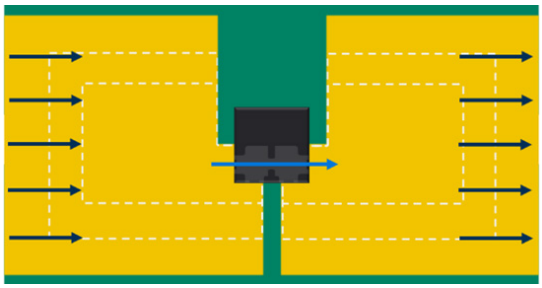

Figure 6: When the trace dimensions must be made smaller in space-constrained layouts, it is recommended to keep the general shape of the ACSEVB-EZ7 and reduce the dimensions on all sides, as indicated by the white dashed lines.

Solder Layer Thickness

In the ACS37220, the leadframe for the measured current is exposed at the bottom side of the package (Figure 1a). This allows the sensor to achieve extremely low electrical resistance and excellent heat dissipation to the underlying PCB. However, when the sensor gets soldered down, molten solder from the current input and output pads generally wicks across the entire exposed leadframe surface. This creates a solder bridge between the current input pad and current output pad, that acts as an additional current path (Figure 7). Thicker solder layers (and accordingly solder bridges) cause more current to pass through the solder bridge instead of through the package. Accordingly, the sensitivity of the ACS37220 decreases with increasing thickness of the solder layer (Figure 8).

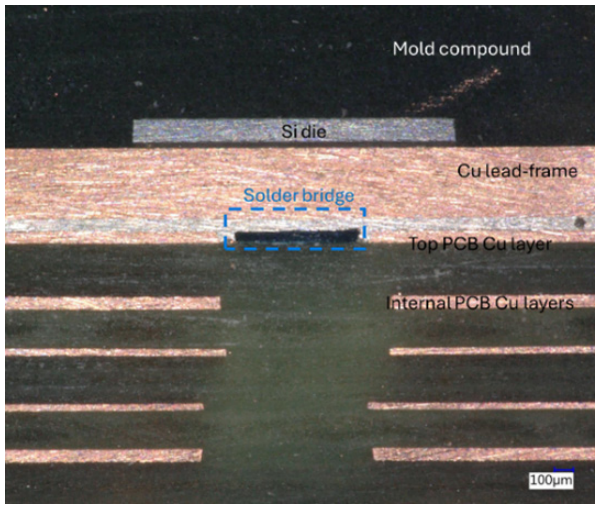

Figure 7: Cross-section photo of a soldered-down ACS37220 along the leadframe path for the measured current showing the formation of a solder bridge between the current input and output pads.

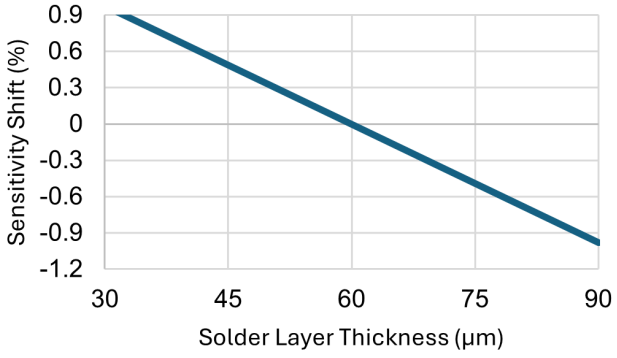

Figure 8: Sensitivity shift of ACS37220 on the ACSEVB-EZ7 evaluation board versus the final thickness of the solder layer after reflow.

The sensitivity of the ACS37220 is factory-calibrated for a 60 µm thick solder layer. The sensitivity decreases by around 0.3% for every 10 µm increase away from 60 µm solder thickness.

The ACS37220 should not be soldered by hand or reworked, as this is likely to leave excessive amounts of solder. Typically, the final solder layer thickness does not vary substantially in well-controlled assembly and reflow processes. To ensure sensitivity accuracy, it is recommended to consult the PCB assembly facility about the expected final solder layer thickness and its expected variation.

Voids in the Solder Layer

Closely related to the shift caused by solder layer thickness described above, the presence of large solder voids also causes a shift in sensitivity. The presence of solder voids causes a negative shift in the typical sensitivity of the ACS37220 because of two factors. First, solder voids tend to increase the solder thickness, because the solder material missing from the void is distributed to the remaining wetted surfaces. Second, the position of the voids also plays a role, because it affects the current distribution in the leadframe close the Hall transducers. For example, solder voids on both the input and output pads, with a radius of 450 µm, cause a decrease in the typical sensitivity by around 0.5% (relative to the case of a continuous solder layer). The exact position of the solder voids along the leadframe can cause an additional decrease of up to 0.4%, with voids located close to the outer edges of the package causing the larger negative shift. Overall, solder voiding can cause a combined sensitivity shift of around –1%. It is recommended to consult the PCB assembly facility about the possible amount of solder voiding and to check for voids in case unexpected negative shifts are observed, for example by X-ray imaging or cross sectioning.

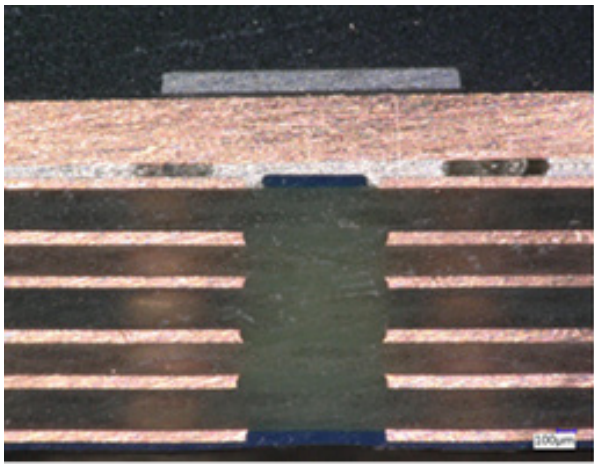

Figure 9: Cross-section photo of a soldered-down ACS37220 along the leadframe path showing large voids at the current input and output pads.

Conclusion

The ACS37220 provides extremely low resistance and high efficiency for the measured current, but achieving high sensitivity accuracy requires consideration of the effects and recommendations described in this document. In cases where these recommendations cannot be followed, it is recommended to check for sensitivity shifts in the designed current measurement system using end-of-line calibration or an electromagnetic simulation. Known systemic sensitivity shifts can be corrected in the subsequent signal stages or in software.

Revision History

Number	Date	Description
–	September 19, 2024	Initial release

955 PERIMETER ROAD • MANCHESTER, NH 03103 • USA
+1-603-626-2300 • FAX: +1-603-641-5336 • ALLEGROMICRO.COM