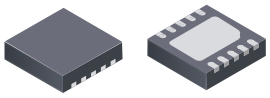
Three Phase Sensorless Sinusoidal Fan Driver

FEATURES AND BENEFITS

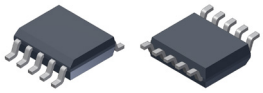
- AEC-Q100 qualified (K version)
- Sinusoidal drive for low audible noise
- Minimum speed function
- Quiet startup adjustment feature
- High efficiency control algorithm
- Sensorless operation
- PWM speed input
- FG speed output
- Lock detection
- Short circuit protection (OCP)
- Overcurrent limit (OCL)

PACKAGES:

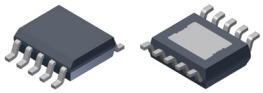
10-contact 3 mm × 3 mm DFN package with exposed thermal pad (suffix EJ)



10-lead SOIC (suffix LN)



10-lead SOIC with exposed thermal pad (suffix LK)



Not to scale

DESCRIPTION

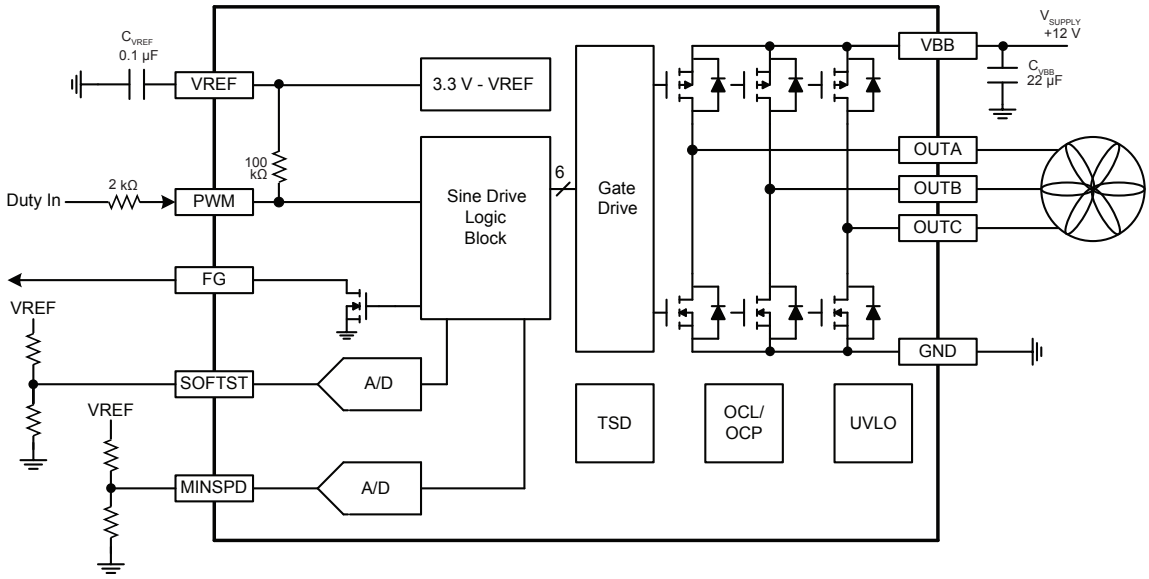
The A5940 three phase motor driver incorporates sinusoidal drive to minimize audible noise and vibration for medium power fans.

A sinusoidal voltage profile is applied to the windings of the motor at startup to quietly startup and gradually ramp up the motor to desired speed. The voltage profile is selectable via SOFTST pin to allow proper operation with a wide range of motor characteristics.

The motor speed is controlled by applying a duty cycle command to the PWM input. The PWM input is allowed to operate over a wide frequency range.

The A5940 is supplied in a 10-contact 3 mm × 3 mm DFN package with exposed thermal pad (suffix EJ), a 10-lead SOIC (suffix LN), and a 10-lead SOIC with exposed thermal pad (suffix LK). The packages are lead (Pb) free, with 100% matte tin leadframe plating.

Typical Application



SELECTION GUIDE

Part Number	Ambient Temperature Range	Packing	Package
A5940GEJTR-T	–40°C to 105°C	1500 pieces per 7-in. reel	10-contact DFN with exposed thermal pad
A5940GLKTR-T	–40°C to 105°C	3000 pieces per 13-in. reel	10-lead SOIC with exposed thermal pad
A5940GLNTR-T	–40°C to 105°C	3000 pieces per 13-in. reel	10-lead SOIC
A5940KLKTR-T [1]	–40°C to 125°C	3000 pieces per 13-in. reel	10-lead SOIC with exposed thermal pad

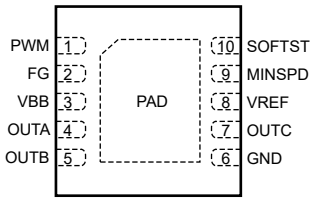
[1] The A5940KLKTR-T variant is in production, however, it has been deemed Pre-End of Life. This variant is approaching end of life. Within a minimum of 6 months, this variant will enter its final, Last Time Buy, order phase. Date of status change: December 5, 2018.

ABSOLUTE MAXIMUM RATINGS

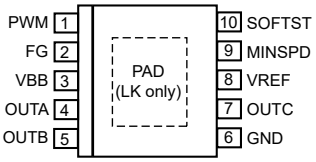
Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		18	V
Logic Input Voltage Range	V_{PWM}	PWM	–0.3 to 6	V
Logic Output (FG)	V_{FG}	FG (I < 5 mA)	18	V
Analog Input	V_{IN}	MINSPD, SOFTST	–0.3 to V_{REF}	V
Output Current	I_{OUT}		I_{OCL}	A
Output Voltage	V_{OUT}	OUTA, OUTB, OUTC	–1.2 to V_{BB}+1	V
Operating Temperature Range	T_A	G temperature range	–40 to 105	°C
		K temperature range	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		150	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Package	Symbol	Test Conditions	Value	Unit
Package Thermal Resistance	EJ	$R_{\theta JA}$	2-sided PCB with 1 in.^{2} copper	60	°C/W
	LN		Single-sided PCB	130	°C/W
	LK		2-sided PCB with 1 in.^{2} copper	40	°C/W



10-contact DFN Pinout (suffix EJ)



10-lead SOIC Pinout (suffix LK/LN)

Terminal List Table

Number	Name	Function
1	PWM	Logic input – speed
2	FG	Speed output signal
3	VBB	Input supply
4	OUTA	Motor terminal A
5	OUTB	Motor terminal B
6	GND	Ground
7	OUTC	Motor terminal C
8	VREF	Analog output
9	MINSPD	Analog input
10	SOFTST	Analog input

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ELECTRICAL CHARACTERISTICS: Unless otherwise specified,
G version valid at T_A = 25°C, V_{BB} = 4 V to 18 V;
K version valid at T_J = –40°C to 125°C; V_{BB} = 4 V to 18 V

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBB Supply Current	I_{BB}	PWM = LOW	–	8	12	mA
Total Driver On-Resistance (Sink + Source)	$R_{DS(on)}$	I = 1 A, T_J = 25°C, V_{BB} = 12 V	–	1.25	1.5	Ω
		Source driver	650	900	1200	mΩ
		Sink driver	250	350	450	mΩ
		I = 1 A, T_J = 25°C, V_{BB} = 4 V	–	1.9	2.2	Ω
VREF Output Voltage	V_{REF}	I_{OUT} = 5 mA	3.2	3.3	3.4	V
Input Pull-Up Resistance (PWM)	R_{PU}	PWM	70	100	130	kΩ
Logic Input Low Level	V_{IL}	PWM	–	–	0.8	V
Logic Input High Level	V_{IH}		2	–	–	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
Output Saturation Voltage	V_{SAT}	I = 5 mA	–	–	0.3	V
FG Output Leakage	I_{FG}	V = 18 V, FG switch OFF	–	–	1	µA
MOTOR FUNCTION						
PWM Duty OF Threshold	DC_{ON}		8.7	9	9.3	%
PWM Duty OFF Threshold	DC_{OFF}		7.3	7.6	7.9	%
PWM Input Frequency Range	f_{PWM}		0.1	–	100	kHz
Motor PWM Freqency	f_{PWM}		21	24.4	28.8	kHz
MIN Speed Selection		Relative to target	0.5	–	0.5	%
Input Current (MINSPD, SOFTST pins)	I_{IN}	V_{IN} = 0 to 5.5 V	–1	0	1	µA
PROTECTION						
VBB Pin Undervoltage Lockout (UVLO)	V_{BBUVLO}	V_{BB} rising	–	3.75	3.95	V
VBB Pin UVLO Hysteresis	$V_{BBUVLOHYS}$		150	300	450	mV
Overcurrent Limit	I_{OCL}	T_J = 25°C	1.7	2.1	2.5	A
Lock Timing	t_{OFF}		4.5	5	5.5	s
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	150	165	180	°C
Thermal Shutdown Hysteresis	T_{JHYS}	Recovery = T_{JTSD} – T_{JHYS}	–	20	–	°C

Note 1: Specified limits are tested at a single temperature and assured across the operating temperature range by design and characterization.

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FUNCTIONAL DESCRIPTION

The A5940 targets fan applications to meet the objectives of low audible noise, minimal vibration, and high efficiency. Allegro's proprietary control algorithm results in a sinusoidal current waveshape that adapts to a variety of motor characteristics to dynamically optimize efficiency across a wide range of speeds.

The speed of the fan is controlled by variable duty cycle PWM input.

The PWM input duty is measured and converted to a 9-bit number. This 9-bit "demand" is applied to a PWM generator block to create the modulation profile. The modulation profile is applied to the three motor outputs, with 120 degree phase relationship, to create the sinusoidal current waveform as shown in Figure 1.

A BEMF detection "window" is opened on phase A modulation profile in order to measure the rotor position so as to define the modulation timing. The control system maintains the window to a small level in order to minimize the disturbance and approximate the ideal sinusoidal current waveform as much as possible.

Protection features include lock detection with restart, motor output short circuit, supply undervoltage monitor, and thermal shutdown.

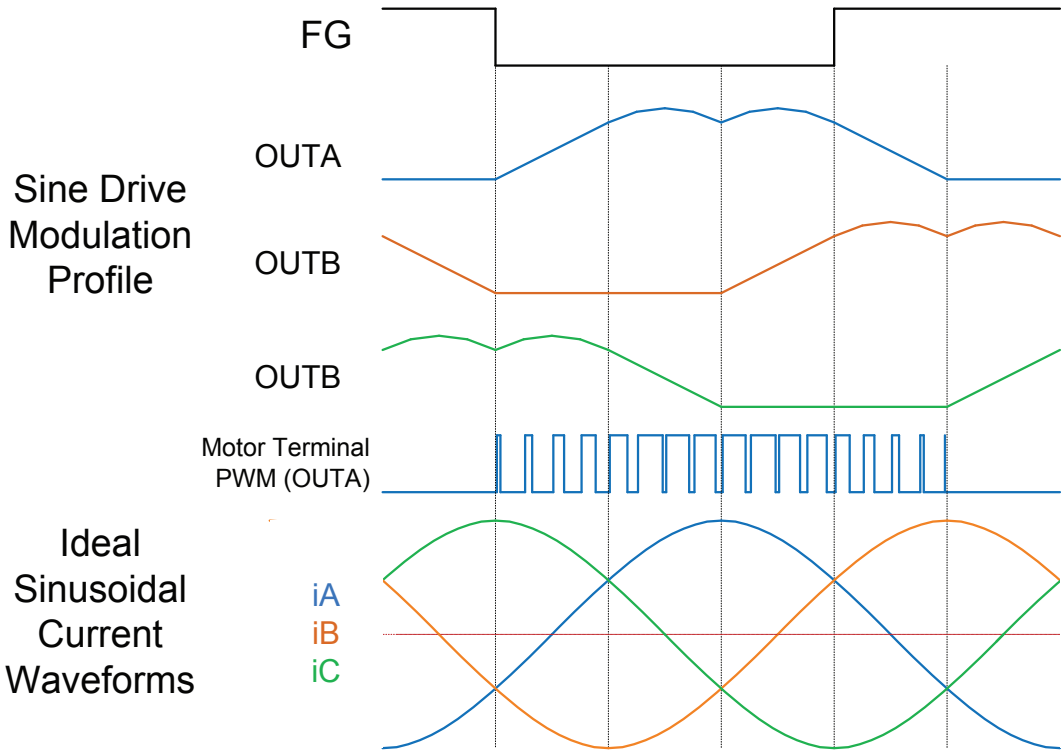

Figure 1. Sinusoidal PWM

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Speed Control

PWM - Duty Cycle Input. A duty cycle measurement circuit converts the applied duty to a demand value (9-bit resolution) to control speed of the fan.

The motor drive will be enabled if duty is larger than DC_ON

The PWM input is filtered to prevent spurious noise from turning on or off unexpectedly.

There is an internal pull-up (100 kΩ) that will turn motor on to maximum speed if input signal is disconnected.

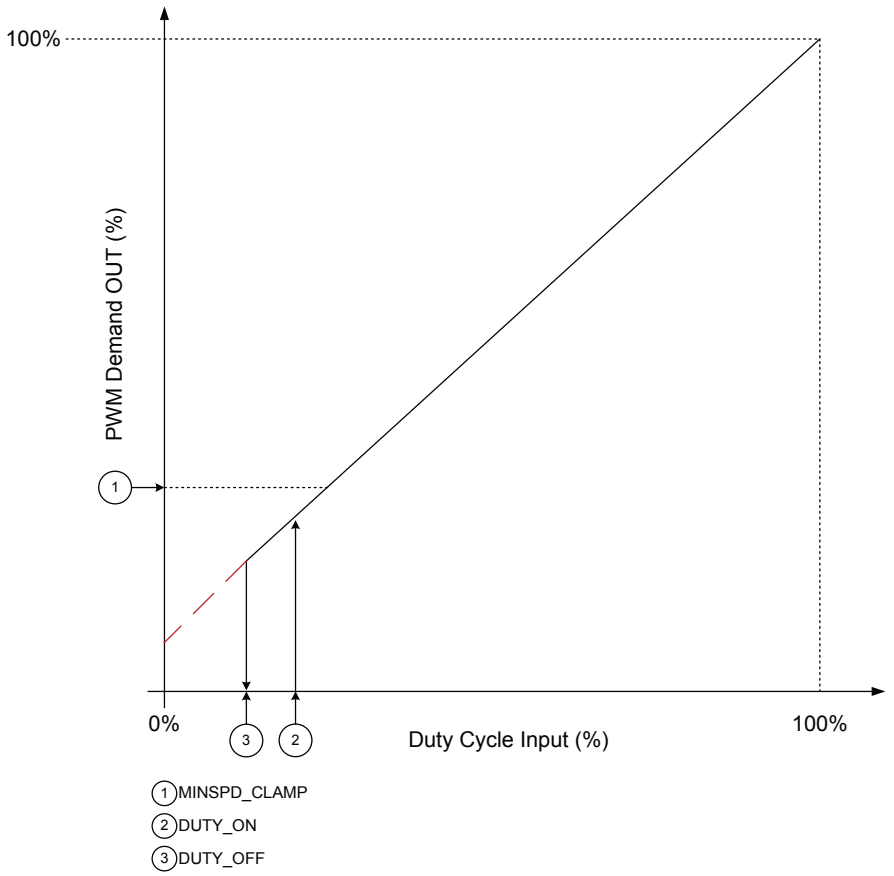

Figure 2. Speed Input Characteristic

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Lock Detect. Speed is monitored to determine if rotor is locked. If a lock condition is detected, the IC will be disabled for t_{OFF} before an auto-restart is attempted.

FG. Open drain output provides speed information to the system. FG changes state one period per electrical revolution of the motor (as shown in Figure 1).

Min Speed Function. Connecting a resistor divider to VREF sets a voltage that is translated to a minimum speed clamp integer by a 4-bit A/D. Connect MINSPD to GND to turn motor off with low (< DC_{OFF}) duty applied. The MINSPD pin should be connected to a voltage between VREF and GND and should not be left an open circuit.

A resistor divider in range 50 to 100 kΩ is recommended.

V_{MINSPD}	Code	Demand %
0	0	0
0.2	51	10.0
0.4	62	12.1
0.6	73	14.3
0.8	82	16.0
1	93	18.2
1.2	104	20.3
1.4	115	22.5
1.6	126	24.7
1.8	137	26.8
2.0	148	29
2.2	159	31.1
2.4	170	33.3
2.6	181	35.4
2.8	192	37.6
VREF	203	39.7

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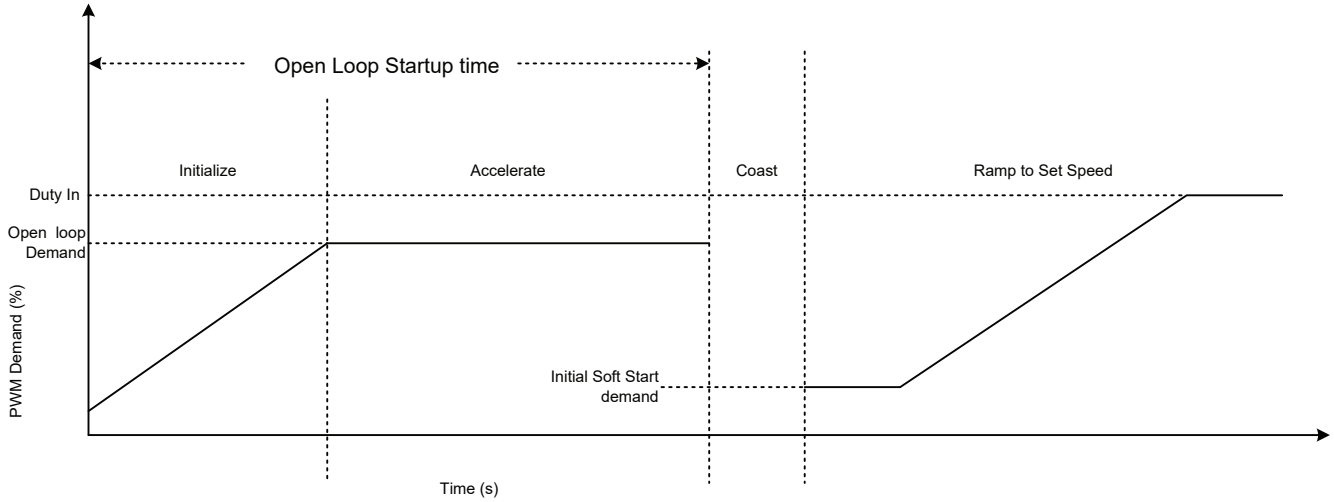
Quiet Startup Operation



A5940 achieves quiet startup with the following sequence:

1. Slowly ramp PWM duty from low value to a chosen Open loop Demand level by stepping motor with a waveshaped sine drive modulation profile.
2. After the fixed open loop Time, the motor position is measured, an initial demand value applied, and slowly the demand is ramped to the final value which is calculated by the duty cycle measurement circuit.
3. The time to ramp to final value depends on Duty IN and Initial Soft Start demand as follows:

   t_{SS} = (target duty % – Initial Demand %) × 8192 ms

   Example target duty = 50%, SOFTST = 15 = VREF (from parameter table Initial SS Demand = 25%)

   t_{SS} = (50-25)% × 8192 ms → 2.048 s

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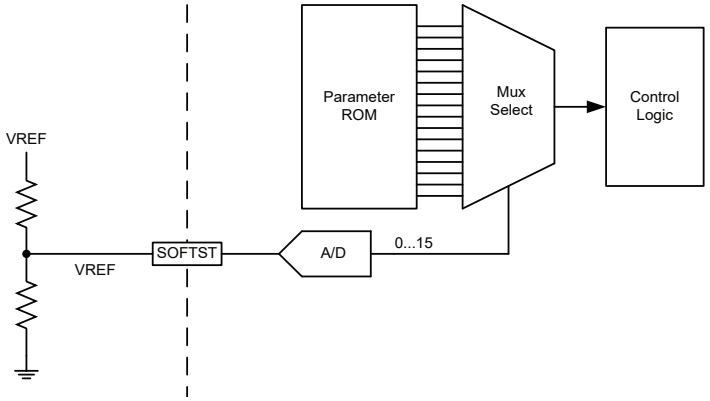
Startup Adjustment

Various permutations of startup parameters are chosen via lookup table with A/D conversion. Sixteen choices of startup parameters are selected by applying voltage at pin SOFTST.

A resistor divider in the range of 50 to 100 kΩ is recommended. The SOFTST pin should be connected to a voltage between VREF and GND and should not be left open circuit.

The various selections have different choices for open loop duration, open loop demand, and initial demand value of soft start after the open loop startup period.



V_{SOFTST}	Selection	Open Loop Time (s)	Open Loop Demand (%)	Initial Soft Start Demand (%)
GND	0	1.1	20.5	11.1
0.2	1	1.1	8.1	6.2
0.4	2	1.1	21.0	11.1
0.6	3	1.1	28.9	23.8
0.8	4	1.1	40.0	14.4
1.0	5	1.1	52.5	11.1
1.2	6	1.1	52.6	23.8
1.4	7	1.1	62.3	23.8
1.6	8	1.1	79.0	11.1
1.8	9	1.1	96.6	11.1
2.0	10	1.9	28.9	14.4
2.2	11	1.9	40.0	23.8
2.4	12	1.9	59.4	37.9
2.6	13	1.9	77	37.9
2.8	14	1.9	98.5	48.8
VREF	15	1.9	63.5	23.8

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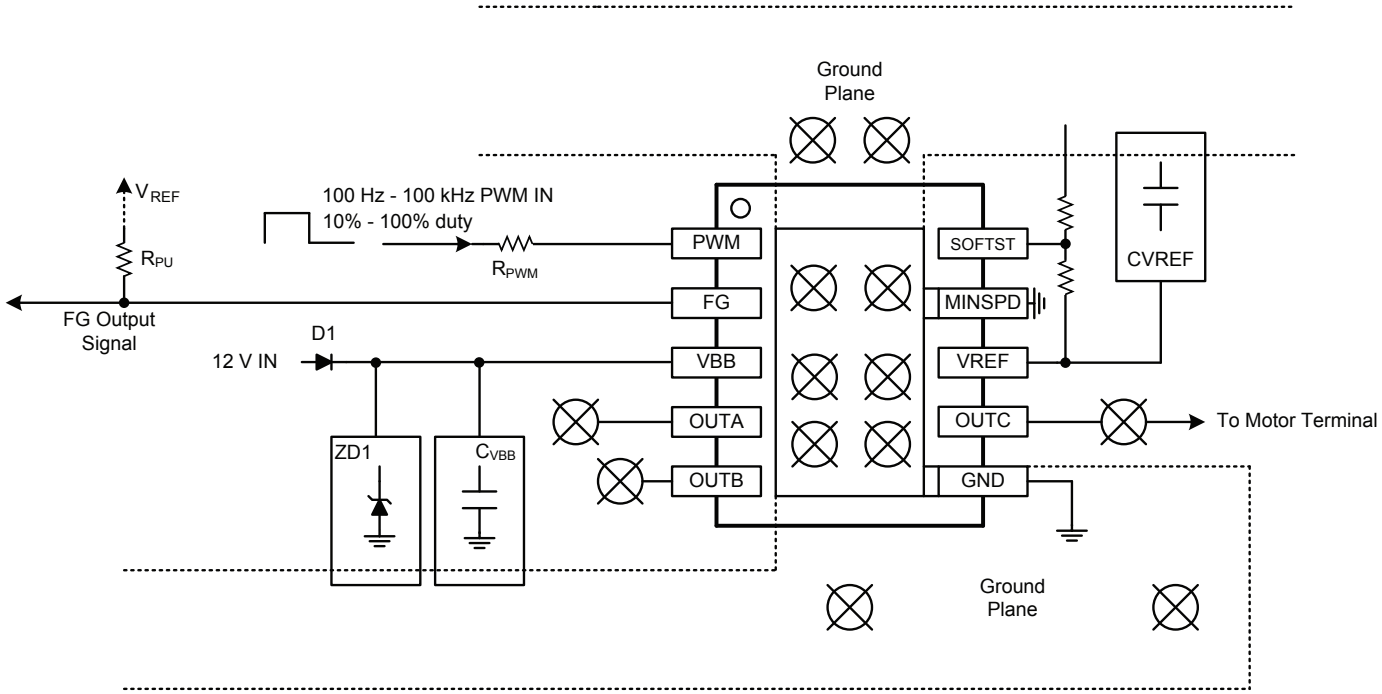
APPLICATION INFORMATION



Typical Application Circuit

Name	Suggested Value	Comment
CVREF	0.1 µF, X5R, 10 V	Ceramic capacitor required
CVBB	4.7 µf to 47 µF	Power Supply Stabilization – Electrolytic or ceramic OK.
R_{FG}	20 kΩ	Optional – pull-up resistor for speed feedback
D1	Not Installed	May be required to isolate motor from system or for reverse polarity protection
ZD1	Not Installed	Optional TVS to limit max V_{BB} due to transients due to motor generation or power line. Suggested to clamp below 18 V (EX : Fairchild SMBJ14A). Typically required if blocking diode D1 used.
R_{PWM}	1 kΩ	Optional – If PWM wired to connector – R_{PWM} will isolate IC pin from noise or overvoltage transients.

Layout Notes:

1. Add thermal vias to exposed pad area. Add ground plane on top and bottom of PCB.
2. Place CVREF and CVBB as close as possible to IC.

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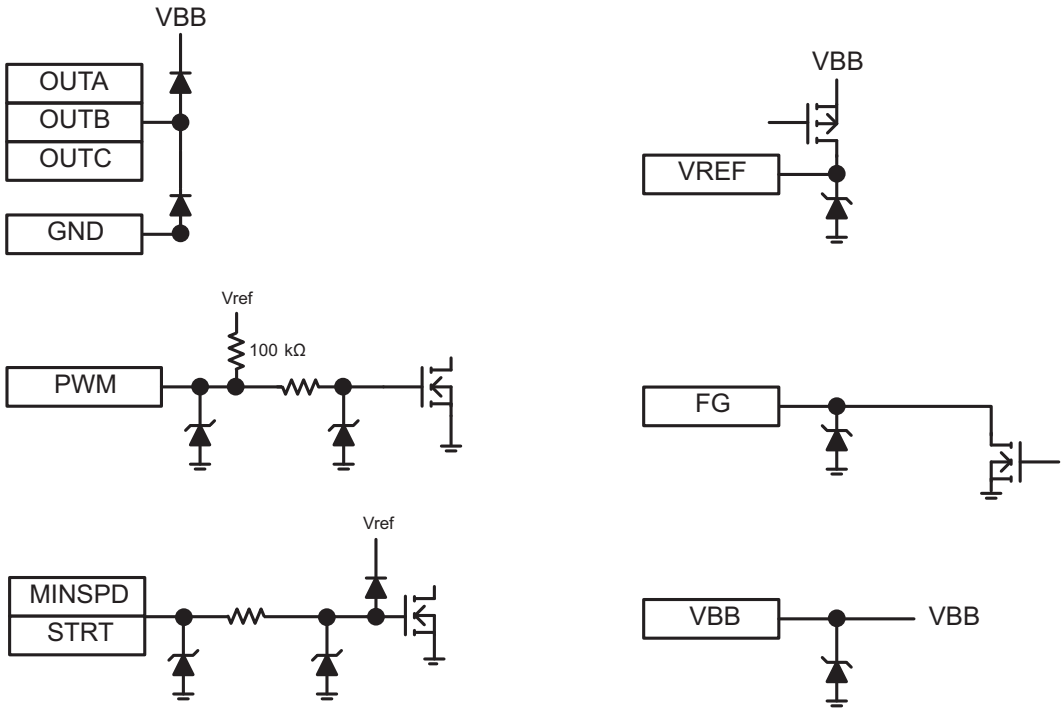
PIN DIAGRAMS



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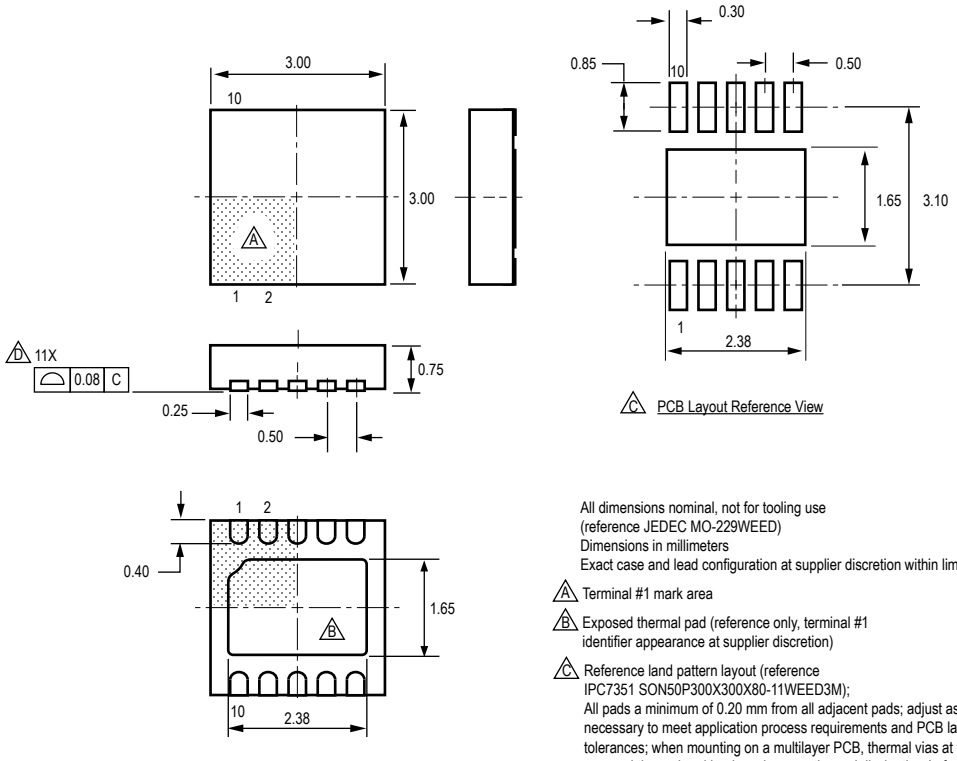
Package EJ, 10-Contact DFN



All dimensions nominal, not for tooling use
(reference JEDEC MO-229WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

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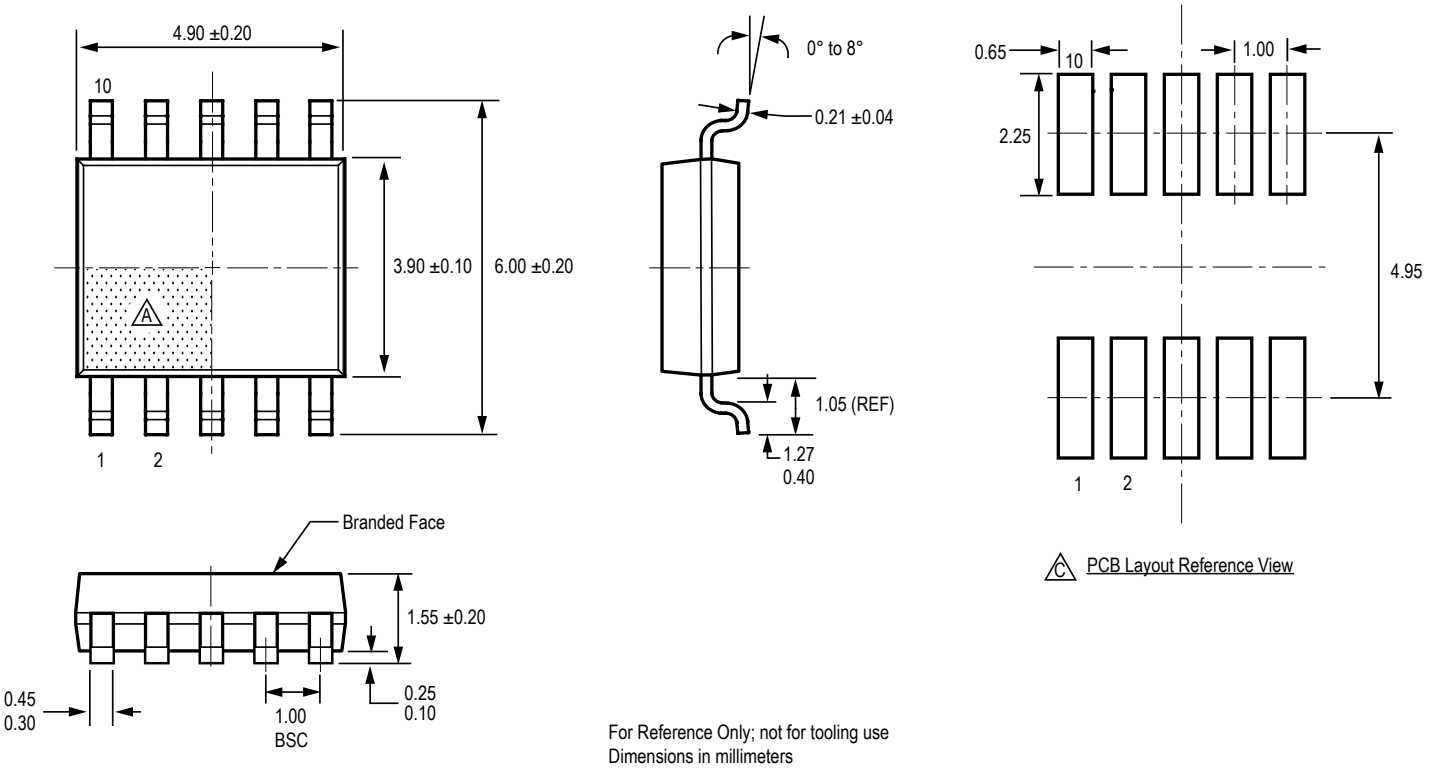
Package LN, 10-Lead SSOP



For Reference Only; not for tooling use
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Branding scale and appearance at supplier discretion

C Reference land pattern layout. All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias near the pin lands can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-7)

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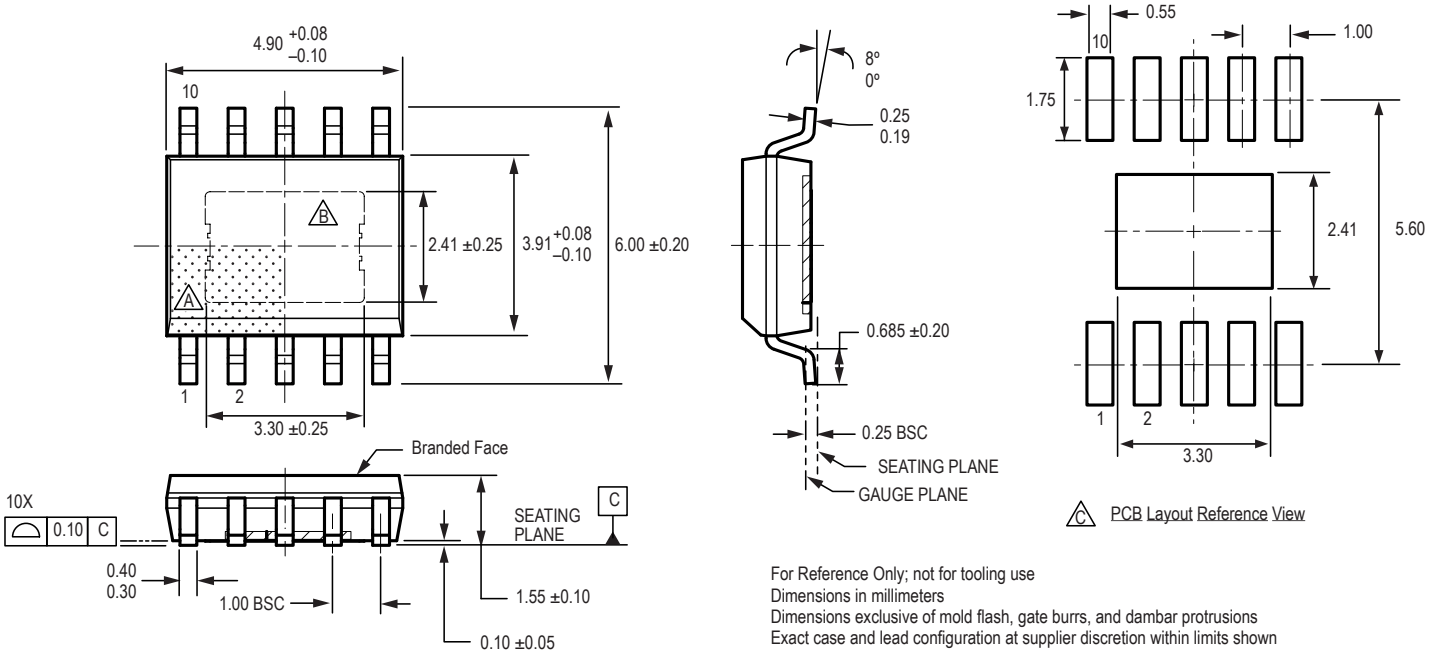
Package LK, 10-Lead eSOIC with Exposed Pad



For Reference Only; not for tooling use
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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Revision History

Number	Date	Description
1	March 20, 2014	Revised Package Drawing
2	July 17, 2014	Added K version
3	March 30, 2016	Corrected LK package drawing dimension
4	July 26, 2018	Minor editorial updates
5	February 5, 2019	Product status changed to Pre-End-of-Life
6	April 1, 2019	Corrected product status

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