High Current Photoflash Capacitor Charger with IGBT Driver for 2 Li+ Batteries

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: December 10, 2012

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

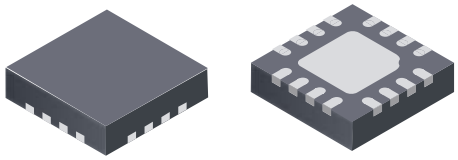
NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

High Current Photoflash Capacitor Charger with IGBT Driver for 2 Li+ Batteries

Features and Benefits

- Wide battery voltage range: 1.5 to 11 V
- Integrated 55 V DMOS switch in very thin profile 3 mm × 3 mm × 0.75 mm nominal height package
- User-adjustable peak current limit, from 0.5 to 1.5 A
- Output voltage sensing on primary side; no resistor divider required
- >75% efficiency
- Fast charging time
- Charge complete indication
- Flexible, high current IGBT driver
  - Independent IGBT driver supply
  - Separate sink and source pins with 6 Ω pull-up and 20 Ω pull-down
  - Interlocked trigger pins improve noise immunity
- No primary-side Schottky diode needed

Package: 16-contact TQFN (suffix ES)



Approximate Scale 1:1

Description

The A8424 charges photoflash capacitors for digital cameras, camcorders, and DSC combos. An integrated 55 V DMOS switch drives the transformer in a flyback topology, optimizing the design for 2-cell Li+ battery input. An integrated IGBT driver with separate source and sink pins allows high performance red-eye reduction implementation.

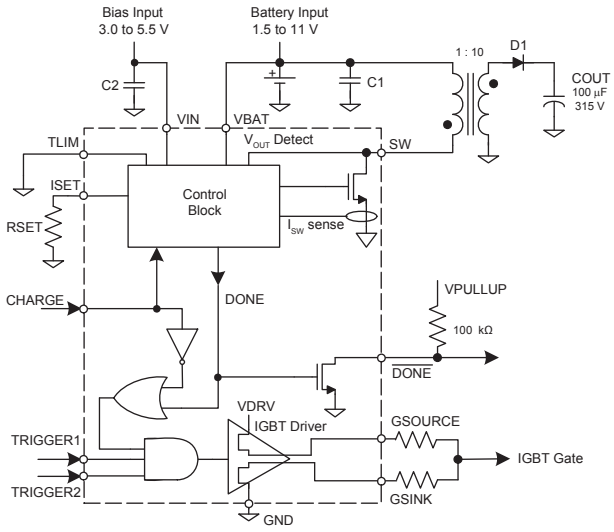
The A8424 offers a programmable peak switch current limit, from 0.5 to 1.5 A, user-adjustable using a resistor to ground. A proprietary control scheme optimizes the capacitor charging time. Low quiescent current and low shutdown current further improve system efficiency and extend battery life.

The A8424 is available in a 16-contact 3 mm × 3 mm TQFN package with exposed pad for enhanced thermal performance. This small, very thin profile (0.75 mm nominal overall height) package is ideal for space-constrained applications. It is lead (Pb) free, with 100% matte-tin leadframe plating.

Applications include:

- SLR camera flash
- Digital camcorder/DSC combo flash
- 2 Li+ input strobe

Typical Application



Selection Guide

Part Number	Packing*
A8424EESTR-T	Tape and reel, 1500 pieces/reel

*Contact Allegro for additional packing options.

Absolute Maximum Ratings*

Characteristic	Symbol	Notes	Rating	Units
SW Pin	V_{SW}		–0.3 to 55	V
VBAT Pin	V_{BAT}		–0.3 to 12	V
VIN Pin	V_{IN}		–0.3 to 7	V
Remaining Pins			–0.3 to V_{IN} + 0.3 V	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

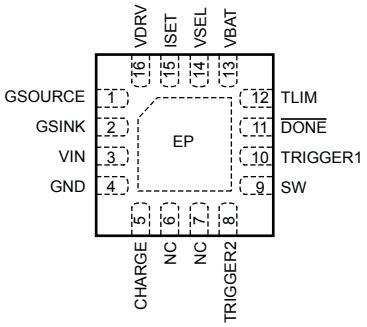
*With respect to GND.

Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB, based on JEDEC standard	47	ºC/W

*Additional thermal information available on Allegro website.

Pin-out Diagram

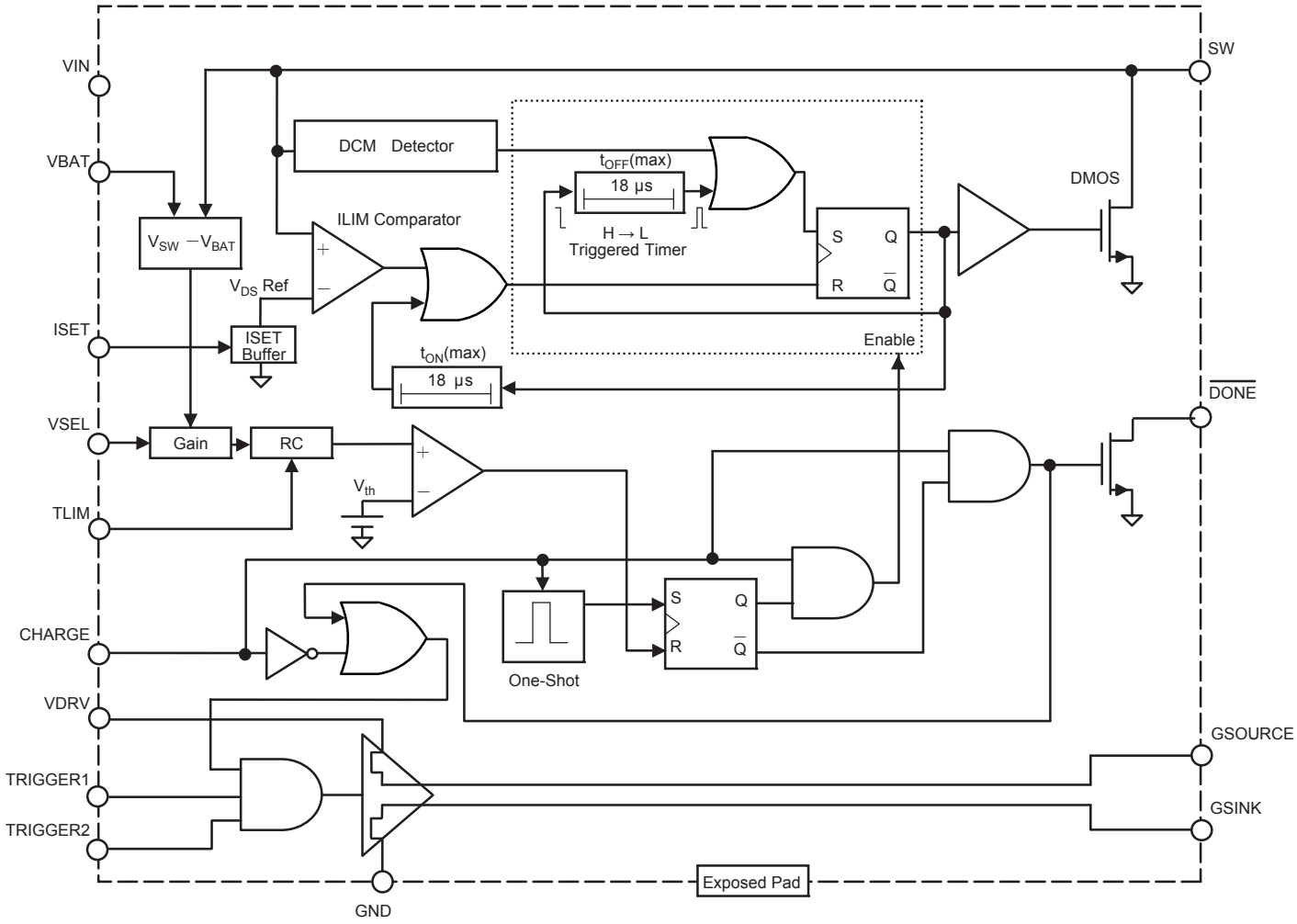


(Top View)

Terminal List Table

Number	Name	Function
1	GSOURCE	IGBT gate drive – source connection
2	GSINK	IGBT gate drive – sink connection
3	VIN	Input voltage; connect to a 3.0 to 5.5 V voltage source
4	GND	Ground connection
5	CHARGE	Pull high to initiate charging; pull low to enter low-power standby mode
6, 7	NC	No connection
8	TRIGGER2	IGBT input trigger 2; internally ANDed with TRIGGER1 pin
9	SW	Drain connection of internal power MOSFET switch; connect to the other terminal of the transformer primary winding
10	TRIGGER1	IGBT input trigger 1; internally ANDed with TRIGGER2 pin
11	$\overline{\text{DONE}}$	Pulls low when output reaches target value and CHARGE pin is high; goes high during charging or whenever the CHARGE pin is low
12	TLIM	Sets time limit for minimum pulse width (secondary-side conduction time); apply logic high for shorter pulses or logic low for longer pulses; see Selection of Transformer section for details
13	VBAT	Battery voltage; connect to the same power supply as used for transformer primary winding
14	VSEL	Output voltage selection; use in conjunction with transformers of differing turns ratios (N = 8, 9, or 10) to achieve desired output voltage and optimal efficiency (this feature is not yet finalized)
15	ISET	Sets the maximum switch current; connect an external resistor to GND to set the target peak current; see Circuit Description section for details
16	VDRV	Supply for IGBT gate driver
–	EP	Exposed pad for enhanced thermal dissipation (not connected electrically)

Functional Block Diagram



ELECTRICAL CHARACTERISTICS typical values valid at V_{IN} = V_{BAT} = 3.6 V, R_{SET} = 33.2 kΩ, I_{SWlim} = 1.0 A, and T_A = 25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBAT Pin Voltage Range[1]	V_{BAT}		1.5	–	11	V
VIN Pin Voltage Range[1]	V_{IN}		3.0	–	5.5	V
UVLO Enable Threshold	V_{INUV}	V_{IN} rising	2.55	2.65	2.75	V
UVLO Hysteresis	$V_{INUVhys}$		–	150	–	mV
Switch Current Limit[2]	$I_{SWlimMAX}$	Maximum, R_{SET} = 22.1 kΩ	1.35	1.5	1.65	A
	$I_{SWlimMIN}$	Minimum, R_{SET} = 66 kΩ	–	0.5	–	A
SW Current Limit to ISET Current Ratio	I_{SWlim}/I_{SET}	R_{SET} = 22.1 kΩ, CHARGE = high	–	27.5	–	kA/A
ISET Pin Voltage While Charging	V_{SET}	R_{SET} = 33.2 kΩ, CHARGE = high	–	1.2	–	V
ISET Pin Internal Resistance	$R_{SET(INT)}$		–	330	–	Ω
Switch On-Resistance	$R_{SWDS(on)}$	V_{IN} = 3.6 V, I_D = 800 mA, T_A = 25°C	–	0.3	–	Ω
Switch Leakage Current[1]	I_{SWlk}	V_{SW} = V_{BAT}(MAX), in shutdown	–	–	1	µA
VIN Pin Supply Current	I_{IN}	Shutdown (CHARGE = low, TRIGGER = low)	–	0.01	1	µA
		Charging done (CHARGE = high, $\overline{\text{DONE}}$ = low)	–	25	100	µA
		Charging (CHARGE = high, TRIGGER = low)	–	2	–	mA
VBAT Pin Supply Current	I_{BAT}	Shutdown (CHARGE = high, TRIGGER = low)	–	0.01	1	µA
		Charging done	–	–	1	µA
		Charging (CHARGE = high, TRIGGER = low)	–	–	50	uA
CHARGE Pin Input Current	I_{CHARGE}	V_{CHARGE} = V_{IN}	–	36	–	µA
CHARGE Pin Input Voltage High[1]	$I_{CHARGE(H)}$	Over input supply range, V_{IN}	1.4	–	–	V
CHARGE Pin Input Voltage Low[1]	$I_{CHARGE(L)}$	Over input supply range, V_{IN}	–	–	0.4	V
CHARGE Pin Pull-down Resistor	R_{CHARGE}		–	100	–	kΩ
Maximum Switch-off Timeout	t_{offMAX}		–	18	–	µs
Maximum Switch-on Timeout	t_{onMAX}		–	18	–	µs
$\overline{\text{DONE}}$ Pin Output Leakage Current[1]	I_{DONElk}		–	–	1	µA
$\overline{\text{DONE}}$ Pin Output Low Voltage[1]	V_{DONEL}	32 µA into $\overline{\text{DONE}}$ pin	–	–	100	mV
Output Comparator Trip Voltage (measured as V_{SW} – V_{BAT})[1]	$V_{OUTTRIP}$	VSEL = GND	31	31.5	32	V
		VSEL = open	–	35	–	V
		VSEL = VIN	–	39.4	–	V
Output Comparator Overdrive	V_{OUTOV}	200 ns pulse width (90% to 90%) TLIM = high	–	200	400	mV
Minimum dV/dt for ZVS Comparator	dV/dt	Measured at SW pin	–	20	–	V/µs
TLIM Pin Input Voltage	V_{TLIM}	TLIM = high	1.4	–	–	V
		TLIM = low	–	–	0.4	V

Continued on the next page …

ELECTRICAL CHARACTERISTICS (continued) typical values valid at V_{IN} = V_{BAT} = 3.6 V, R_{SET} = 33.2 kΩ, I_{SWlim} = 1.0 A, and T_A=25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
IGBT Driver						
VDRV Pin IGBT Driver Supply Voltage[1]	V_{DRV}		3	–	5.5	V
TRIGGERx Pins Input Current	I_{TRIG}	$V_{TRIGGER}$ = V_{IN}	–	36	–	µA
TRIGGERx Pins High Input Voltage[1]	$V_{TRIG(H)}$	Over input supply range, V_{IN}	1.4	–	–	V
TRIGGERx Pins Low Input Voltage[1]	$V_{TRIG(L)}$	Over input supply range, V_{IN}	–	–	0.4	V
TRIGGERx Pins Pull-down Resistor	R_{TRIGPD}		–	100	–	kΩ
GSOURCE On-Resistance to VDRV	$R_{SrcDS(on)}$	V_{DRV} = 3.6 V, $V_{GSOURCE}$= 1.8 V	–	5	–	Ω
GSINK On-Resistance to GND	$R_{SnkDS(on)}$	V_{DRV} = 3.6 V, V_{GSINK}= 1.8 V	–	20	–	Ω
Propagation Delay (Rising)	t_{dr}	Connect GSOURCE to GSINK, R_{GATE} = 12 Ω, C_{LOAD} = 6500 pF, V_{DRV} = 3.6 V	–	30	–	ns
Propagation Delay (Falling)	t_{df}		–	140	–	ns
Output Rise Time	t_r		–	80	–	ns
Output Fall Time	t_f		–	320	–	ns

[1]Specifications over the range T_A= –40°C to 85°C; guaranteed by design and characterization.
[2]Current limit guaranteed by design and correlation to static test. Refer to Application Information section for peak current in actual circuits.

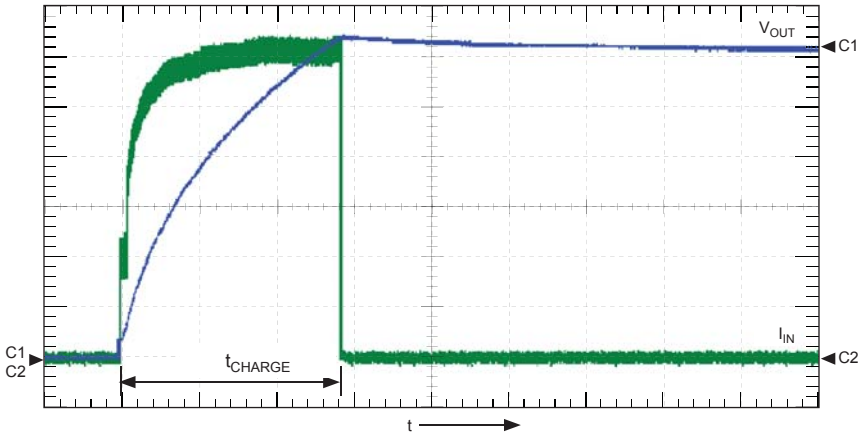
Performance Characteristics

Charging Time at Various Peak Current Levels

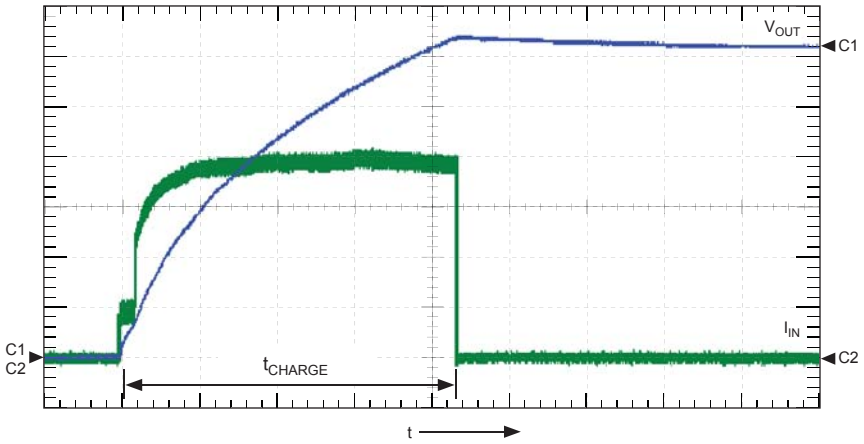
Common Parameters		
Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C2	I_{IN}	100 mA
t	time	1 s
Conditions	**Parameter**	**Value**
	V_{IN}	3.6 V
	V_{BAT}	5 V
	C_{OUT}	100 µF/ 330 V UCC

Transformer = TDK LD5T565630T-003, L_P = 10.5 µH, N = 10.2

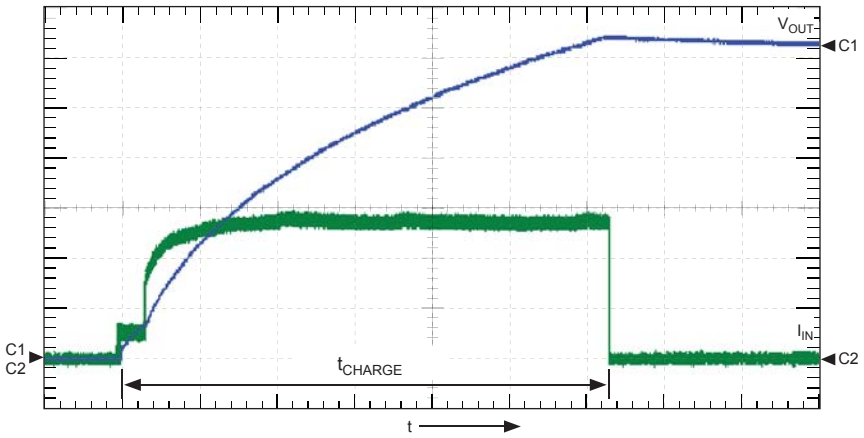
Conditions	Parameter	Value
	R_{SET}	22.1 kΩ
	I_{SWlim}	≈1.5 A



Conditions	Parameter	Value
	R_{SET}	33.2 kΩ
	I_{SWlim}	≈1.0 A

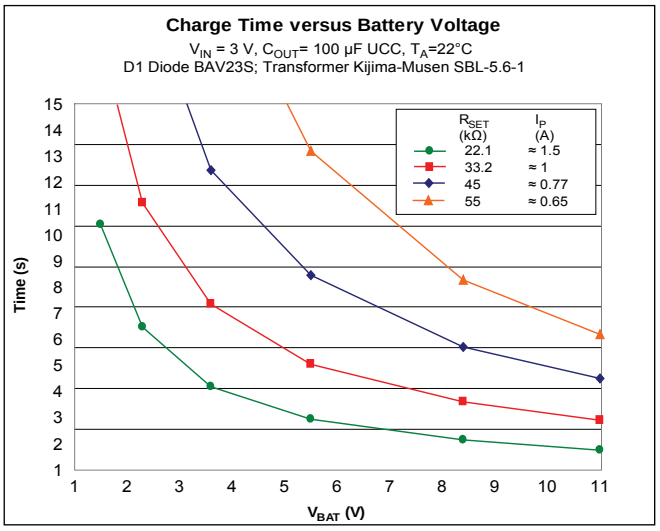


Conditions	Parameter	Value
	R_{SET}	45 kΩ
	I_{SWlim}	≈0.8 A

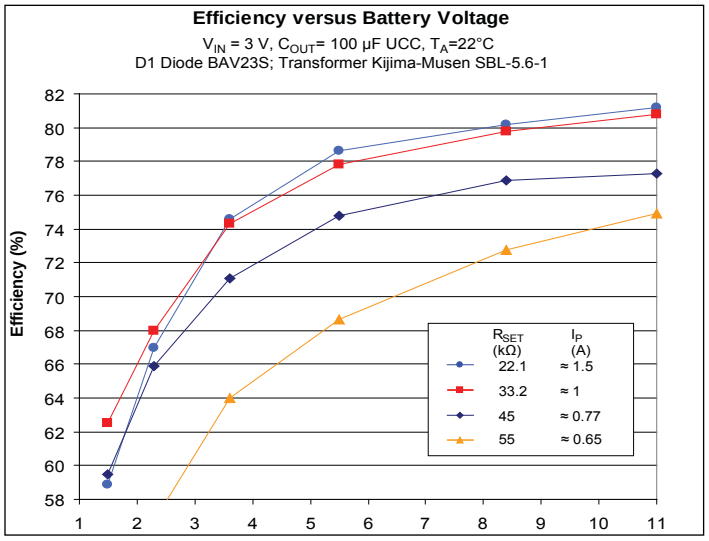


Performance Characteristics

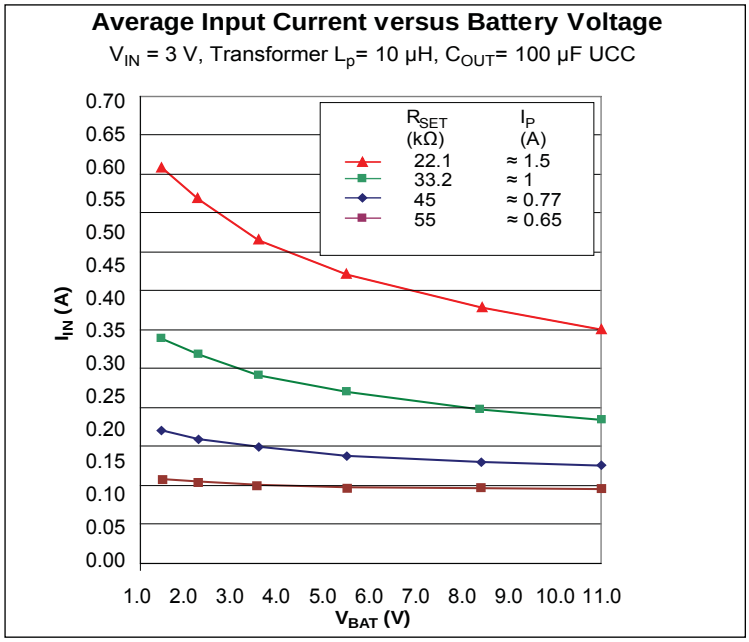
0 to 325 Volts



C_{OUT}= 100 µF. For larger or smaller capacitances, charging time scales proportionally.



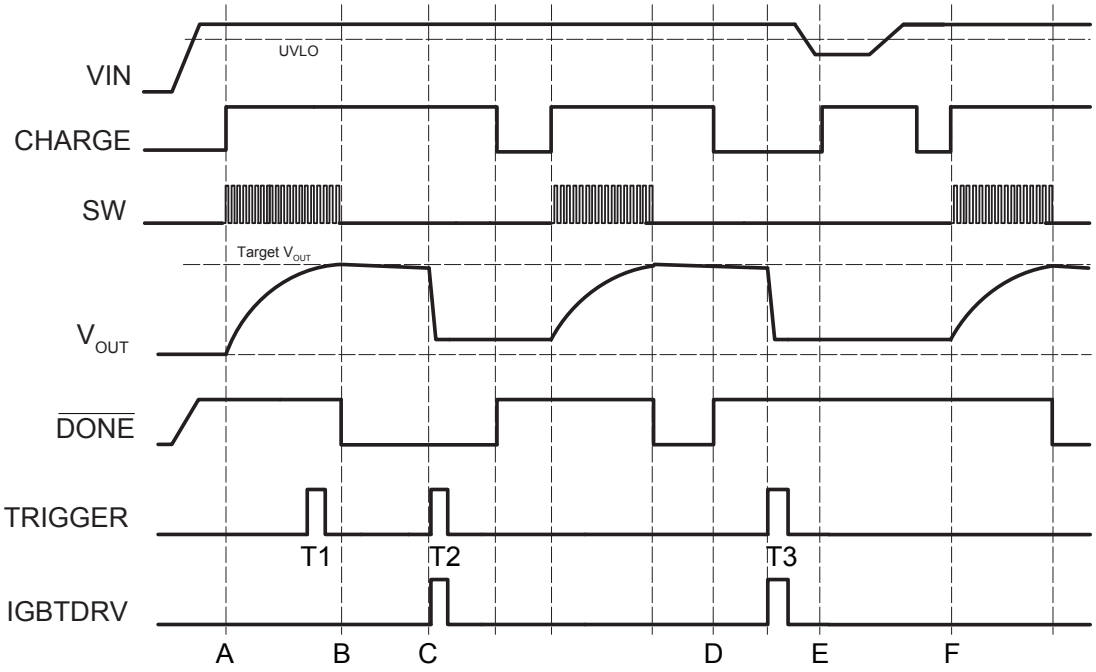
This data was obtained using a Kijima-Musen SBL-5.6-1 transformer (L_P = 9.8 µH, N = 10.2). Highest efficiency is achieved at high battery voltage and large peak current (1 to 1.5 A). At lower current (< 1 A), switching frequency increases and so do switching losses. Therefore a transformer with higher primary inductance is preferred when operating at lower current.



The average input current decreases with higher V_{BAT}. .

Timing and IGBT Interlock Function

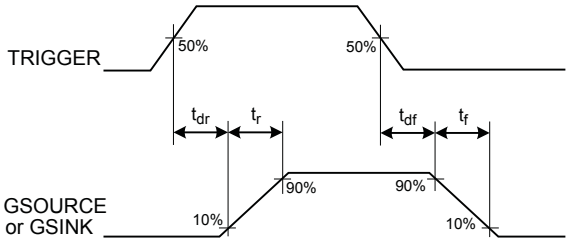
The two TRIGGER signals are internally ANDed together. As shown in the timing diagram, below, triggering is prohibited during the initial charging process. This prevents premature firing of the flash before the output capacitor has been charged to its target voltage. Refer to the section IGBT Gate Driver Interlock for details.



Explanation of Events

A	Start charging process by pulling CHARGE pin high, provided that V_{IN} is above the UVLO level. Triggering (T1) is locked during the charging process (CHARGE and $\overline{DONE}$ pins are both high).
B	Charging stops when V_{OUT} reaches the target voltage level. Triggering (T2) is enabled after completion of charging (CHARGE pin is high and $\overline{DONE}$ pin is low).
C	Start a new charging process with a low-to-high transition at the CHARGE pin.
D	Pull the CHARGE pin low to put the controller into the low-power standby mode. Triggering (T3) is always enabled when CHARGE is low.
E	Charging does not start, because V_{IN} is below the UVLO level when the CHARGE pin goes high.
F	After V_{IN} goes above the UVLO level, another low-to-high transition at the CHARGE pin is required to start the charging process.

IGBT Drive Timing Definition



Application Information

Circuit Description

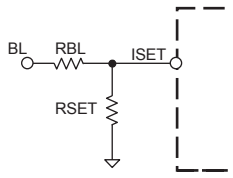
The A8424 is a photoflash capacitor charger control IC with a high current limit (up to 1.5A) and low $R_{DS(on)}$ (0.35 Ω maximum). The IC also integrates an IGBT driver for strobe operation of the flash tube, dramatically saving board space in comparison with discrete solutions for strobe flash operation.

The IC is turned on by a low-to-high signal on the CHARGE pin. When the charging cycle is initiated, the primary current ramps up linearly at a rate determined by the battery voltage and the primary side inductance. When the primary current reaches the set limit, the internal MOSFET is turned off immediately to allow the energy to be pushed into the photoflash capacitor through the secondary winding. The secondary current drops linearly as the output capacitor is charged. The charging cycle starts again when the transformer flux is reset or after a predetermined time period (18 µs maximum off-time) has passed, whichever occurs first.

The peak switch current limit is determined by a resistor, RSET, connected between the ISET pin and GND. The value of RSET can be between 22 and 66 kΩ. This generates an ISET current between 18 and 55 µA, which corresponds to a desired peak switch current in a range from 0.5 to 1.5 A.

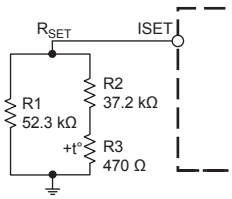
Smart Current Limit (Optional)

With the help of some simple external logic, the user can change the charging current according to the battery voltage. For example, assume that I_{SET} is normally 50 µA (for I_{SWlim} = 1.5 A). Referring to the following illustration, when the battery voltage drops below 2.5 V, the signal at BL (battery-low) should go high. The resistor RBL, connecting BL to the ISET



pin, then injects 20 µA into RSET. This effectively reduces ISET current to 30 µA (for I_{SWLIM} = 0.9 A). If necessary, BL can also be connected to the TLIM pin to reduce the minimum pulse width. The disadvantage of this method is that 20 µA flows continuously while BL is high.

In another example of a possible application, we can make use of a PTC thermistor to decrease the switch current limit when the board temperature exceeds 65°C. Referring to the following figure, R3 is a PTC type thermistor such as the Murata PRF18BG471QB1RB.



In this configuration, the peak currents at various PCB temperatures are as follows:

T_{PCB} (°C)	R_3 (kΩ)	R_{SET} (kΩ)	I_{peak} (A)
25	0.470	22.0	1.5
65	4.7	23.3	1.4
80	47.0	32.3	1.0

Selection of Transformer

1. The transformer turns ratio ($N = N_S / N_P$) determines the output voltage, according to the following formula:

$$V_{OUT} = K \times N - V_d \,, \qquad (1)$$

where K is 31.5 (when VSEL is connected to GND), and V_d is the forward drop of the output diode (approximately 2 V).

2. The primary inductance, L_P, determines the on-time of the switch, as follows:

$$t_{on} = -L_P / R \times \ln\left(1 - I_{SWlim} \times R / V_{BAT}\right) , \qquad (2)$$

where R is the total resistance in the primary current path (including $R_{SWDS(on)}$ and the DC resistance of the transformer).

If V_{BAT} is much larger than $I_{SWlim} \times R$, then t_{on} can be approximated using the following formula:

$$t_{on} = I_{SWlim} \times L_P / V_{BAT} \,. \qquad (3)$$

3. The secondary inductance, L_S, determines the off-time of the switch, as follows:

$$t_{off} = (I_{SWlim} / N) \times L_S / V_{OUT} \,. \qquad (4)$$

Because $L_S / L_P = N \times N$:

$$t_{off} = (I_{SWlim} \times L_P \times N) / V_{OUT} \,. \qquad (5)$$

The minimum pulse width for t_{off} determines the minimum primary inductance required for the transformer. For example, if $I_{SWlim} = 0.7$ A, N = 10, and $V_{OUT} = 315$ V, then L_P must be at least 9 µH in order to keep t_{off} at 200 ns or longer. In general, choosing a transformer with larger L_P results in higher efficiency (because the higher the value of L_P, the lower the switch frequency, and hence the lower the switching loss). But transformers with higher L_P ratings also require more windings and larger magnetic cores. Therefore a trade-off must be made between transformer size and efficiency.

In order to provide greater design flexibility with different transformer, the TLIM pin can be used to select between two minimum pulse width settings, 200 and 400 ns. When operating at low current or when using a transformer with low inductance, the SW pulse width is very narrow, so TLIM should be pulled high to enable the IC to operate down to $t_{off} = 200$ ns. Conversely, when the SW pulse width is wider than 400 ns, it is generally better to pull TLIM low. This is because when operating at high current, leakage inductance and other parasitics may cause excessive peaking of the SW waveform. Setting TLIM to low reduces the effects of peaking and provides a more accurate target voltage in this case. The relationship between t_{off} and switch output is shown in figure 1.

The A8424 has an additional feature that allows wider choices of transformers. The VSEL pin selects the values of K corresponding to values of N. For the target output voltage of approximately 315 V, the values of K would be:

N	K
10	31.5
9	35
8	39.4

By using transformers with lower turns ratios, an efficiency gain of 1% to 2% can be expected typically.

For example, if VSEL is open and a transformer of N = 9 is used, then applying equation 1, the final output voltage will be:

$$V_{OUT} = K \times N - V_d = 35 \times 9 - 2 \approx 313 \text{ V} \,.$$

Is desired, VSEL can also be used to achieve a higher output voltage. For example, if we use a transformer with N = 10 but set K = 35, then the final output voltage would be approximately 348 V instead.

Selection of Switching Current Limit

The A8424 features continuously adjustable peak switching current between 0.5 and 1.5 A. This is done by selecting the value of the external resistor RSET (connected between the ISET pin and GND), which determines the ISET bias current, and therefore the switching current limit, I_{SWlim}.

To the first order approximation, I_{SWlim} is related to I_{SET} and R_{SET} by the following equation:

$$I_{SWlim} = I_{SET} \times K$$

$$= (V_{SET} \times R_{SET}) \times K \, , \qquad (6)$$

where $K \approx 28000$ when the IC bias voltage, V_{IN}, is 3.6 V.

In real applications, the switching current limit is affected by bias voltage, battery voltage, and the transformer primary inductance, L_P. If necessary, the following expressions can be used to determine I_{SWlim} more accurately:

$$I_{SET} = V_{SET} / (R_{SET} + R_{SET(INT)} - K \times R_{G(INT)}) \, , (7)$$

where $R_{SET(INT)}$ is the internal resistance of the ISET pin (330 Ω typical), $R_{G(INT)}$ is the internal resistance of the bonding wire for the GND pin (27 mΩ typical), and:

$$I_{SWlim} = I_{SET} \times (K' + V_{IN} \times K'') + (V_{BAT} / L_P) \times t_d \, , \qquad (8)$$

where K' = 24350, K" = 1040, and t_d = delay in SW turn-off (0.12 µs typical).

Figure 2 shows the relationship between R_{SET} and I_{SWlim} at different bias voltages, V_{IN}, when battery voltage, V_{BAT}, is fixed at 3.6 V.

Figure 3 shows the relation between RSET and I_{SWlim} at different battery voltages, when bias voltage is fixed at 3.6 V). Note that the spread is inversely proportional to the primary inductance of transformer used.

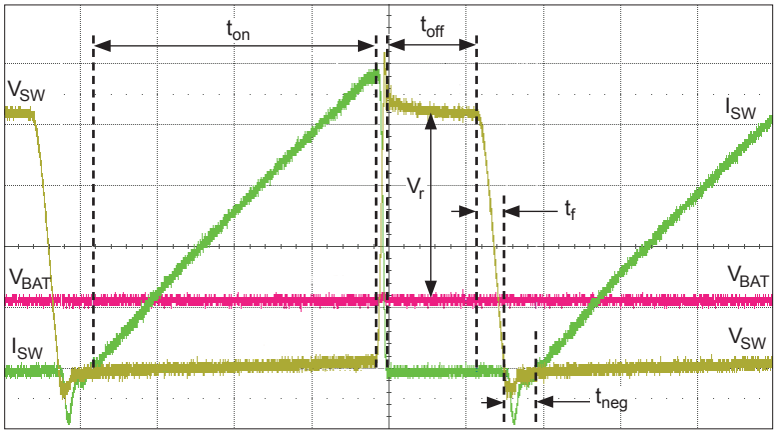


Figure 1. Relationship of t_{off} and switch output.

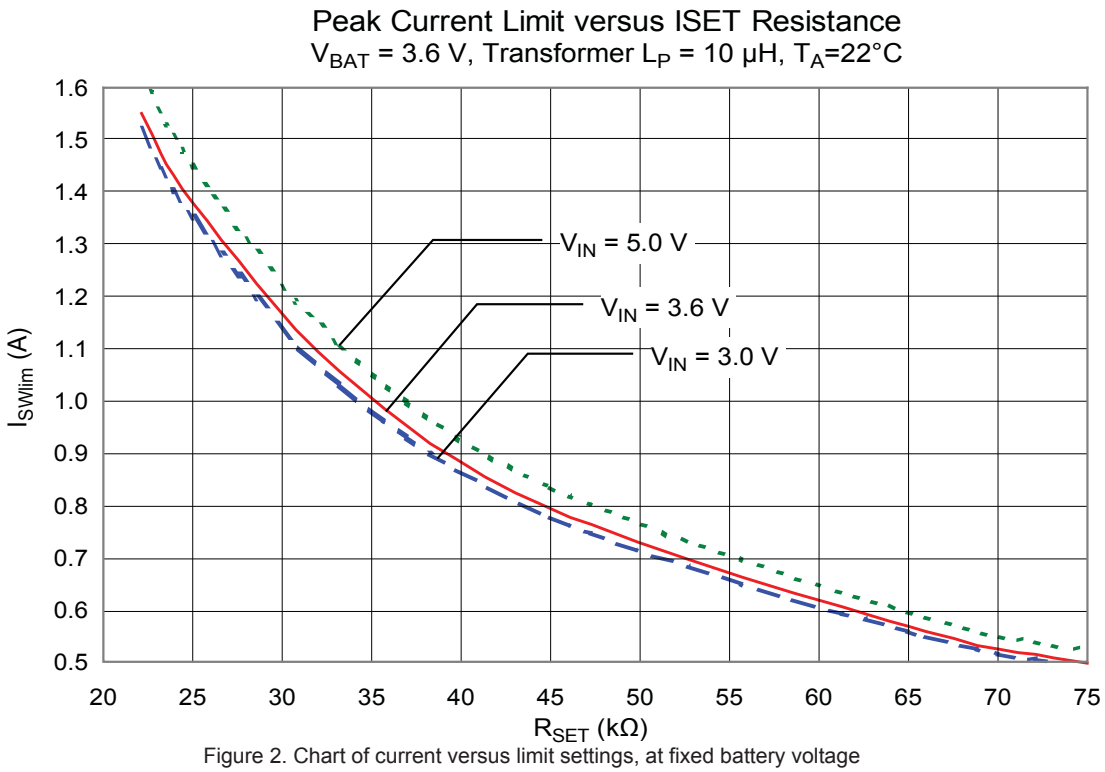


Figure 2. Chart of current versus limit settings, at fixed battery voltage

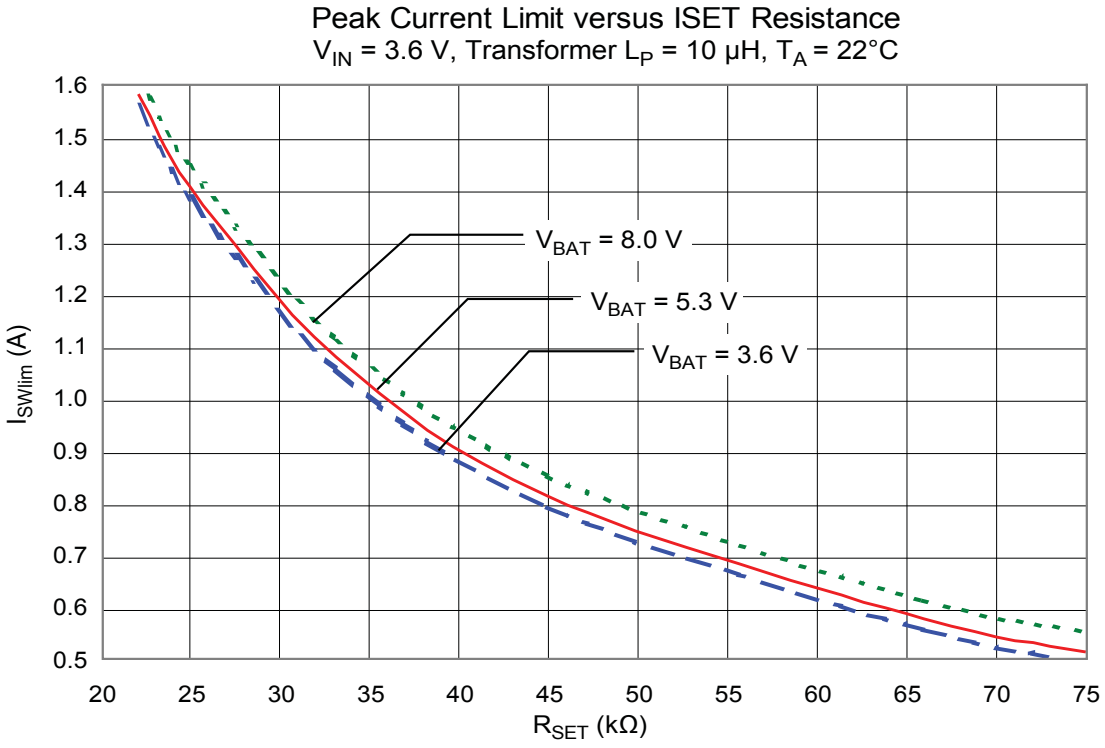


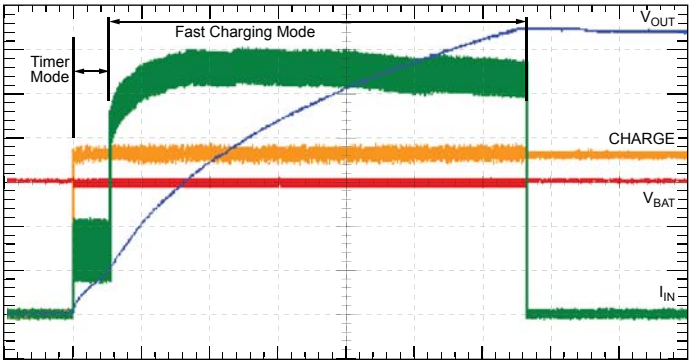
Figure 3. Chart of current versus limit settings, at fixed bias voltage

Fast Charging and Timer Modes

The A8424 achieves fast charging time and high efficiency by operating in discontinuous conduction mode (DCM) with zero-voltage-switching (ZVS). This operation is shown in figure 4.

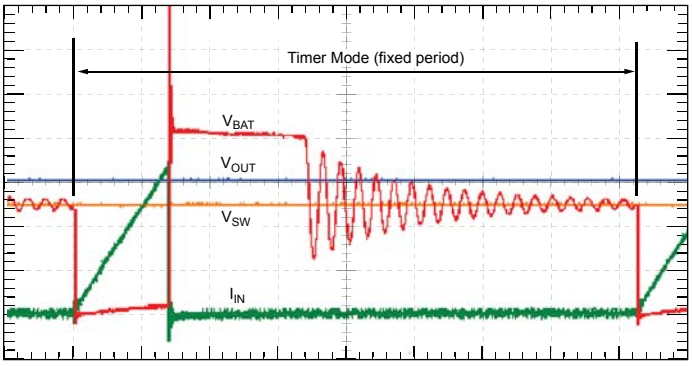
The IC operates in Timer mode when beginning to charge a completely discharged photoflash capacitor, usually when the output voltage, V_{OUT}, is less than approximately 40 V (depending on the inductance of transformer used). Timer mode has a fixed switching period of approximately 18 µs. One advantage of Timer mode is that it limits the initial battery current surge and thus acts as a "soft-start," as shown in figure 5.

As soon as sufficient voltage has built up at the output capacitor, the IC changes into Fast-Charging mode.



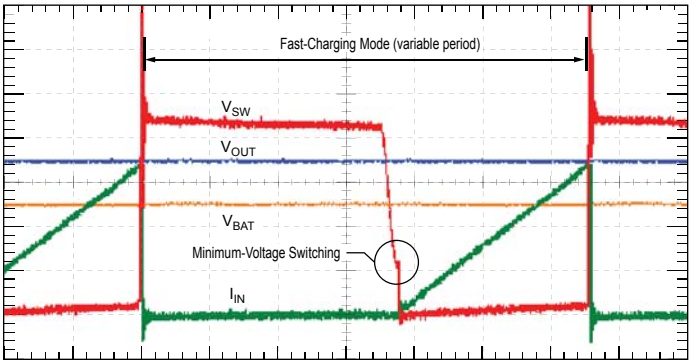
t = 500 ms/div; V_{OUT} =50 V/div; I_{IN} =100 mA/div; V_{IN} = 3.6 V; V_{BAT} = 5.0 V; R_{SET} = 22.1 kΩ (I_P≈ 1.5 A); C_{OUT} = 100 µF/300 V; Transformer T-19-083

Figure 4. Relationship of Timer mode and Fast Charging mode



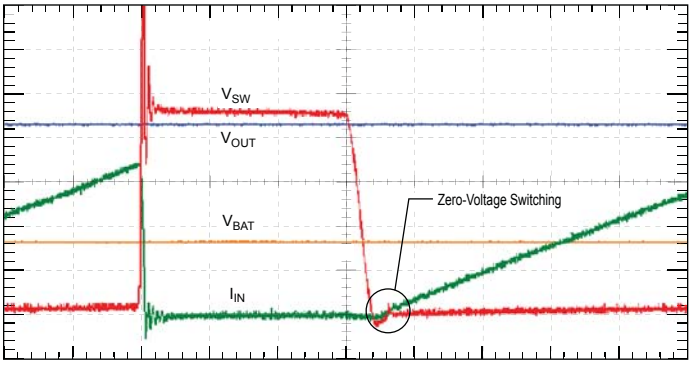
t = 2 µs/div; V_{IN} = 3.6 V; V_{BAT} = 5 V; V_{OUT} = 30 V; Transformer L_P= 10 µH

Figure 5. Timer mode (CCM), V_{OUT} < 40 V



t = 1 µs/div, V_{IN} = 3.6 V, V_{BAT} = 5 V, V_{OUT} = 35 V, Transformer L_P= 10 µH

Figure 6. Fast-charging mode (DCM), V_{OUT} > 35 V



t = 0.5 µs/div, V_{IN} = 3.6 V, V_{BAT} = 5 V, V_{OUT} = 85 V

Figure 7. Zero-voltage switching

As shown in figure 6, in this mode the next switching cycle starts after the secondary-side current has stopped flowing, and the switch voltage has dropped to a minimum value. A special dV/dt detection circuit is used to allow minimum-voltage switching, even if the SW voltage does not drop to zero volts. This enables fast-charging to start earlier than previously possible, thereby reducing the overall charging time.

When output voltage is high enough (such that the reflected voltage, $V_r = V_{OUT}/ N$, is greater than V_{BAT}), true zero-voltage switching is achieved, which further improves efficiency as well as reducing switching noises (figure 7).

Components Recommendation

Selection of the flyback transformer should be based on the peak current, according to the following table:

I_{Peak} Range (A)	Supplier	Part Number	L_P (µH)	N
0.5 to 1.5	Tokyo Coil	T-16-024A	12.8	10.25
0.6 to 1.2	TDK	LDT565630T-003	10.5	10.2
0.75 to 1.0	TDK	LDT565620ST-203	8.2	10.2

IGBT Gate Driver Application

The integrated IGBT driver is used to drive an external flash trigger IGBT. Separate GSOURCE and GSINK pins allow the user to adjust IGBT turn-on and turn-off rise times. For the Electrical Characteristics table in this document, IGBT drive timing is defined with the GSOURCE and GSINK pins connected together, and supplying a load comprising a 12 Ω resistor and a 6500 pF capacitor.

IGBT Gate Driver Interlock

The TRIGGER1 and TRIGGER2 pins are ANDed together inside the IC to control the IGBT gate driver. If only one trigger pin is used, the other trigger pin must be tied to the VIN pin to ensure that the unused trigger pin is at logic high.

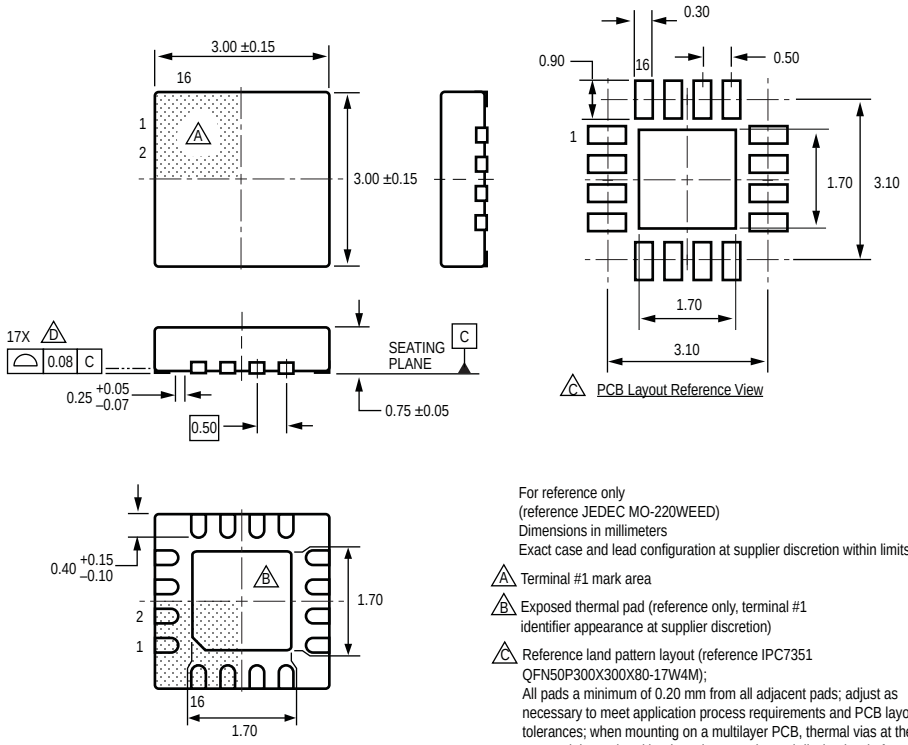
Triggering is disabled (locked) during charging. This is to prevent switching noise from interfering with the IGBT driver. After the CHARGE pin goes high (at the start of a charging cycle), the IC must wait for completion of the charging cycle ($\overline{DONE}$ goes low) before triggering can be enabled, according to the following chart:

Conditions		Resulting State
CHARGE	$\overline{DONE}$	IGBT Gate Driver
Low	Don't Care	Enabled
High	High	Disabled
High	Low	Enabled

The IGBT gate driver is always enabled when the CHARGE pin is low.

It is up to the system-level programming to ensure that a trigger signal is not applied without sufficient voltage at the output capacitor.

Package ES, 3 mm x 3 mm 16-Contact TQFN
with Exposed Thermal Pad



For reference only
(reference JEDEC MO-220WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P300X300X80-17W4M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Revision History

Revision	Revision Date	Description of Revision
Rev. 1	April 19, 2012	Finalize $R_{\theta JA}$, update Selection Guide, and miscellaneous format changes

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