ACS37030 and ACS37032

DC to 5 MHz Bandwidth, Galvanically Isolated, High-Accuracy Current Sensor IC with Reference Output (ACS37030) or Fault (ACS37032)

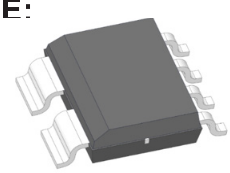
FEATURES AND BENEFITS

- High operating bandwidth for fast control loops or where high-speed switching currents are monitored
  - □ DC to 5 MHz bandwidth
  - □ 40 ns typical response time
- High accuracy and low noise
  - □ ±2% sensitivity error over temperature
  - □ ±10 mV maximum offset voltage over temperature
  - □ 50 mA_{RMS} input referred noise
  - □ 3.3 V non-ratiometric supply operation
  - □ Differential sensing immune to external magnetic fields
- VREF output voltage for differential routing in noisy application environments (ACS37030)
- FAULT output for fast open drain overcurrent detection (ACS37032)
- Highly isolated compact surface-mount package
  - □ 3500 V_{RMS} rated isolation voltage
  - □ 840 V_{RMS} / 1188 V_{DC} basic isolation voltages
  - □ 420 V_{RMS} / 594 V_{DC} reinforced isolation voltages
- Wide operating temperature, –40°C to 150°C
- AEC-Q100 Grade 0 qualified

PACKAGE:

6-pin SOIC
(suffix LZ)

Not to scale



CB Certificate Number:
US-42934-UL

DESCRIPTION

The ACS37030/2 is a fully integrated current sensor IC that senses current flowing through the primary conductor. Two signal paths are used: a Hall-effect element path to capture DC and low-frequency current information, and an inductive coil path to capture high-frequency current information. These two paths are summed to allow for sensing of a wide frequency band with a single device. The properties of the coil increase SNR as frequency increases, minimizing noise seen at the output.

The internal construction provides high isolation by magnetically coupling the field generated by current flow in the conductor to the fully monolithic Hall and coil IC. The current is sensed differentially by two Hall plates and two coils that subtract out interfering common-mode magnetic fields. The IC has no physical connection to the integrated current conductor and provides a 3500 V_{RMS} isolation voltage between the primary and secondary signal leads of the package. This high rating provides a basic working voltage of 840 V_{RMS}.

Both zero current reference (ACS37030) and overcurrent fault with internal pull up (ACS37032) options are available.

The ACS37030/32 is provided in a six-lead custom SOIC surface mount package with the current conductor leads formed together for a reduced resistance of 0.6 mΩ. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free.

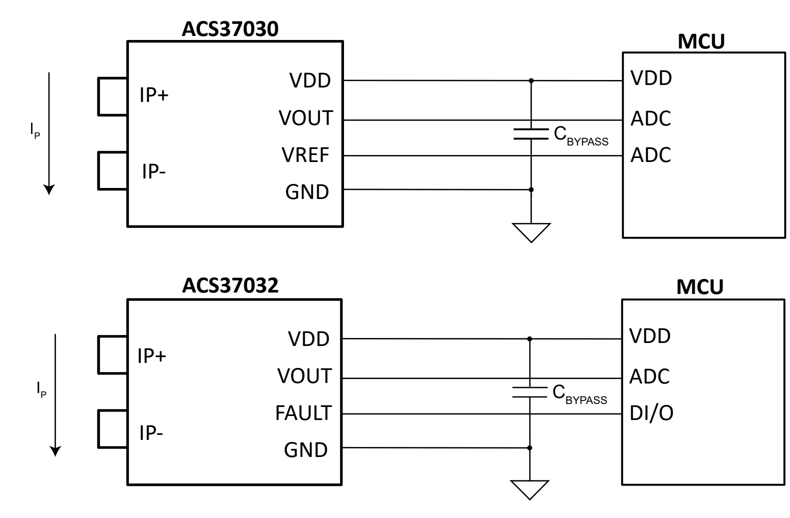
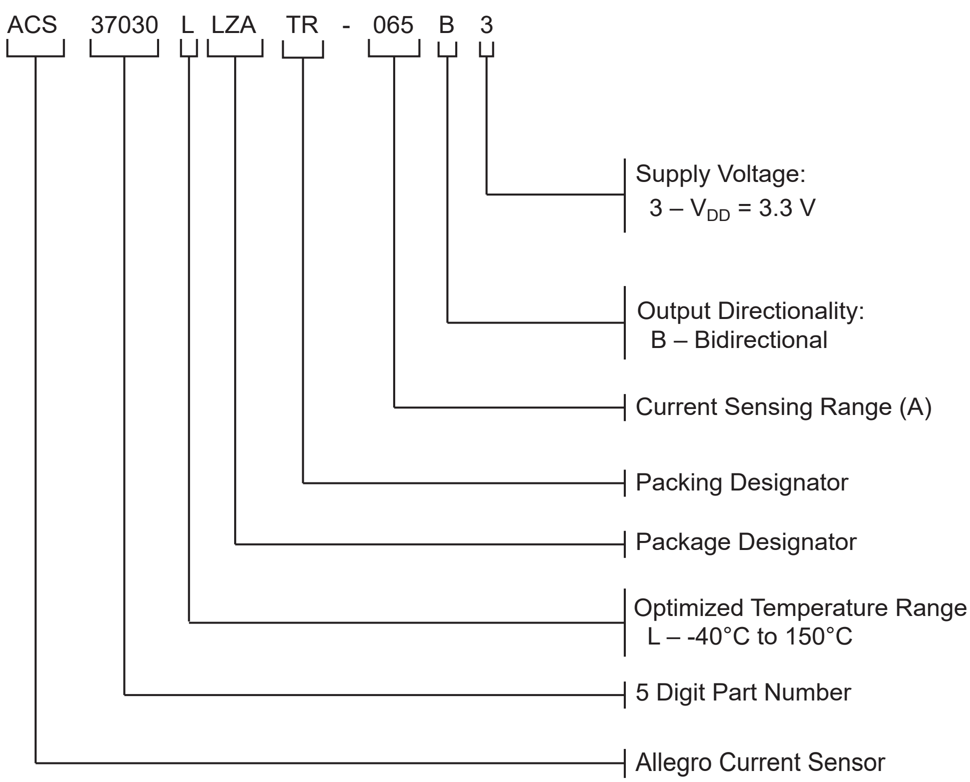


Figure 1: Typical Application Circuit

The ACS37030/32 outputs an analog signal, V_{OUT}, that varies linearly with the bidirectional AC or DC primary current, I_P, within the range specified.

SELECTION GUIDE

Part Number	Current Sensing Range, I_{PR} (A)	Sensitivity (mV/A)	V_{DD} (V)	V_{QVO} (V)	Optimized Temperature Range T_A (°C)	Packing
ACS37030LLZATR-020B3	±20	66	3.3	1.65	–40 to 150	Tape and reel, 3000 pieces per reel
ACS37030LLZATR-040B3	±40	33				
ACS37030LLZATR-065B3	±65	20.3				
ACS37032LLZATR-020B3	±20	66				
ACS37032LLZATR-040B3	±40	33				
ACS37032LLZATR-065B3	±65	20.3				



ABSOLUTE MAXIMUM RATINGS[1]

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{DD}		–0.5 to 4	V
Forward Output Voltage	V_O	Applies to V_{OUT}, V_{REF}, and FAULT	–0.5 to V_{DD} + 0.5 (< 3.8)	V
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Value	Units
Withstand Strength [1]	V_{ISO}	Agency rated for 60 seconds per UL 62368-1 (edition 3)	3500	V_{RMS}
Impulse Withstand	$V_{IMPULSE}$	Tested ±5 pulses at 2/minute in compliance to IEC 61000-4-5, 1.2 µs (rise) / 50 µs (width)	5000	V_{PK}
Working Voltage for Basic Isolation	V_{WVBI}	Maximum approved working voltage for basic (single) isolation according to UL 62368-1 (edition 3)	1188	V_{PK} or V_{DC}
			840	V_{RMS}
Working Voltage for Reinforced Isolation	V_{WVRI}	Maximum approved working voltage for reinforced isolation according to UL 62368-1 (edition 3)	594	V_{PK} or V_{DC}
			420	V_{RMS}
Clearance	D_{CL}	Minimum distance through air from IP leads to signal leads	4.2	mm
Creepage	D_{CR}	Minimum distance along package body from IP leads to signal leads	4.2	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	54	µm
Comparative Tracking Index	CTI	Material Group I	>600	V

[1] Production tested for 1 second in accordance with UL 62368-1 (edition 3).

PACKAGE CHARACTERISTICS

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Internal Conductor Resistance	R_{IC}	T_A = 25°C	–	0.68	–	mΩ
Internal Conductor Inductance	L_{IC}	T_A = 25°C	–	2.4	–	nH
Moisture Sensitivity Level	MSL	Per IPC/JEDEC J-STD-020	–	2	–	–

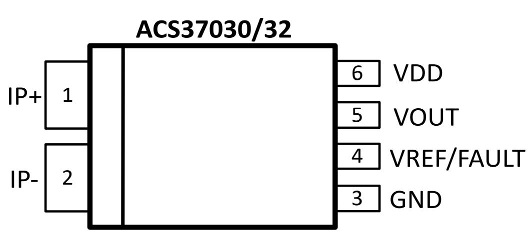


Figure 2: LZ Package Pinout Diagram

Terminal List

Number	Name	Description
1	IP+	Positive terminal for current being sensed
2	IP–	Negative terminal for current being sensed
3	GND	Device ground terminal
4	VREF/FAULT	Reference or overcurrent fault output
5	VOUT	Analog output signal
6	VDD	Device power supply terminal

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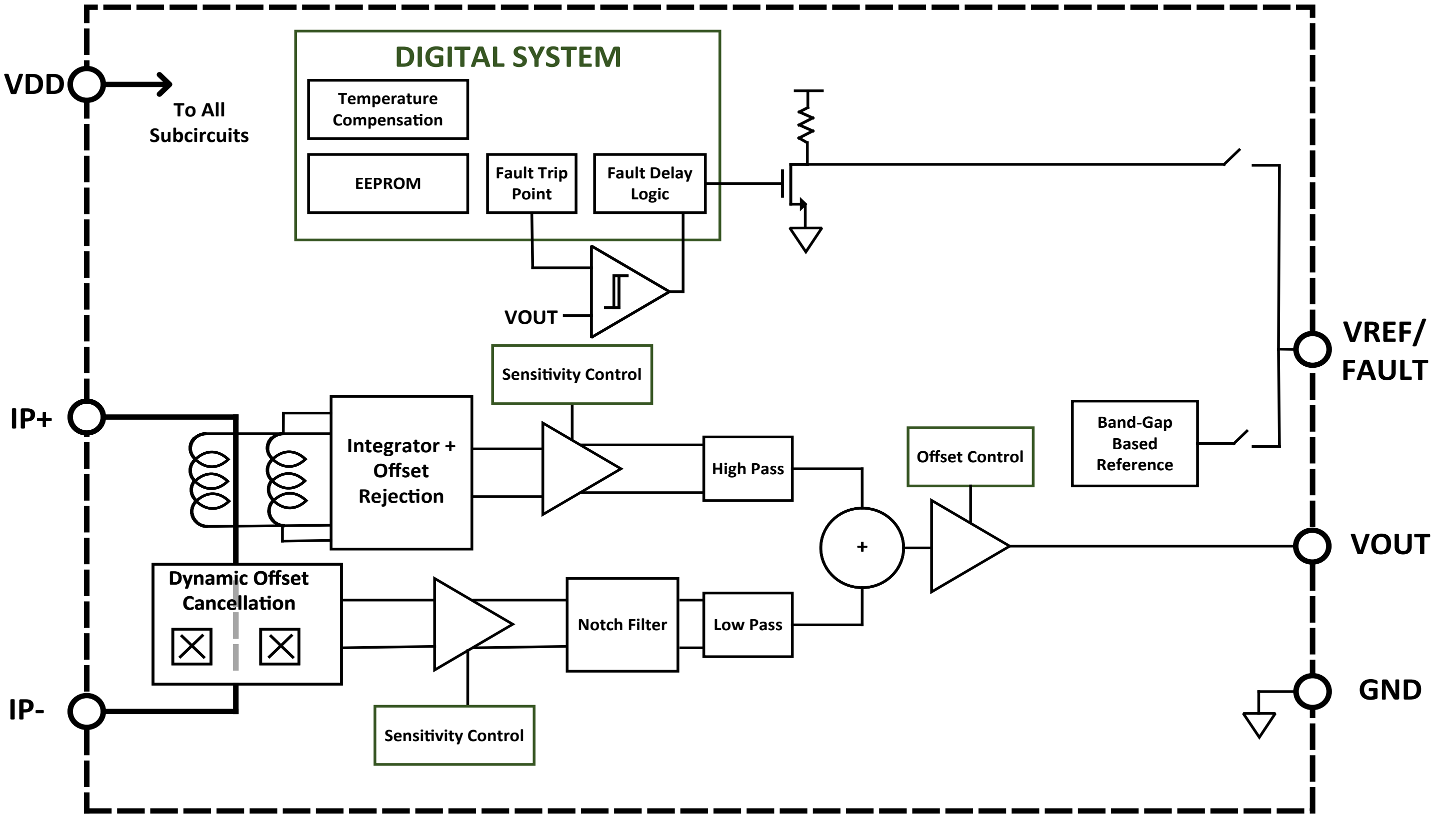

Figure 3: Functional Block Diagram

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COMMON ELECTRICAL CHARACTERISTICS: Valid through full operating temperature range, T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, and V_{DD} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}		3	3.3	3.6	V
Supply Current	I_{DD}	V_{DD} = 3.3 V, no load on V_{OUT} or V_{REF}	–	20	30	mA
Supply Bypass Capacitor	C_{BYPASS}	VDD to GND	0.1	–	–	µF
Output Resistive Load	R_{L_VOUT}	VOUT to GND, VOUT to VDD	50	–	–	kΩ
Output Capacitive Load	C_{L_VOUT}	VOUT to GND	–	–	100	pF
Power-On Reset Voltage	V_{POR}	V_{DD} rising 1 V/ms	2.6	2.9	3	V
POR Hysteresis	V_{POR_HYS}		200	250	–	mV
Power-On Time	t_{PO}		–	2	4	ms
OUTPUT SIGNAL CHARACTERISTICS (VOUT)						
Saturation Voltage	V_{SAT_H}	R_L = 50 kΩ to GND	3	–	–	V
	V_{SAT_L}	R_L = 50 kΩ to V_{DD}	–	–	0.15	V
VOUT Short Circuit Current	I_{SC_VOUT}	T_A = 25°C, shorted to GND	–	25	–	mA
		T_A = 25°C, shorted to VDD	–	–25	–	mA
Bandwidth	BW	Small signal –3 dB, C_L = 100 pF	–	5	–	MHz
Rise Time	t_R	T_A = 25°C, C_L = 100 pF	–	40	–	ns
Response Time	t_{RESP}	T_A = 25°C, C_L = 100 pF	–	40	–	ns
Propagation Delay	t_{PD}	T_A = 25°C, C_L = 100 pF	–	30	–	ns
Noise	I_N	BW = 5 MHz, T_A = 25°C, C_L = 100 pF	–	50	–	mA_{RMS}
Common-Mode Field Rejection	CMFR	Input-referred error due to a common-mode field	–	0.9	–	mA/G
REFERENCE OUTPUT CHARACTERISTICS (VREF)						
VREF Resistive Load	R_{L_VREF}	VREF to GND or VREF to VDD	50	–	–	kΩ
VREF Capacitive Load	C_{L_VREF}	VREF to GND	–	–	100	pF
Reference Source Current Limit	I_{SC_VREF}	VREF shorted to GND	–	25	–	mA
	I_{SK_VREF}	VREF shorted to VDD	–	–25	–	mA
FAULT OUTPUT CHARACTERISTICS						
Overcurrent Operating Range	I_{OCR}		90	100	110	%
Internal Overcurrent Pull-Up Resistance	R_{L_IFAULT}		–	10	–	kΩ
Overcurrent Error	E_{OC}		–10	–	10	$\%I_{OCR}$ [1]
FAULT Output Low Voltage	V_{FAULT_L}	R_{L_FAULT} = 10 kΩ, fault condition present	–	0.1	0.4	V
FAULT Leakage Current	I_{FAULT_OFF}	R_{L_FAULT} = 10 kΩ, no fault condition present	–	100	500	nA
Overcurrent Hysteresis	I_{OC_HYS}		–	6	10	$\%I_{PR}$
Overcurrent Response Time [2]	t_{OC_RESP}		–	50	–	ns
Overcurrent Release Time [2]	t_{OC_REL}		–	100	–	ns
Overcurrent Hold Time [2]	t_{OC_HLD}		–	0.1	–	ms

[1] Where I_{OCR} is the specific point at which the OCF trigger will occur.
[2] Guaranteed by design and bench validated.

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ACS37030LLZATR-020B3 PERFORMANCE CHARACTERISTICS: Valid through full operating temperature range, T_A = – 40°C to 150°C, C_{BYPASS} = 0.1 µF, and V_{DD} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–20	–	20	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	66	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	1.65	–	V
Reference Voltage Output	V_{REF}		–	1.65	–	V
ERROR COMPONENTS						
Sensitivity Error	E_{SENS}	I_P= $I_{PR(max)}$, T_A = –40°C to 150°C, DC	–2	±1	2	%
		I_P= 7 A, T_A = –40°C to 150°C, 500 kHz	–	±2	–	%
Offset Error	V_{OE}	I_P = 0 A, T_A = –40°C to 150°C	–10	±5	10	mV
Reference Voltage Output Error	V_{REF_E}	I_P = 0 A, T_A =–40°C to 150°C	–10	±5	10	mV
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = –40°C to 150°C	–10	±5	10	mV
Power Supply Offset Error	V_{OE_PS}	3.15 to 3.45 V, T_A = 25°C	–5	±3	5	mV
Power Supply Sensitivity Error	E_{SENS_PS}	3.15 to 3.45 V, T_A = 25°C	–1.5	±1	1.5	%
ERROR INCLUDING LIFETIME DRIFT [2]						
Hall Path Sensitivity Error Including Lifetime Drift	$E_{SENS\_H\_LT}$	I_P= $I_{PR(max)}$, DC	–3.5	–	3.5	%
Coil Path Sensitivity Error Including Lifetime Drift	$E_{SENS\_C\_LT}$	I_P= 7 A, AC	–3.75	–	3.75	%
Offset Error Including Lifetime Drift	V_{OE_LT}	I_P = 0 A, T_A = –40°C to 150°C	–10	–	10	mV
Reference Voltage Error Including Lifetime Drift	V_{REF_LT}	T_A = –40°C to 150°C	–10	–	10	mV
Quiescent Voltage Error Including Lifetime Drift	V_{QVO_LT}	I_P = 0 A, T_A = –40°C to 150°C	–10	–	10	mV

[1] Typical values are the mean ±3 sigma of production distributions.
[2] Lifetime drift minimum/maximum values are ±3 sigma, and are based on a statistical combination of production distributions and worst-case drift distributions observed after AEC-Q100 qualification stresses.

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Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–40	–	40	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	33	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	1.65	–	V
Reference Voltage Output	V_{REF}		–	1.65	–	V
ERROR COMPONENTS						
Sensitivity Error	E_{SENS}	I_P= $I_{PR(max)}$, T_A = –40°C to 150°C, DC	–2	±1	2	%
		I_P= 7 A, T_A = –40°C to 150°C, 500 kHz	–	±2	–	%
Offset Error	V_{OE}	I_P = 0 A, T_A = –40°C to 150°C	–10	±5	10	mV
Reference Voltage Output Error	V_{REF_E}	I_P = 0 A, T_A =–40°C to 150°C	–10	±5	10	mV
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = –40°C to 150°C	–10	±5	10	mV
Power Supply Offset Error	V_{OE_PS}	3.15 to 3.45 V, T_A = 25°C	–5	±3	5	mV
Power Supply Sensitivity Error	E_{SENS_PS}	3.15 to 3.45 V, T_A = 25°C	–1.5	±1	1.5	%
ERROR INCLUDING LIFETIME DRIFT [2]						
Hall Path Sensitivity Error Including Lifetime Drift	$E_{SENS\_H\_LT}$	I_P= $I_{PR(max)}$, DC	–3.5	–	3.5	%
Coil Path Sensitivity Error Including Lifetime Drift	$E_{SENS\_C\_LT}$	I_P= 7 A, AC	–3.75	–	3.75	%
Offset Error Including Lifetime Drift	V_{OE_LT}	I_P = 0 A, T_A = –40°C to 150°C	–10	–	10	mV
Reference Voltage Error Including Lifetime Drift	V_{REF_LT}	T_A = –40°C to 150°C	–10	–	10	mV
Quiescent Voltage Error Including Lifetime Drift	V_{QVO_LT}	I_P = 0 A, T_A = –40°C to 150°C	–10	–	10	mV

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Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–65	–	65	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	20.3	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	1.65	–	V
Reference Voltage Output	V_{REF}		–	1.65	–	V
ERROR COMPONENTS						
Sensitivity Error	E_{SENS}	I_P= 40 A, T_A = –40°C to 150°C, DC	–2	±1	2	%
		I_P= 7 A, T_A = –40°C to 150°C, 500 kHz	–	±2	–	%
Offset Error	V_{OE}	I_P = 0 A, T_A = –40°C to 150°C	–10	±5	10	mV
Reference Voltage Output Error	V_{REF_E}	I_P = 0 A, T_A =–40°C to 150°C	–10	±5	10	mV
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = –40°C to 150°C	–10	±5	10	mV
Power Supply Offset Error	V_{OE_PS}	3.15 to 3.45 V, T_A = 25°C	–5	±3	5	mV
Power Supply Sensitivity Error	E_{SENS_PS}	3.15 to 3.45 V, T_A = 25°C	–1.5	±1	1.5	%
ERROR INCLUDING LIFETIME DRIFT [2]						
Hall Path Sensitivity Error Including Lifetime Drift	$E_{SENS\_H\_LT}$	I_P= 40 A, DC	–3.5	–	3.5	%
Coil Path Sensitivity Error Including Lifetime Drift	$E_{SENS\_C\_LT}$	I_P= 7 A, AC	–3.75	–	3.75	%
Offset Error Including Lifetime Drift	V_{OE_LT}	I_P = 0 A, T_A = –40°C to 150°C	–10	–	10	mV
Reference Voltage Error Including Lifetime Drift	V_{REF_LT}	T_A = –40°C to 150°C	–10	–	10	mV
Quiescent Voltage Error Including Lifetime Drift	V_{QVO_LT}	I_P = 0 A, T_A = –40°C to 150°C	–10	–	10	mV

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Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–20	–	20	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	66	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	1.65	–	V
Overcurrent Threshold	I_{OC}		–	100	–	$\%I_{PR}$
Overcurrent Hysteresis	I_{OC_HYS}		–	1.2	–	A
FAULT ERROR						
Overcurrent Error	I_{OC_E}		–2	–	2	A
ERROR COMPONENTS						
Sensitivity Error	E_{SENS}	I_P= $I_{PR(max)}$, T_A = –40°C to 150°C, DC	–2	±1	2	%
		I_P= 7 A, T_A = –40°C to 150°C, 500 kHz	–	±2	–	%
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = –40°C to 150°C	–10	±5	10	mV
Power Supply Offset Error	V_{OE_PS}	3.15 to 3.45 V, T_A = 25°C	–5	±3	5	mV
Power Supply Sensitivity Error	E_{SENS_PS}	3.15 to 3.45 V, T_A = 25°C	–1.5	±1	1.5	%
ERROR INCLUDING LIFETIME DRIFT[2]						
Hall Path Sensitivity Error Including Lifetime Drift	$E_{SENS\_H\_LT}$	I_P= $I_{PR(max)}$, DC	–3.5	–	3.5	%
Coil Path Sensitivity Error Including Lifetime Drift	$E_{SENS\_C\_LT}$	I_P= 7 A, AC	–3.75	–	3.75	%
Quiescent Voltage Error Including Lifetime Drift	V_{QVO_LT}	I_P = 0 A, T_A = –40°C to 150°C	–10	–	10	mV

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Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–40	–	40	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	33	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	1.65	–	V
Overcurrent Threshold	I_{OC}		–	100	–	$\%I_{PR}$
Overcurrent Hysteresis	I_{OC_HYS}		–	2.4	–	A
FAULT ERROR						
Overcurrent Error	I_{OC_E}		–4	–	4	A
ERROR COMPONENTS						
Sensitivity Error	E_{SENS}	$I_P = I_{PR(max)}$, T_A = –40°C to 150°C, DC	–2	±1	2	%
		I_P= 7 A, T_A = –40°C to 150°C, 500 kHz	–	±2	–	%
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = –40°C to 150°C	–10	±5	10	mV
Power Supply Offset Error	V_{OE_PS}	3.15 to 3.45 V, T_A = 25°C	–5	±3	5	mV
Power Supply Sensitivity Error	E_{SENS_PS}	3.15 to 3.45 V, T_A = 25°C	–1.5	±1	1.5	%
ERROR INCLUDING LIFETIME DRIFT [2]						
Hall Path Sensitivity Error Including Lifetime Drift	$E_{SENS\_H\_LT}$	$I_P = I_{PR(max)}$, DC	–3.5	–	3.5	%
Coil Path Sensitivity Error Including Lifetime Drift	$E_{SENS\_C\_LT}$	I_P= 7 A, AC	–3.75	–	3.75	%
Quiescent Voltage Error Including Lifetime Drift	V_{QVO_LT}	I_P = 0 A, T_A = 25°C to 150°C	–10	–	10	mV

[1] Typical values are the mean ±3 sigma of production distributions.
[2] Lifetime drift minimum/maximum values are ±3 sigma, and are based on a statistical combination of production distributions and worst-case drift distributions observed after AEC-Q100 qualification stresses.

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Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–65	–	65	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	20.3	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	1.65	–	V
Overcurrent Threshold	I_{OC}		–	100	–	$\%I_{PR}$
Overcurrent Hysteresis	I_{OC_HYS}		–	3.9	–	A
FAULT ERROR						
Overcurrent Error	I_{OC_E}		–6.5	–	6.5	A
ERROR COMPONENTS						
Sensitivity Error	E_{SENS}	I_P= 40 A, T_A = –40°C to 150°C, DC	–2	±1	2	%
		I_P= 7 A, T_A = –40°C to 150°C, 500 kHz	–	±2	–	%
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = –40°C to 150°C	–10	±5	10	mV
Power Supply Offset Error	V_{OE_PS}	3.15 to 3.45 V, T_A = 25°C	–5	±3	5	mV
Power Supply Sensitivity Error	E_{SENS_PS}	3.15 to 3.45 V, T_A = 25°C	–1.5	±1	1.5	%
ERROR INCLUDING LIFETIME DRIFT [2]						
Hall Path Sensitivity Error Including Lifetime Drift	$E_{SENS\_H\_LT}$	I_P= 40 A, DC	–3.5	–	3.5	%
Coil Path Sensitivity Error Including Lifetime Drift	$E_{SENS\_C\_LT}$	I_P= 7 A, AC	–3.75	–	3.75	%
Quiescent Voltage Error Including Lifetime Drift	V_{QVO_LT}	I_P = 0 A, T_A = 25°C to 150°C	–10	–	10	mV

[1] Typical values are the mean ±3 sigma of production distributions.
[2] Lifetime drift minimum/maximum values are ±3 sigma, and are based on a statistical combination of production distributions and worst-case drift distributions observed after AEC-Q100 qualification stresses.

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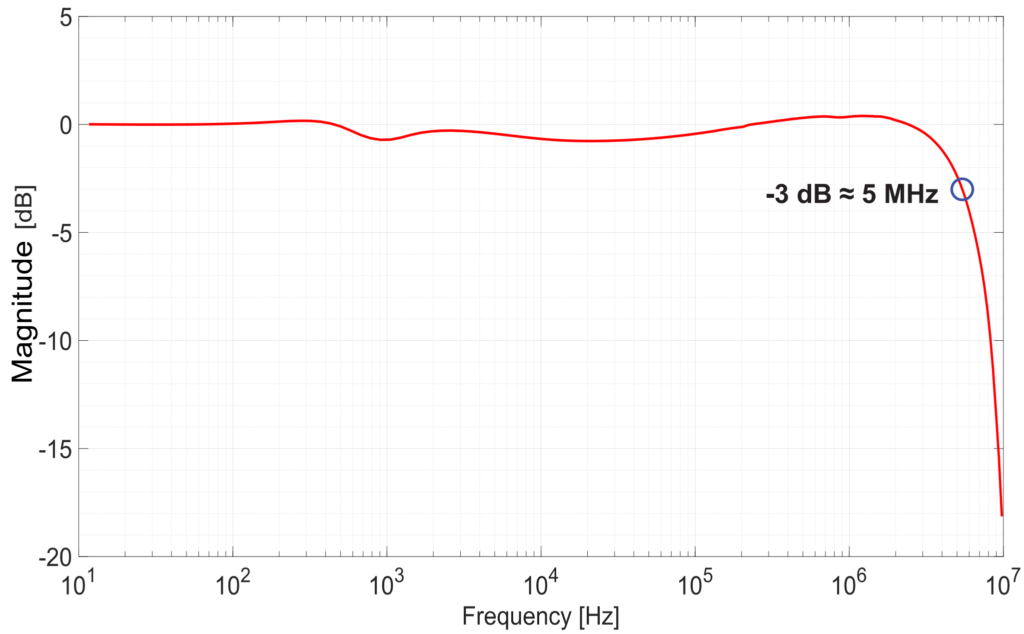
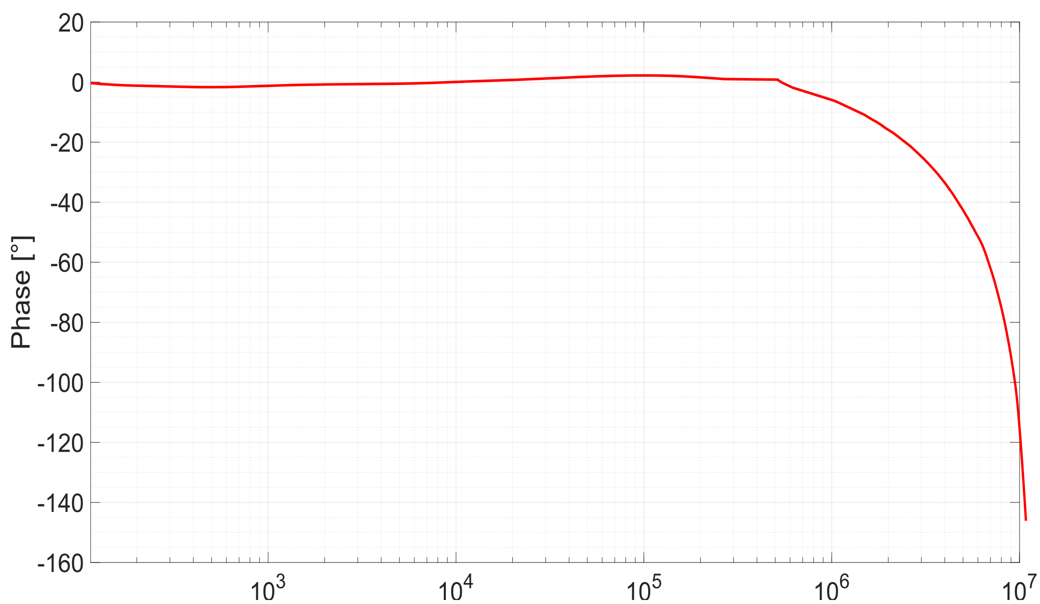
ACS37030/2 TYPICAL FREQUENCY RESPONSE





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RESPONSE CHARACTERISTICS DEFINITIONS AND PERFORMANCE DATA

Response Time (t_{RESP})

The time interval between a) when the sensed input current reaches 90% of its full-scale value, and b) when the sensor output reaches 90% of its full-scale value.

Propagation Delay (t_{PD})

The time interval between a) when the sensed input current reaches 10% of its full-scale value, and b) when the sensor output reaches 10% of its full-scale value.

Rise Time (t_R)

The time interval between a) when the sensor output reaches 10% of its full-scale value, and b) when the sensor output reaches 90% of its full-scale value.

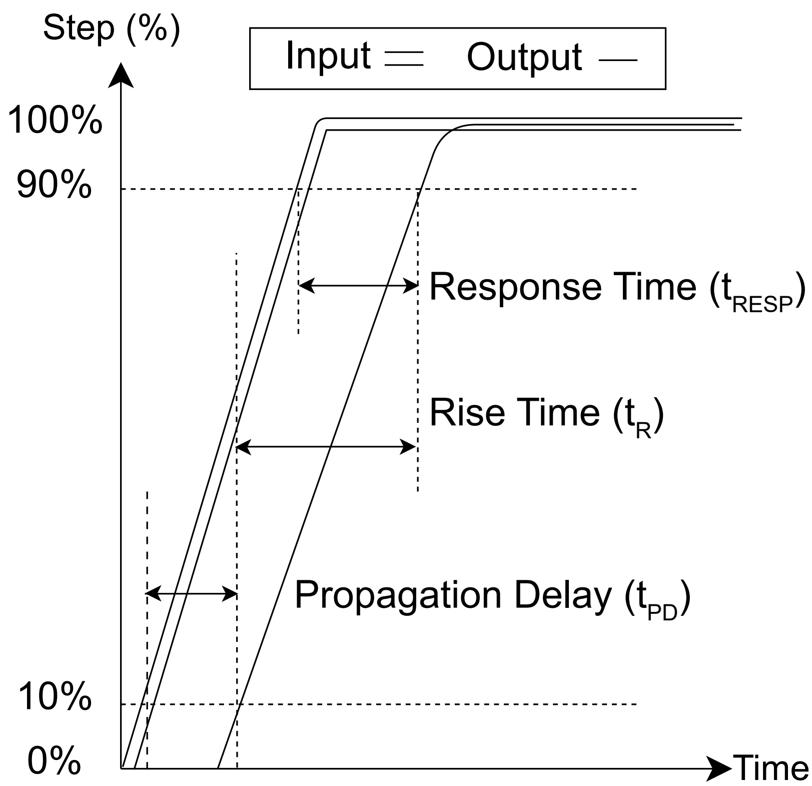

Figure 4: Step Response Characteristics

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FUNCTIONAL DESCRIPTION OF POWER ON/OFF OPERATION

Introduction

The voltage of V_{OUT} during a high-impedance state will be most consistent with a known load (R_{L_VOUT}, C_{L_VOUT}). Figure 5 and Figure 6 use the same labeling scheme for different power thresholds. References in brackets "[ ]" are valid for each of these plots.

POWER-ON OPERATION

As V_{DD} ramps up, the V_{OUT} and V_{REF} pins are high-Z until V_{DD} reaches and passes V_{POR} [1]. Once V_{DD} has passed V_{POR} [1], V_{OUT} enters normal operation.

POWER-OFF OPERATION

As V_{DD} drops below $V_{POR} - V_{POR\_HYS}$ (power-on voltage minus the hysteresis level for the power-on voltage), the outputs will enter a high-Z state. The hysteresis on the power-on voltage prevents noise on the supply line from causing the ACS37030 from entering/exiting POR around the V_{POR} level.

NOTE: Because the device is entering a high-Z state and not driving the output, the time it takes the output to reach a steady state will depend on the external circuitry used.

Voltage Thresholds

POWER-ON RESET RELEASE VOLTAGE (V_{POR})

If V_{DD} falls below $V_{POR} - V_{POR\_HYS}$ [2] while in operation, the digital circuitry turns off and the output will re-enter a high-Z state. After V_{DD} recovers and exceeds V_{POR} [1], the output will begin reporting again after the delay of t_{PO}.

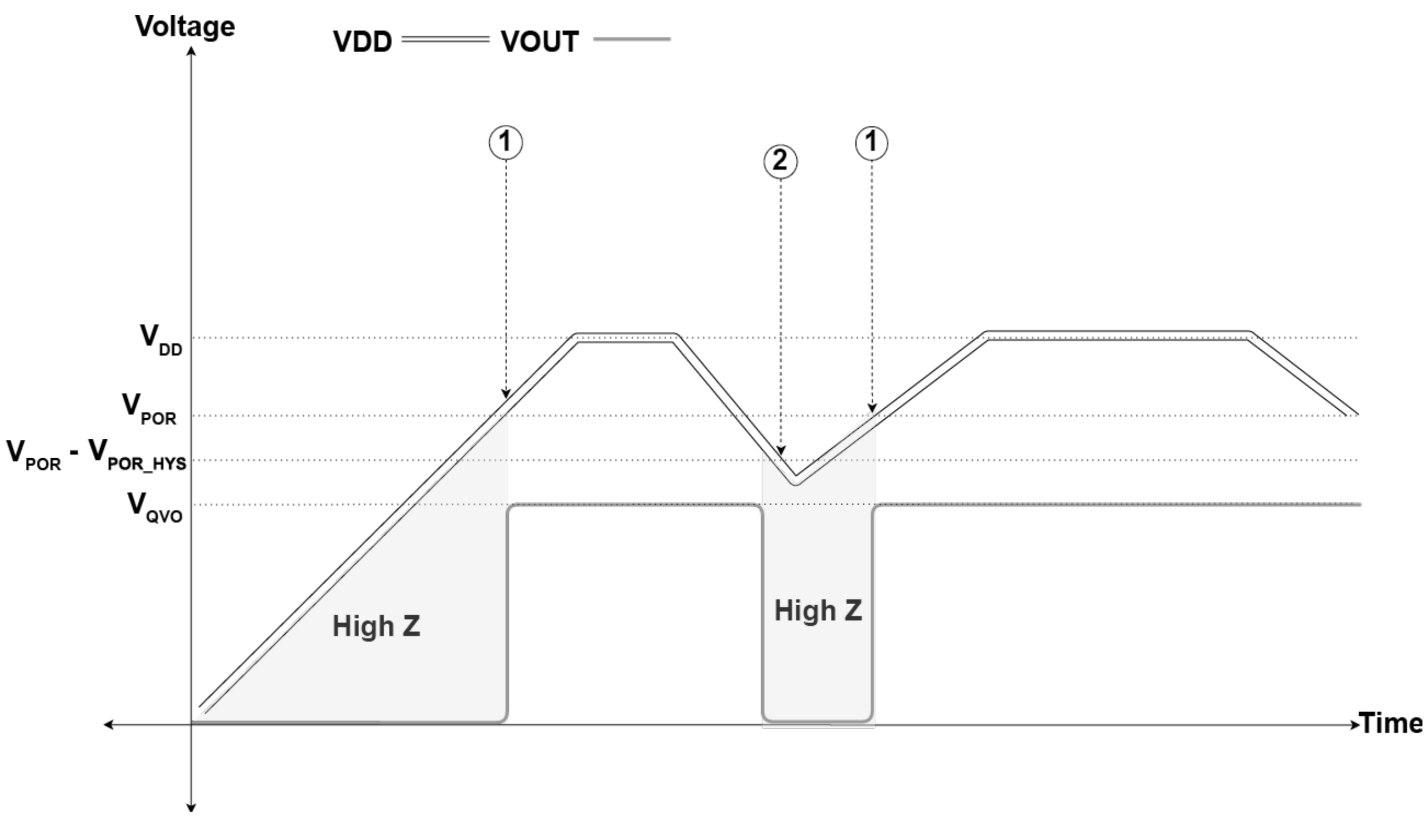

Figure 5: Power States Thresholds with V_{OUT} Behavior for a 3.3 V Device, R_L = Pull-Down

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Timing Thresholds

POWER-ON DELAY (t_{PO})

When the supply is ramped to V_{POR} [1], the device will require a finite time to power its internal components before the outputs are released from high-Z and can respond to an input magnetic field. Power-On Time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, which can be seen as the time from [1] to [A]. After this delay, the output will quickly approach $V_{OUT(IP)} = Sens \times I_P + V_{REF}$.

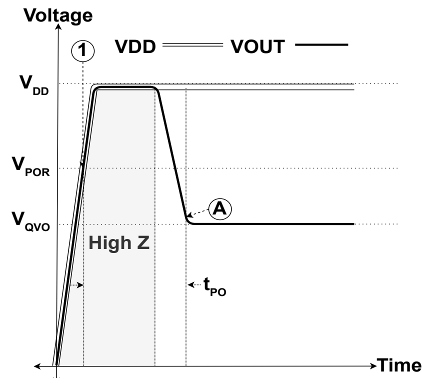

Figure 6: t_{PO} behavior, R_{L_VOUT} = Pull-Up

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DEFINITIONS OF OPERATING AND PERFORMANCE CHARACTERISTICS

Quiescent Voltage Output (V_{QVO})

Quiescent Voltage Output, or V_{QVO}, is defined as the voltage on the output, V_{OUT}, when zero amps are applied through I_P.

Quiescent Voltage Output Error(V_{QVO_E})

Quiescent Voltage Output Error, or V_{QVO_E}, is defined as the error of the VOUT voltage to the V_{QVO} target over all temperatures, with 0 A applied. To improve over temperature performance, the temperature drift is compensated with Allegro factory trim to remain within the limits across temperature.

Reference Voltage Output (V_{REF})

The Reference Voltage Output, or V_{REF}, reports the quiescent voltage output for the output channel, V_{OUT}. The internally generated V_{REF} is used in a pseudo-differential mode to remove errors due to the reference shifts or noise on the ground line. ACS37030 only.

Reference Voltage Output Error (V_{REF_E})

Reference Voltage Output Error, or V_{REF_E}, is defined as the error of the VREF output voltage to the target Reference Voltage Output, V_{REF}. ACS37030 only.

Offset Error (V_{OE})

Offset Error, or V_{OE}, is defined as the difference between V_{QVO} and V_{REF}. V_{OE} includes $V_{QVO\_E} - V_{REF}$ drift over temperature. ACS37030 only.

Output Saturation Voltage (V_{SAT_H} /V_{SAT_L})

Output Saturation Voltage, or V_{SAT}, is defined as the voltage that the V_{OUT} does not pass as a result of an increasing magnitude of current. V_{SAT_H} is the highest voltage the output can drive to, while V_{SAT_L} is the lowest. Note that changing the sensitivity does not change the V_{SAT} points.

Sensitivity (Sens)

Sensitivity, or Sens, is the ratio of the output swing versus the applied current through the primary conductor, I_P. This current causes a voltage deviation away from V_{QVO} on the V_{OUT} output until V_{SAT}. The magnitude and direction of the output voltage swing is proportional to the magnitude and direction of the applied current. This proportional relationship between output and input is Sensitivity and is defined as:

$$Sens = \frac{V_{OUT(IP_1)} - V_{OUT(IP_2)}}{IP_1 - IP_2}$$

where IP_1 and IP_2 are two different currents, and where $V_{OUT(IP1)}$ and $V_{OUT(IP2)}$ are the voltages of the device at those applied currents.

Sensitivity Error (E_{SENS})

Sensitivity Error, or E_{SENS}, is the error of Sensitivity from the sensitivity target including drift over temperature. Sensitivity error is compensated with Allegro factory trim.

Error Components Including Lifetime Drift (E_{SENS_LTD}/V_{QVO_LTD}/V_{REF_LTD}/V_{OE_LTD})

Lifetime drift characteristics are based on a statistical combination of production distributions and worst-case distribution of parametric drift of individuals observed during AEC-Q100 qualification. Solder reflow induces stress on the ACS37030/32 device causing parametric shifts, and lifetime drift limits apply immediately after solder reflow as well as long term use.

Power Supply Sensitivity Error (E_{SENS_PS})

Power Supply Sensitivity Error, or E_{SENS_PS}, is defined as the difference in E_{SENS} measurements when V_{DD} is at the nominal value and V_{DD} is ±5%. For a 3.3 V device, this is 3.15 V to 3.45 V.

Power Supply Offset Error (V_{OE_PS})

Power Supply Offset Error, or V_{OE_PS}, is defined as the difference in V_{OE} measurements when V_{DD} is at the nominal value and and V_{DD} is ±5%. For a 3.3 V device, this is 3.15 V to 3.45 V.

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OVERCURRENT FAULT (OCF) BEHAVIOR

The overcurrent fault (OCF) function (ACS37032 only) pulls the open-drain FAULT pin low when the applied current exceeds a preset threshold (I_{OCR}). On the ACS37032, this threshold is internally set to 100% of the full-scale rated current. This flag trips symmetrically for positive and negative applied currents.

The implementation for the OCF circuitry is accurate over temperature and does not require further temperature compensation.

OVERCURRENT ERROR (I_{OC_E})

Overcurrent Error, or I_{OC_E}, is the error between the ideal I_{OC} and the measured I_{OC}.

OVERCURRENT HYSTERESIS (I_{OC_HYS})

Overcurrent Hysteresis, or I_{OC_HYST}, is defined as the magnitude of current in percentage of the FS that must drop before a fault assertion will be cleared. This can be seen as the separation between the voltages [9] to [10] in Figure 7.

OVERCURRENT FAULT RESPONSE TIME (t_{OC_RESP})

Overcurrent Response Time, or t_{OC_RESP}, is defined as the time from when the input reaches the operating point [9] until the OCF pin falls below V_{FAULT_L} [G].

OVERCURRENT FAULT HOLD TIME (t_{OC_HLD})

Overcurrent Hold Time, or t_{OC_HLD}, is defined as the minimum time the OCF flag will be asserted after an OCF event. After the hold time has been reached, the OCF will release if the OCF condition has ended ([G] until [J] in Figure 8) or persist if the OCF condition is still present. Factory default is 0.1 ms.

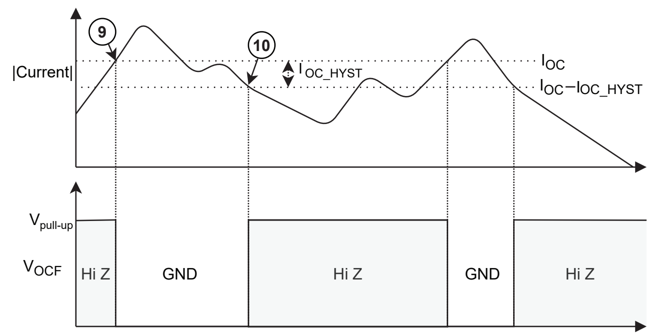

Figure 7: Fault Thresholds and OCF Pin Functionality

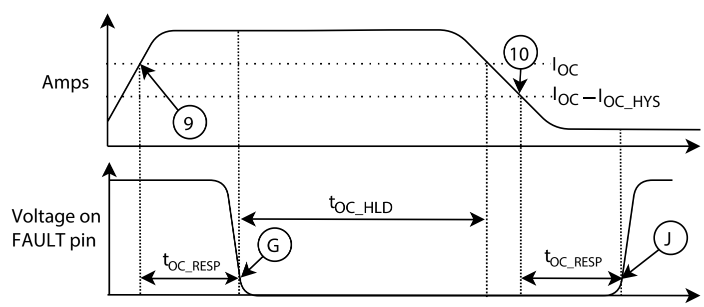

Figure 8: Fault Hold with Clear Fault After Hold Time

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THERMAL PERFORMANCE

Thermal Rise vs. Primary Current

Self-heating due to the flow of current in the package IP conductor should be considered during the design of any current sensing system. The sensor, printed circuit board (PCB), and contacts to the PCB will generate heat and act as a heat sink as current moves through the system.

The thermal response is highly dependent on PCB layout, copper thickness, cooling techniques, and the profile of the injected current. The current profile includes peak current value, current "on-time", and duty cycle.

Placing vias under the copper pads of the Allegro current sensor evaluation board minimizes the current path resistance and improves heatsinking to the PCB, while vias outside of the pads limit the current path to the top of the PCB trace and have worse heatsinking under the part (see Figure 9 and Figure 10).

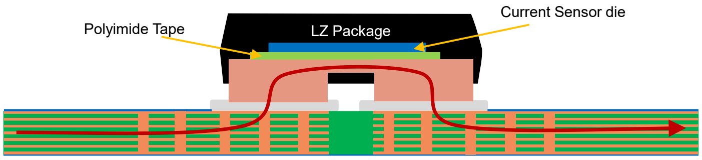

Figure 9: Vias Under Copper Pads, LZ Package

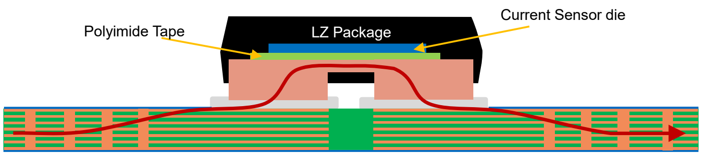

Figure 10: No Vias Under Copper Pads, LZ Package

The plot in Figure 11 shows the measured rise in steady-state die temperature of the LZ package versus DC continuous current at an ambient temperature, T_A, of 25°C for two board designs: filled vias under copper pads and no vias under copper pads (vias outside pad). Note the thermal offset curves may be directly applied to other values of T_A. Using in-pad vias has better thermal performance than no in-pad vias.

The plot in Figure 12 shows the measured rise in steady-state die temperature of the LZ package versus DC continuous current at an ambient temperature of 25°C and an ambient temperature of 125°C. The evaluation boards used have filled vias under the copper pads.

The thermal capacity of the ACS37030-32 in the LZ package should be verified by the end user in the application-specific conditions. The maximum junction temperature, $T_{J(max)}$ (165°C), should not be exceeded. Measuring the temperature of the top of the package is a close approximation of the die temperature.

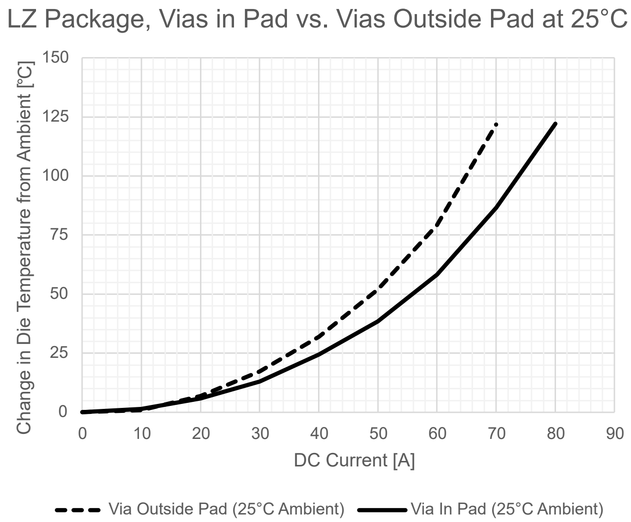

Figure 11: LZ Package Comparison with and without In-Pad Vias at Ambient Temp

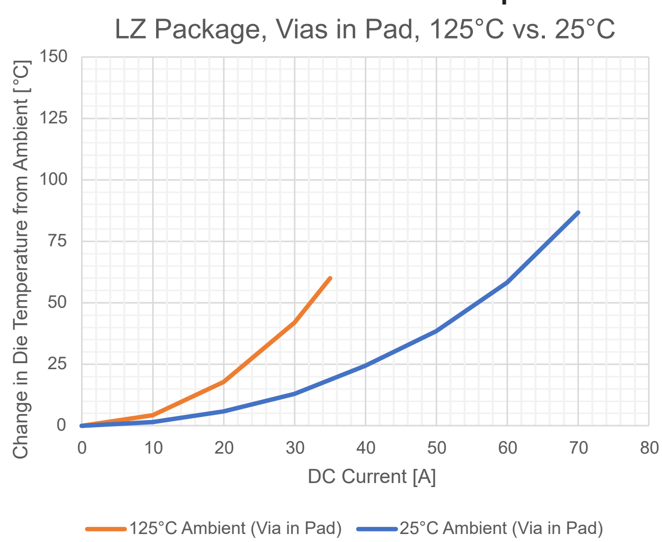

Figure 12: LZ Package Comparison at 125°C and 25°C, Vias in-Pad

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Safe Operating Region

Current applied to the IP pins of the ASC37030-32 in the LZ package will heat the package, as illustrated above. The amount of heating will depend on the current applied and duration. Figure 13 shows the range of applied current and duration of current which will not cause any detrimental effects on the part.

If enough energy is applied, the copper IP lead will melt and fuse open. This is shown by the blue line, Time to Fuse.

The maximum junction temperature is 165°C, above which the PN junctions on the die could be damaged if the maximum junction temperature is exceeded for extended periods of time. This could result in changes in the product performance or create long-term reliability risks. The region in which this occurs is shown by the green line, Time to 165°C.

The LZ package has a polyimide insulation barrier to enable high working voltages. Extended heating of the polyimide film will cause deterioration of the material, reducing the insulation effectiveness of the package. This is shown by the red line, Time to Insulation Degradation.

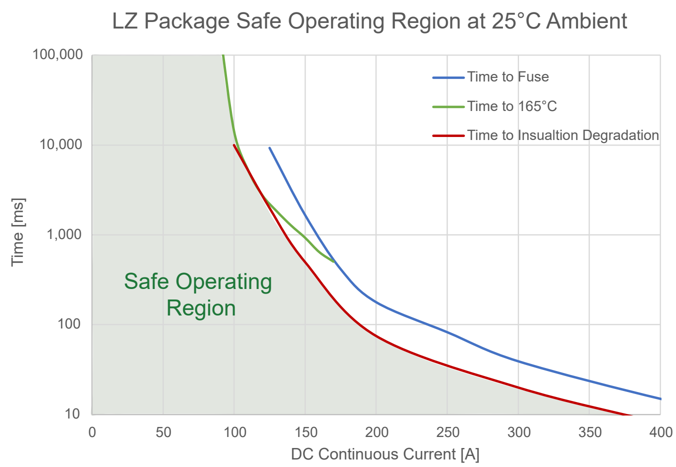


Figure 13: LZ Package Safe Operating Region

Evaluation Board Layout

Thermal data shown in Figure # was collected using the LC/LZ Current Sensor Evaluation Board (ACSEVB-LC8-LZ6, TED-0004110). This board includes six layers and the evaluation board is shown in Figure 14.

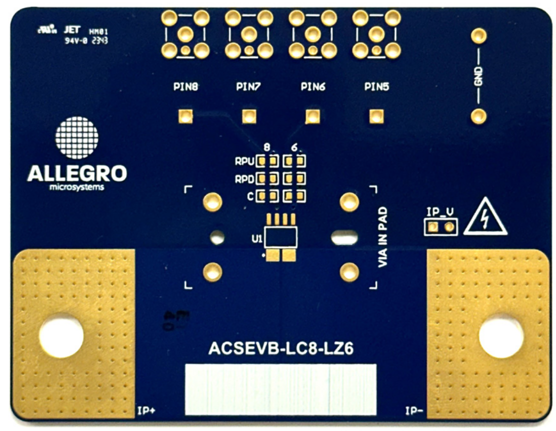


Figure 14: LZ Package Allegro Evaluation Board

Design support files for the ACSEVB-LC8-LZ6 evaluation board are available for download from the Allegro website. See the technical documents section of the ACS37030-32 webpage for more information.

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use
(Reference DWG-0000385, Rev. 1)
PRELIMINARY
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

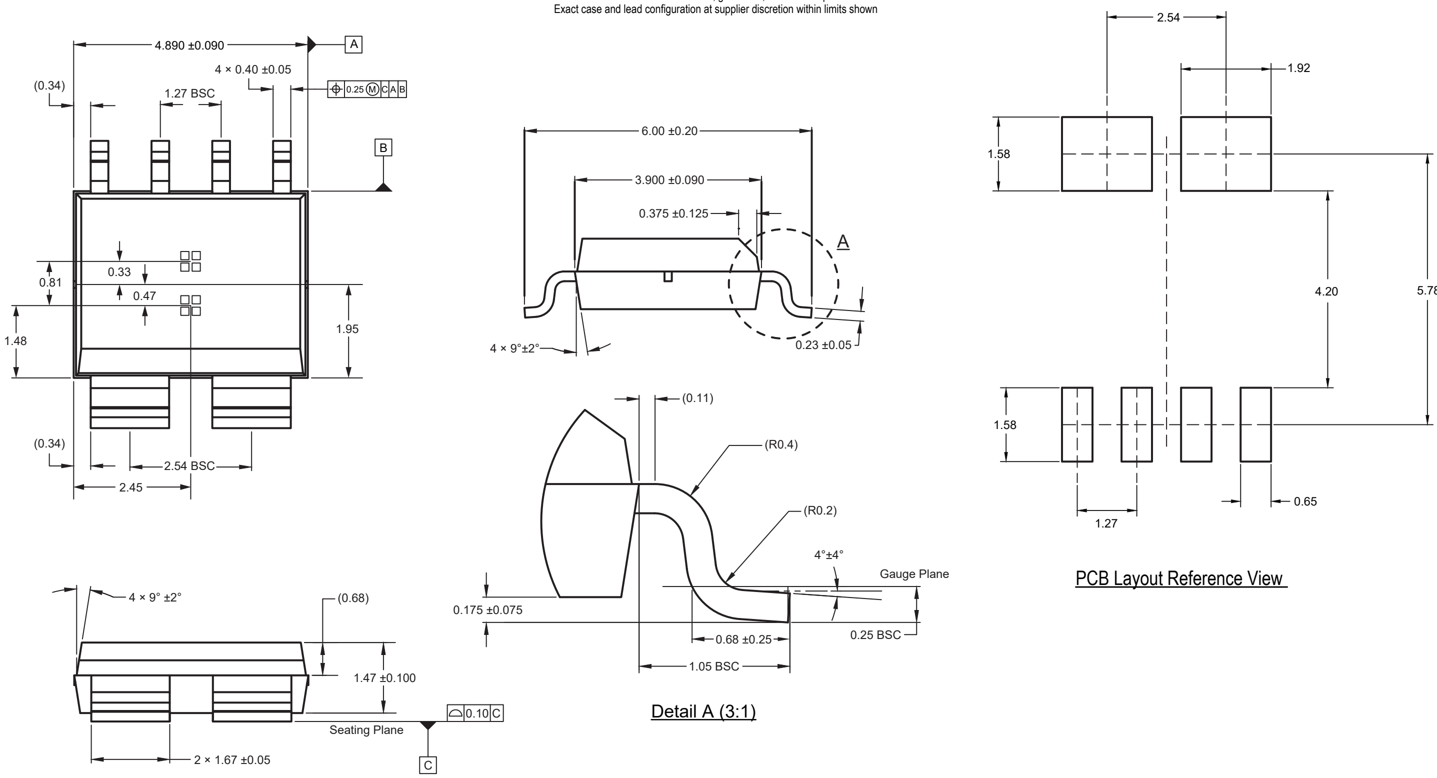
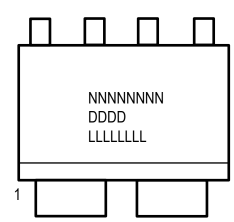


Figure 15: Custom 6-Pin SOIC (Suffix LZ)



Standard Branding Reference View
N = Device Part Number
D = Date Code
L = Assembly Lot Number

Figure 16: LZ Package Branding

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Revision History

Number	Date	Description
–	November 29, 2023	Initial release
1	January 18, 2024	Added UL Number (page 1); removed "certification pending" footnote from Isolation Characteristics table (page 3); updated Sensitivity Error and Coil Path Sensitivity Error test conditions (pages 6-11); updated Thermal Performance section (pages 18-19)
2	June 12, 2024	Added output resistive load characteristic (page 5)

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