APM80905-1

36 V, 4 A, Low-EMI, Synchronous Buck LED Driver Module with PWM Monitor

FEATURES AND BENEFITS

- Automotive ASIL B, AEC-Q100 Grade 1 qualified solution for infrared LED driver monitoring system (DMS)
- Ultra-low electromagnetic interference (EMI) architecture with integrated EMI-mitigation capacitors and spread-spectrum operation to comply with automotive requirements
- Safety protection against out-of-range PWM on-time and duty cycle with PWM monitoring feature for eye-safe operation capability
- High-integration architecture including high-side and low-side MOSFET switches and 5 V peripheral low-voltage dropout (LDO) to reduce solution size and cost
- Safety diagnostics for ASIL B compliance including:
  - Low-power shutdown (1 µA typical)
  - High-side output current sense
  - High-side MOSFET current-limit protection
  - Active-low fault flag output
  - Undervoltage lockout (UVLO)
  - Thermal shutdown protection
- Robust protection against:
  - Adjacent pin-to-pin short
  - Pin-to-ground short
  - Component open/short faults

APPLICATIONS

- Driver monitoring systems
- Advanced driver-assistance systems
- Instrument clusters

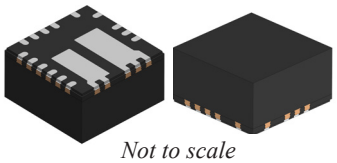
DESCRIPTION

The APM80905 is a 36 V, 4 A, ASIL B, low-EMI, synchronous buck switching regulator module that provides a regulated current output to drive high-power infrared or standard LEDs. The module integrates both the high-side and low-side N-channel MOSFET switches, high-frequency input voltage and boot capacitors. The APM80905 also includes several fault-protection features including a PWM dimming signal monitor with configurable LED on-time and duty cycle limits to simplify the design of driver monitoring systems.

The switching frequency is programmable from 400 kHz to 2.2 MHz with an external resistor. Output current is programmable by an external current sense resistor, and the output voltage is automatically adjusted to drive one or multiple LEDs in series, optimizing system efficiency regardless of the number of LEDs in the string. The analog dimming input, ADIM, allows for LED current calibration or thermal foldback with an external negative temperature coefficient (NTC) thermistor. An open-drain fault flag pin, FFn, is pulled low to alert the system or controller that a fault was detected.

The APM80905 is offered in a compact, thermally enhanced 4 mm × 4 mm × 2.1 mm quad-flat no-lead (QFN) package with wettable flank.

PACKAGE



Not to scale

24-pin QFN
4 mm × 4 mm × 2.1 mm
with wettable flank
(suffix NB)

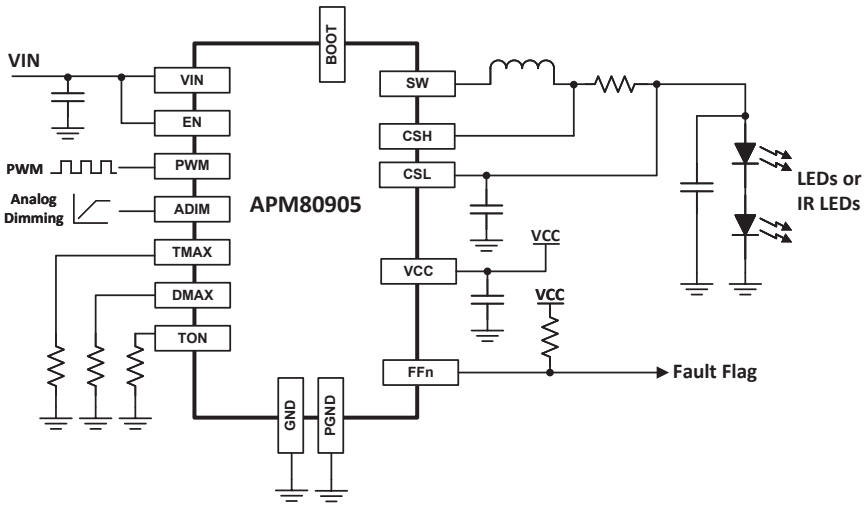


Figure 1: APM80905 Typical Application Circuit

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SELECTION GUIDE

Part Number	Dither	Description	Packing [1]	Lead Finish
APM80905KNBATR-1	Enabled	24-pin wettable flank QFN package with thermal pad	3000 pieces per 13-inch reel	Matte Tin

[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{IN}		–0.3 to 42	V
Switch Pin Voltage	V_{SW}		–0.3 to V_{IN} + 0.3	V
		Transient < 100 ns	–1.5 to V_{IN} + 0.3	V
EN, PWM Pin [2] Voltages	V_{EN}		−0.3 to V_{IN} + 0.3	V
Current Sense Voltages	V_{CSH}, V_{CSL}		−0.3 to V_{IN} + 0.3	V
BOOT Pin Voltage	V_{BOOT}	Continuous	V_{SW} – 0.3 to V_{SW} + 5.5	V
		t < 1 ms	V_{SW} – 0.3 to V_{SW} + 7	V
All other pins			–0.3 to 7	V
Operating Junction Temperature	$T_{J(max)}$		–40 to 150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] PWM pin is high-voltage-rated only for failure modes and effects analysis (FMEA) purposes. The user is expected to use it as a logic-level pin only. If the PWM pin is used for high voltage, the IC is not pin-to-pin short-protected for the PWM and DMAX pins, so a user-compromise must be made for the DMAX pin protection. The only recommended use of the PWM pin is as a logic-level pin.

THERMAL CHARACTERISTICS [1]

Characteristic	Symbol	Test Conditions	Value	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	43	°C/W

[1] Additional thermal information available on the Allegro website.

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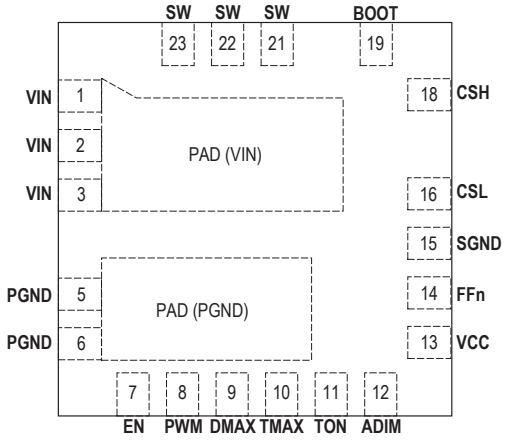
PINOUT DIAGRAM AND TERMINAL LIST

QFN-24 Pinout Diagram



Terminal List

Number	Name	Function
1, 2, 3	VIN	Power input for control circuits and power stage. Connect a ceramic capacitor between VIN and PGND close to this pin.
5, 6	PGND	Power ground pins.
7	EN	Enable pin. Pull this pin high to enable the APM80905.
8	PWM	Logic input for PWM dimming. The LEDs are on while this pin is high, EN is high, and no faults are detected.
9	DMAX	Programming pin for maximum safe output current duty cycle. Connect a resistor between DMAX and GND to set the maximum LED current duty cycle.
10	TMAX	Programming pin for maximum safe output current on-time. Connect a resistor between TMAX and GND to set the maximum LED current on-time.
11	TON	Programming pin for DC-DC converter high-side power switch on-time. Connect a resistor between TON and GND to set the high-side power switch on-time of the buck converter.
12	ADIM	Analog dimming control voltage input.
13	VCC	Internal bias regulator output. Connect a 1 µF to 4.7 µF ceramic capacitor from VCC to PGND close to this pin.
14	FFn	Open-drain, active-low fault signal. Pulled low when a fault is detected. Connect a pull-up resistor to desired logic level.
15	SGND	Signal ground pin.
16	CSL	LED current sense low pin. A resistor placed between CSH and CSL sets the current in the LED string. Place a 0.1 µF ceramic capacitor very close to the CSL pin.
18	CSH	LED current sense high pin. A resistor placed between CSH and CSL sets the current in the LED string.
19	BOOT	High-side gate driver bootstrap pin. The boot circuit capacitor is inside the package. This pin is provided for testing purposes and should be left floating.
21, 22, 23	SW	Buck converter power switch output pins. Connect these pins to the power inductor.
PAD1	Exposed Pad	PAD1 is an exposed pad and should be soldered to VIN.
PAD2	Exposed Pad	PAD2 is an exposed pad and should be soldered to the PGND plane for enhanced thermal performance.

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FUNCTIONAL BLOCK DIAGRAM

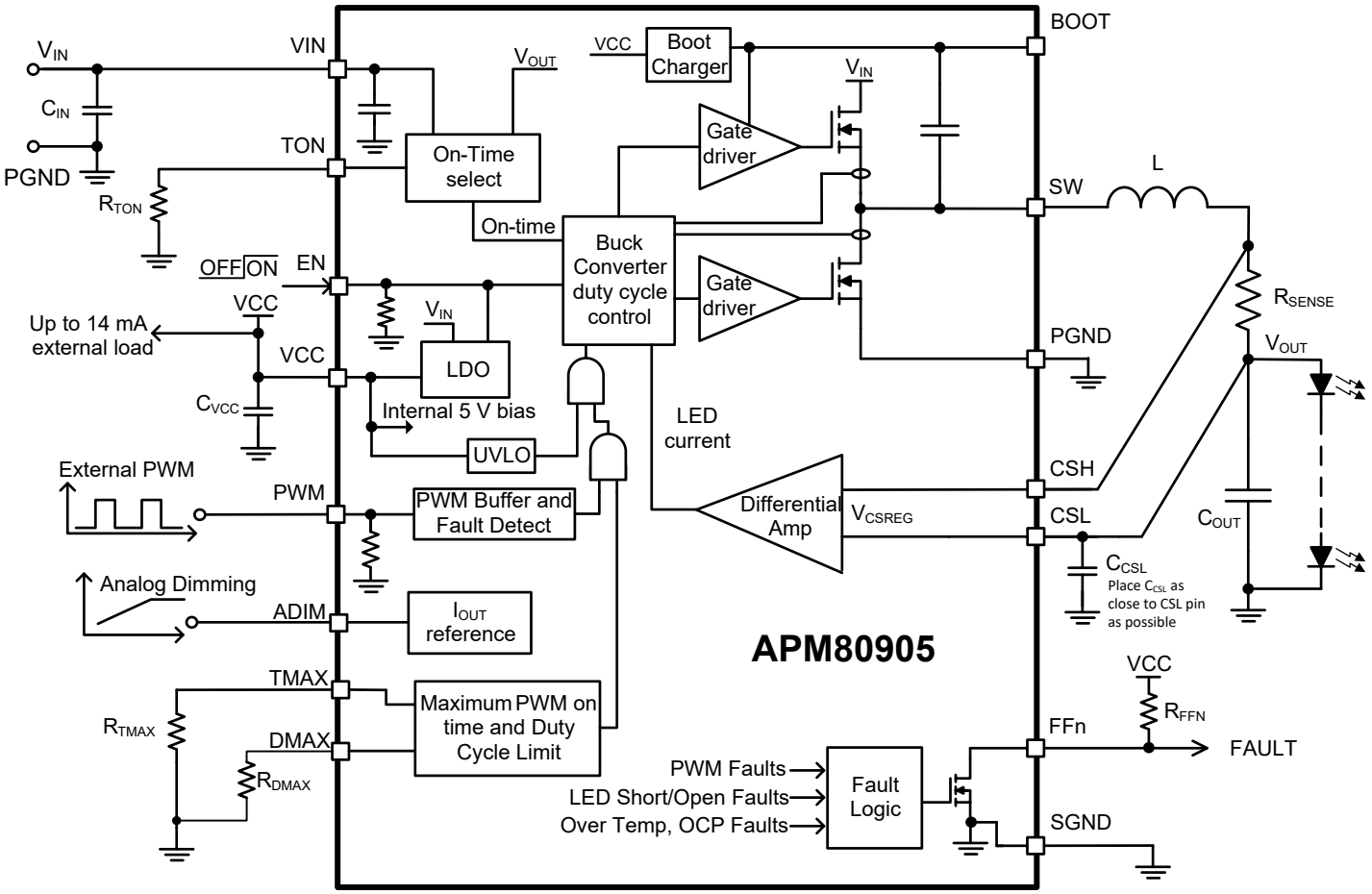

Figure 2: Functional Block Diagram

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ELECTRICAL CHARACTERISTICS: Valid at V_{IN} ≤ 12 V, V_{OUT} = 6 V, typical values at T_J = 25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
INPUT SUPPLY						
Input Voltage Range	V_{IN}	V_{IN} must first rise above $V_{UVLO(ON,MAX)}$	4.5	–	36	V
Input Supply Undervoltage Lockout Startup Threshold	$V_{UVLO(ON)}$	V_{IN} rising	–	–	4.31	V
Input Supply Undervoltage Lockout Hysteresis	$V_{UVLO(HYS)}$		–	165	–	mV
Input Supply Current [1]	I_{IN}	V_{EN} = $V_{EN(HI)}$, V_{PWM} = $V_{IL(PWM)}$	–	5	–	mA
Input Shutdown Current [1]	$I_{IN(SD)}$	V_{EN} = 0 V	–	1	10	µA
POWER SWITCHES						
Buck Switch Current Limit Threshold	$I_{SW(LIM)}$		6	6.4	7	A
Buck High-Side Switch On-Resistance	$R_{DSON(HS)}$	V_{BOOT} = V_{IN} + 4.3 V, T_J = 25°C, I_{SW} = 0.5 A	–	90	–	mΩ
Buck Low-Side Switch On-Resistance	$R_{DSON(LS)}$	V_{BOOT} = 4.3 V, T_J = 25°C, I_{SW} = 0.5 A	–	60	–	mΩ
Selected On-Time	t_{ON}	V_{IN} = 12 V, V_{CSL} = 6 V, R_{TON} = 100 kΩ	1.37	1.50	1.62	µs
Switching Minimum On-Time	$t_{ON(MIN)}$		–	108	130	ns
Switching Minimum Off-Time	$t_{OFF(MIN)}$	V_{CSH} – V_{CSL} = 0 V	–	70	90	ns
On-Time Spread Spectrum Range	$t_{ON(SWEEP)}$		–	±5	–	%
On-Time Spread Spectrum Modulation Frequency	$f_{SW(MOD)}$		–	10	–	kHz
REGULATION COMPARATOR AND ERROR AMPLIFIER						
Output Current Sense Common Mode Voltage [2]	V_{OUT}	V_{IN} = 36 V, f_{SW} = 500 kHz, I_{LED} = 0.5 A, measured at CSL pin	2.65	–	32	V
Differential Output Current Sense Voltage [3]	V_{CSREG}	V_{CSH} – V_{CSL} average, ADIM tied to VCC (no analog dimming)	189	195	201	mV
CSH Input Sense Current [1]	I_{CSH}	V_{CSH} – V_{CSL} = 0.195 V	–	230	–	µA
CSL Input Sense Current [1]	I_{CSL}	V_{CSH} – V_{CSL} = 0.195 V	–	165	–	µA
ANALOG DIMMING INPUT						
ADIM Voltage for 100% LED Current	VADIM(H)	V_{CSH} – V_{CSL} = V_{CSREG}	1.75	–	–	V
Regulation Threshold at 50% Analog Dimming	$V_{CSREG(50)}$	V_{ADIM} = 0.925 V	97	100	103	mV
Regulation Threshold at 20% Analog Dimming	$V_{CSREG(20)}$	V_{ADIM} = 0.620 V	–	40	–	mV
INTERNAL LINEAR REGULATOR						
VCC Pin Output Voltage	V_{CC}	0 mA < I_{VCC} < 14 mA, V_{IN} > 6 V	4.85	5.0	5.15	V
VCC Dropout Voltage	$V_{CC(DROP)}$	Measure V_{IN} – V_{CC}: V_{IN} = 4.8 V, I_{VCC} = 14 mA	–	0.35	0.75	V
VCC External Load	$I_{VCC(EXT)}$	V_{IN} > 6 V	–	–	14	mA
VCC Undervoltage Lockout Rising	$V_{CC(UVLO)}$		3.60	3.9	4.15	V
VCC Undervoltage Lockout Hysteresis	$V_{CC(UVLO,HYS)}$		180	230	280	mV

Continued on the next page…

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ELECTRICAL CHARACTERISTICS (continued): Valid at V_{IN} ≤ 12 V, V_{OUT} = 6 V, typical values at T_J = 25°C, unless otherwise noted

PWM INPUT						
PWM High Voltage	$V_{IH(PWM)}$	V_{PWM} increasing	–	–	1.2	V
PWM Low Voltage	$V_{IL(PWM)}$	V_{PWM} decreasing	0.6	–	–	V
PWM Pin Pull-Down Resistance	$R_{PWM(PD)}$	V_{CC} = 5 V, V_{PWM} = 3 V	–	100	–	kΩ
ENABLE INPUT						
EN High Voltage	$V_{EN(HI)}$	V_{EN} rising	1.14	1.2	1.26	V
EN Input Hysteresis	$V_{EN(HYS)}$	EN/UVHI EN/UVLO	38	104	170	mV
EN Pin Sink Current [1]	I_{EN}	V_{EN} = 1.2 V	–	1	5	µA
EN Pin Pull-Down Resistance [2]	$R_{EN(PD)}$	V_{IN} > 3 V	–	2	–	MΩ
FAULT						
Minimum V_{ADIM} for LED Open/Short Fault Detection		V_{ADIM} rising	475	500	525	mV
V_{OUT} Low Threshold for LED Short Fault Detection		V_{OUT} falling	1.5	1.7	1.9	V
Sense Voltage Threshold for LED Open Fault	$V_{CS(OPEN)}$	V_{CSREG} = 200 mV start falling (PWM duty = max), V_{ADIM} = V_{CC}	35	65	95	mV
Sense Voltage Hysteresis for LED Open Fault [2]	$V_{CS(OPEN,HYS)}$	V_{CSREG} = 200 mV start falling (PWM duty = max), V_{ADIM} = V_{CC}	–	20	–	mV
Fault Deglitch Timer	t_{FDG}		45	60	75	µs
Fault Mask Timer	t_{MASK}		90	120	150	µs
FFn Pull-Down Voltage	$V_{FAULT(PD)}$	Fault condition asserted, pull-up current = 1 mA	–	–	0.4	V
FFn Pin Leakage Current [1]	$I_{FAULT(LKG)}$	Fault condition cleared, pull-up to 5 V	–	–	1	µA
FFn Rising Delay Timer [2]	t_{RISE}	Low-to-high transition time for FFn pin			10	µs
FFn Falling Delay Timer [2]	t_{FALL}	High-to-low transition time for FFn pin			10	µs
Cool-Down Timer for Fault Retry	t_{RETRY}		–	1	–	ms
THERMAL SHUTDOWN						
Thermal Shutdown Threshold [2]	T_{SD}		150	165	180	°C
Thermal Shutdown Hysteresis [2]	T_{SDHYS}		–	25	–	°C
PWM MONITORING						
Minimum PWM On-Time Safety Limit Setting	$t_{PWMON(MIN)}$	R_{TMAX} = 6.65 kΩ	0.218	0.250	0.282	ms
Maximum PWM On-Time Safety Limit Setting	$t_{PWMON(MAX)}$	R_{TMAX} = 191 kΩ	4.37	5.00	5.63	ms
Minimum PWM Off-Time Safety Limit Setting	$t_{BLANK(MIN)}$	R_{DMAX} = 5.36 kΩ	0.71	0.82	0.93	ms
Maximum PWM Off-Time Safety Limit Setting	$t_{BLANK(MAX)}$	R_{DMAX} = 178 kΩ	16.6	19	21.4	ms

[1] Negative current is defined as coming out of (sourcing from) the specified device pin or node.
[2] Determined by design and characterization. Not production tested
[3] In test mode, a ramp signal is applied between the CSH and CSL pins to determine the V_{CSH} – V_{CSL} regulation threshold voltage. In actual application, the average V_{CSH} – V_{CSL} voltage is regulated at V_{CSREG} regardless of ripple voltage.

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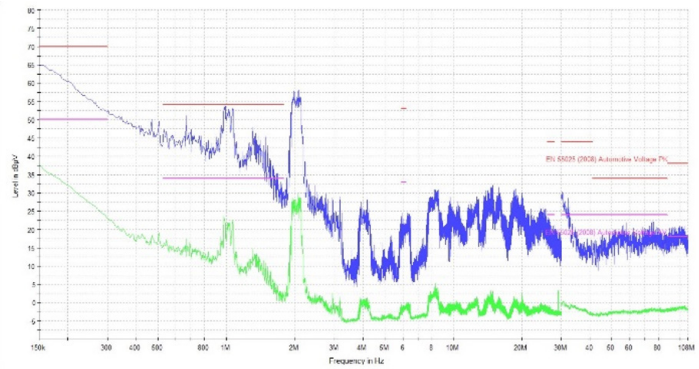
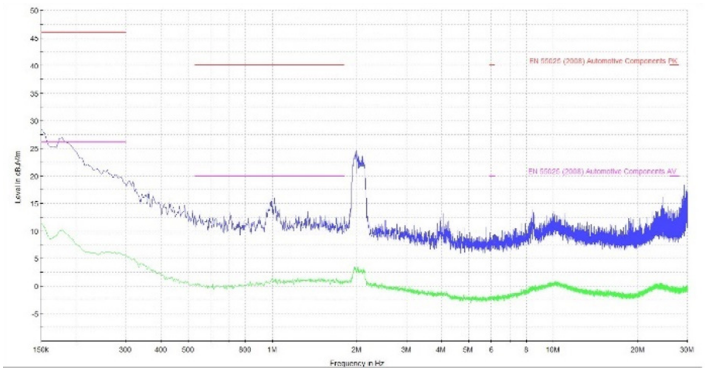
EMI/EMC PERFORMANCE CHARACTERISTICS

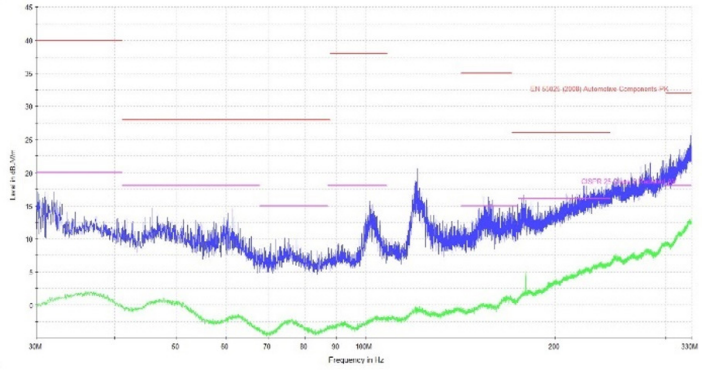
V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 2.15 MHz



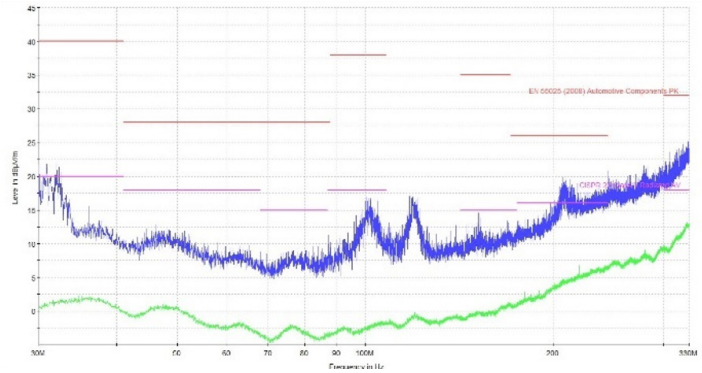
Conducted Emissions (150 kHz to 30 MHz)



Radiated Emissions (150 kHz to 30 MHz) (Monopole)



**Radiated Emissions (30 MHz to 330 MHz)
(Horizontal Biconical)**



**Radiated Emissions (30 MHz to 330 MHz)
(Vertical Biconical)**

NOTE: Allegro is not an accredited electromagnetic compatibility (EMC) laboratory. The information presented here is for reference only: APM80905 is operating at a switching frequency of 2.2 MHz for all tests with combined nominal input capacitance of 47 µF using ceramic surface mount capacitors.

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FUNCTIONAL DESCRIPTION

Overview

The APM80905 is a synchronous buck regulator module designed for driving a high-current LED or IR LED string. It employs average current-mode control to maintain constant LED current and consistent brightness.

LED Current

The LED current level is easily programmable by selection of an external current sense resistor with a value determined by:

Equation 1:

$$R_{SENSE} = \frac{V_{CSREG}}{I_{LED}}$$

where $V_{CSREG} = V_{CSH} - V_{CSL} = 195$ mV typical.

Switching Frequency

The APM80905 operates in fixed adaptive on-time mode. The on-time is programmed using an external resistor connected between the TON pin and ground. The switching frequency is dependent on several application-specific factors including input voltage, output voltage, and output current. Figure 3 shows the relationship between R_{TON} and switching frequency for a typical application with two different output currents. Since most applications are designed to target a switching frequency, such as above or below the AM radio band in automotive applications, Equation 2 can be used to approximate the value of the R_{TON} resistor value for a given switching frequency. Use Figure 4 and Figure 5 to find the constant *k* for applications with a similar input to output voltage ratio. For other applications or for more help selecting R_{TON}, consult the APM80905 Design Tool on the product web page. If switching frequency is critical to the application, the APM80905 application should be validated across all system parameters because the switching frequency varies with the system state due to the constant on-time control architecture.

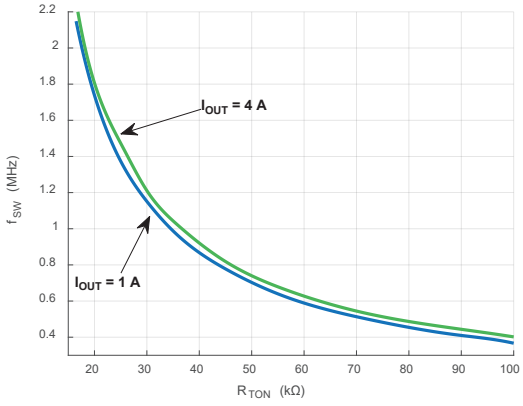

Figure 3: Switching Frequency vs. R_{TON}

Equation 2:

$$R_{TON} = \frac{1}{k \times f_{SW}}$$

Equation 3:

$$t_{ON} = k \times R_{TON} \times \frac{V_{OUT}}{V_{IN}}$$

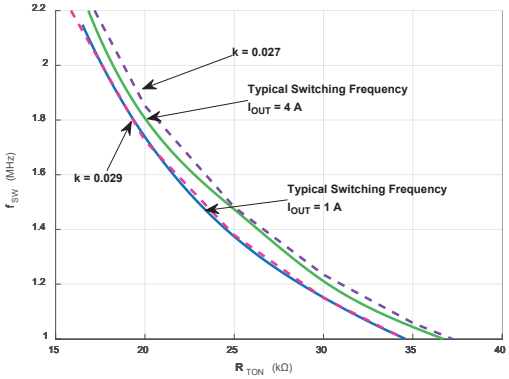

Figure 4: Switching Frequency vs. R_{TON} for f_{SW} > 1 MHz, V_{IN} = 12 V, V_{OUT} ≈ 6 V

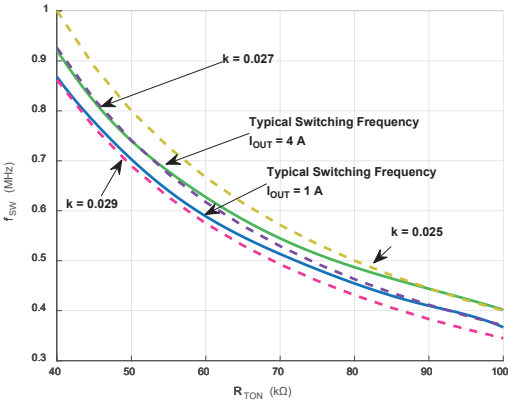

Figure 5: Switching Frequency vs. R_{TON} for f_{SW} < 1 MHz, V_{IN} = 12 V, V_{OUT} ≈ 6 V

Frequency Dithering

The APM80905 uses spread-spectrum clocking to minimize EMI at the fundamental switching frequency and its harmonics, generated by the switch node. The frequency-dithering range is fixed at ±5% with a modulation frequency of 10 kHz. The switching-frequency dither is a triangle wave, sweeping linearly between 0.95 × t_{ON} and 1.05 × t_{ON}, where t_{ON} is the programmed on-time.

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Enable

A voltage on EN that exceeds the nominal 1.2 V threshold enables the APM80905. The EN comparator has a typical hysteresis of 100 mV. Once enabled, if EN decreases to less than the 1.1 V (typ) disable threshold, the APM80905 enters the shutdown state, stops switching, and draws only 1 µA (typ) from V_{IN}.

The EN pin is high-voltage tolerant and can be directly connected to VIN for always-on applications. However, if EN exceeds the VIN voltage at any time, a series 10 kΩ resistor is required to limit the current flowing into the EN pin. The series EN pin resistor is not necessary if EN is driven from a logic input.

There is an internal 2 MΩ (typ) pull-down on the EN pin that is active once the voltage on the VIN pin is greater than approximately 3 V, preventing a leakage current path to GND through the APM80905 if the VIN supply is disabled but the EN pin is still driven high from a different supply.

Internal VCC Regulator

The VCC regulator is used as the power supply for the internal control circuitry and can supply up to 14 mA to an external load. A 1 µF to 4.7 µF ceramic capacitor placed close to the VCC pin, with a low-impedance connection to VCC and GND, is recommended.

PWM Dimming

The LED brightness is controlled by the pulse-width-modulated signal applied to the PWM pin. The APM80905 drives the LED current to the target level set by R_{SENSE} when the PWM pin is high and drives the LED current off when the PWM pin is low.

The dimming ratio is the ratio of the on-time to the period of the PWM signal. For example, by selecting a PWM period of 5 ms (200 Hz) and a PWM on-time of 5 µs, a dimming ratio of 0.1% can be achieved. This is sometimes referred to as 1000:1 dimming. In an actual application, the minimum dimming ratio is determined by various system parameters including: V_{IN}, V_{OUT}, inductance of the power inductor, LED current, switching frequency, and PWM frequency. The device is capable of PWM on-time as short as 5 µs; however, if fault flag operation for open or short LED detection is required, the PWM on-time must be greater than the maximum fault mask timer, t_{MASK}.

The PWM pin is a logic input pin and is internally pulled to GND through a 100 kΩ (typ) resistor. The EN and PWM pins function as illustrated in Table 1.

Table 1: EN and PWM Pin States

EN Pin	PWM Pin	FFn	VCC	LEDs
Low	x	X	OFF	OFF
High	Low/Open	X	ON	OFF
High	High	High	ON	ON
High	High	Low	ON	OFF

PWM Monitoring

The APM80905 continuously monitors the on-time and duty cycle of the incoming PWM signal and drives the FFn pin low and disables the LED current if a fault is detected.

On-Time Limit

The first PWM monitor is a maximum on-time limit. A TMAX fault is detected when the incoming PWM signal on-time exceeds the maximum on-time set by R_{TMAX}. A TMAX fault drives the FFn pin low and disables the LED current for the remainder of the PWM cycle. The TMAX fault is cleared on the next PWM rising edge. Use Equation 4 to calculate R_{TMAX} and refer to Figure 6.

Equation 4:

$$R_{TMAX} = 2.5413(t_{MAX})^2 + 25.527\ t_{MAX}$$

where t_{MAX} is in milliseconds and R_{TMAX} is in kΩ.

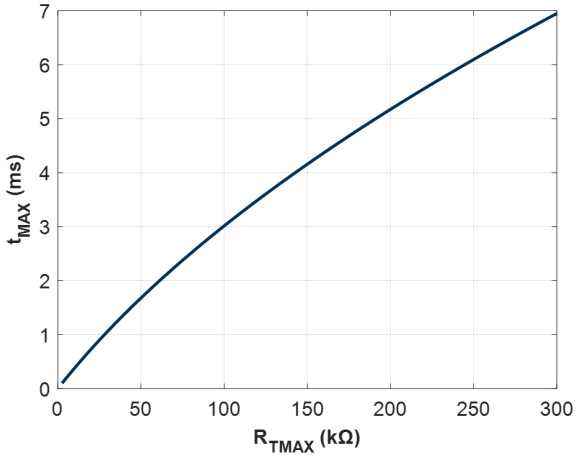

Figure 6: t_{MAX} vs. R_{TMAX}

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Duty Cycle Limit

The second PWM monitor circuit is a maximum duty cycle limit set by a resistor from the DMAX pin to GND, R_{DMAX}. The DMAX fault monitors the incoming PWM signal off-time, and determines duty cycle with respect to the on-time limit TMAX set with R_{TMAX}. A DMAX fault is triggered at a PWM rising edge when the PWM off-time is less than the minimum blanking time, t_{BLANK}, set by R_{DMAX}. A DMAX fault disables the LED current for at least t_{BLANK} and can be cleared on the next PWM rising edge after waiting t_{BLANK}. Calculate R_{DMAX} by first calculating the off-time, t_{BLANK}, at t_{MAX} using Equation 5.

Equation 5:

$$t_{BLANK} = t_{MAX}\left(\frac{1}{D_{MAX}} - 1\right)$$

where D_{MAX} is the maximum duty cycle percentage normalized from 0 to 1.

Then, solve for the resistor value of R_{DMAX} using the blanking time in Equation 6 and refer to Figure 7.

Equation 6:

$$R_{DMAX} = 0.1529 \times t_{BLANK}^2 + 6.5112 \times t_{BLANK} - 0.1486$$

where t_{BLANK} is in milliseconds and R_{DMAX} is in kΩ.

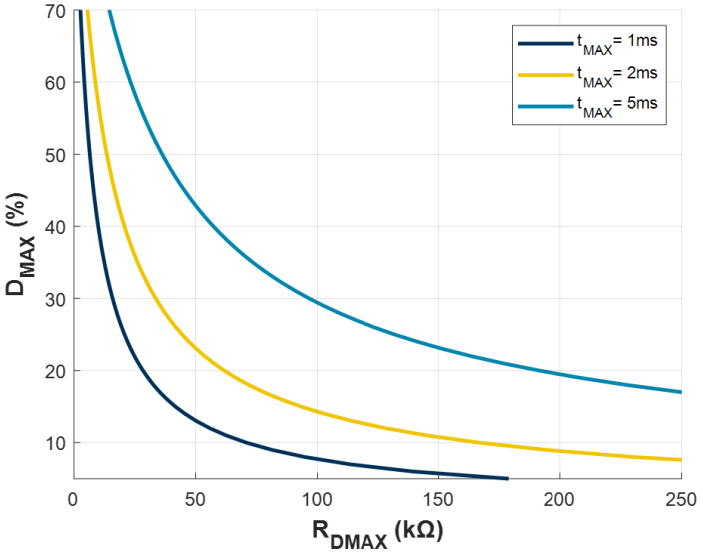

Figure 7: D_{MAX} vs. R_{DMAX}

The TMAX and DMAX fault scenarios are presented in Figure 8 to Figure 11. A dark blue line represents a signal external to the APM80905, a gray line represents an internal signal not responsible for triggering a fault, and a red line represents an internal signal responsible for triggering a fault.

Typical Operation

When the PWM signal on-time is less than the configured TMAX value and duty cycle is less than the configured DMAX value, there is not a reported fault and the LED current follows the PWM signal and the FFn pin remains high, as shown in Figure 8. The PWM on-time is less than the t_{MAX} timer and the PWM off-time is greater than the t_{BLANK} timer.

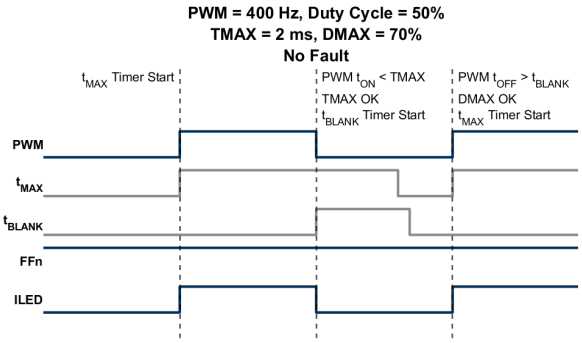

Figure 8: No TMAX or DMAX Fault

TMAX Fault

When the PWM signal on-time exceeds the configured TMAX value set by R_{TMAX}, the LED current is shut off and the FFn pin is pulled low. The fault is cleared on the next PWM rising edge. If the fault occurs again, the same process repeats, as shown in Figure 9.

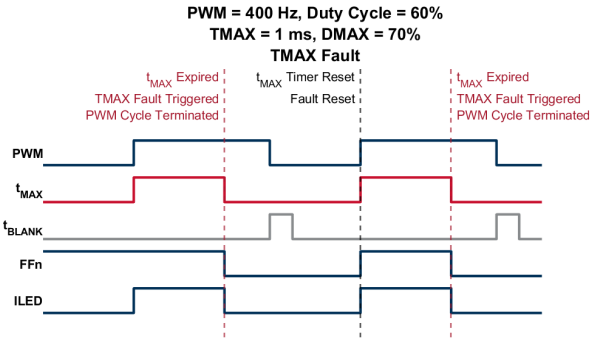

Figure 9: TMAX Fault

DMAX Fault

A DMAX fault occurs when the duty cycle exceeds the configured duty cycle limit set by R_{DMAX}. In Figure 10, the PWM on-time is less than the maximum set by the internal t_{MAX} timer so there is no TMAX fault, but the PWM off-time is less than the minimum required off-time of t_{BLANK}, which triggers a DMAX fault. The DMAX fault drives the FFn pin low and prevents the

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LED current from turning on for that PWM cycle. After waiting for at least the t_{BLANK} timer, the fault is reset upon the next PWM rising edge.

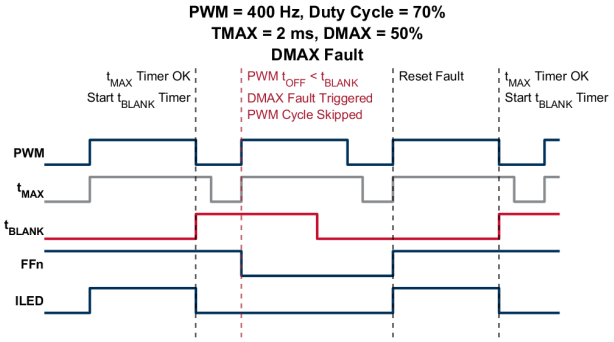

Figure 10: DMAX Fault

TMAX and DMAX Fault

Even if the LED cycle is terminated early due to a TMAX fault, the incoming PWM signal off-time must be greater than t_{BLANK}. If a DMAX fault is triggered following a TMAX fault, the LED current remains off and the PWM cycle is skipped, similar to the DMAX fault in Figure 11. When a DMAX fault follows a TMAX fault, the faults are reset by the falling edge of the next PWM pulse after the t_{BLANK} timer expires and the PWM pulse does not exceed t_{MAX}.

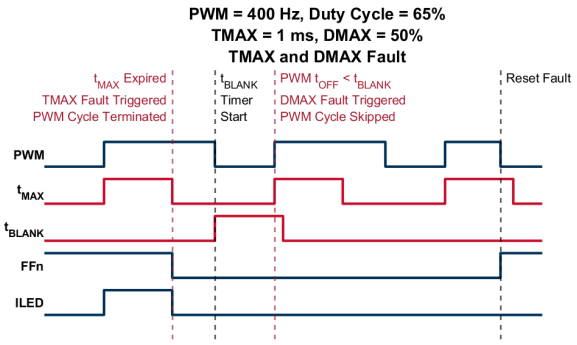

Figure 11: TMAX and DMAX Fault

Analog Dimming

The APM80905 includes an analog dimming feature that can be used for multiple applications including LED binning, extending the dimming ratio, or LED current foldback with increased LED temperature. Analog dimming adjusts the regulation voltage, V_{CSREG}, maintained across R_{SENSE}. The voltage on the ADIM pin, V_{ADIM}, determines the level of dimming applied. If analog dimming is not used, ADIM should be tied to VCC. The APM80905 does not detect an ADIM shorted to VCC fault because it is a valid operating state, where the LED current is not derated.

Dimming is not applied when V_{ADIM} exceeds 1.75 V. When V_{ADIM} is between 0.62 and 1.3 V, the LED current varies linearly with V_{ADIM} from 20% to 90%. The LED current regulation voltage, V_{CSREG}, can be calculated by Equation 7 or the dimming ratio by Equation 8, and is shown in Figure 12.

Equation 7:

$$V_{CSREG} = (V_{ADIM} - 0.42) \times 0.195$$

Equation 8:

$$DimPct = (V_{CSREG} / V_{CSNOM}) \times 100\%$$

where DimPct is the analog dimming percentage and V_{CSNOM}, the V_{CSREG} value with no dimming, is 0.195 V.

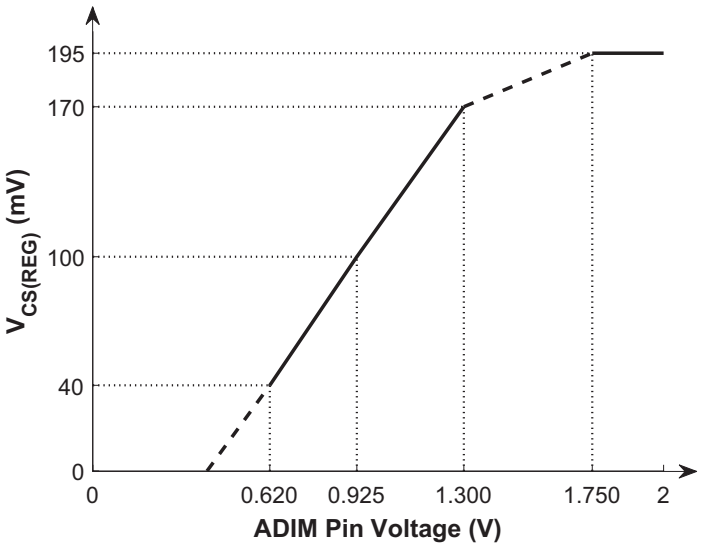

Figure 12: ADIM Pin Voltage vs. LED Current Reference Voltage

The voltage across the sense resistor must always be greater than 0 V, including at the valley of the inductor current ripple.

Temperature-based LED current foldback can be implemented as a voltage divider with an NTC thermistor on the ADIM pin, as shown in Figure 13. The resistors R_S and R_P can be added or removed as needed to tune the NTC voltage divider response.

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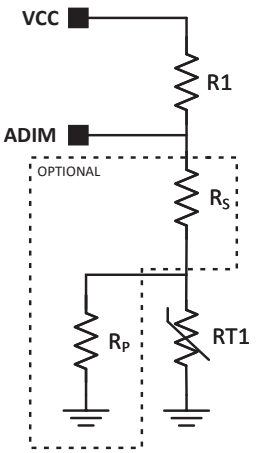

Figure 13: NTC Thermistor Circuit for Temperature-Based Output Current Foldback

Minimum and Maximum Output Voltages

The maximum output voltage is limited by the input voltage and the duty cycle of the power stage at the minimum off-time, $t_{OFF(MIN)}$. At higher switching frequencies, the minimum off-time becomes a larger percentage of the switching period, limiting the maximum duty cycle in the switching period. The same principal applies to the minimum output voltage at the minimum on-time, $t_{ON(MIN)}$. See Figure 14 for the minimum and maximum duty cycle for a given switching frequency. The output voltage range is a function of the input voltage and duty cycle range.

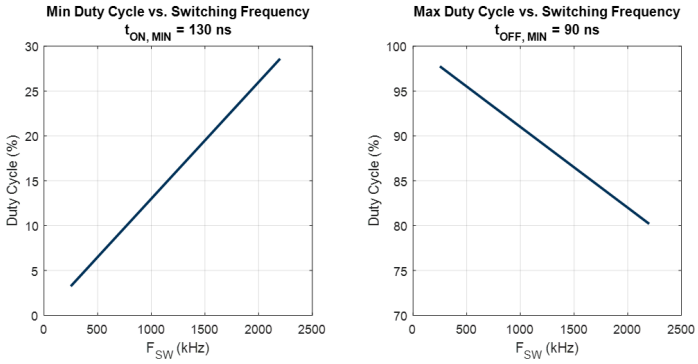

Figure 14: Duty Cycle Limits at $t_{ON(MIN)}$ and $t_{OFF(MIN)}$

For example, with a minimum off-time of 90 ns at f_{SW} = 2 MHz, the maximum duty cycle is 82% and, for an input voltage of 18 V, the maximum output voltage is approximately 14.76 V (based on the simplified equation of $V_{OUT} = V_{IN} \times D$, where D is the switching converter duty cycle). The maximum output voltage is also slightly reduced by the power loss and thermal condition of the IC.

Similarly, at a minimum on-time of 130 ns and f_{SW} = 2 MHz, the minimum duty cycle is 26%; therefore, with an input voltage of 9 V, the minimum V_{OUT} is 2.34 V. However, the internal current sense amplifier is designed to operate accurately down to V_{OUT} = 2.65 V. Therefore, the output voltage should not be less than 2.65 V; else, the output current accuracy becomes reduced.

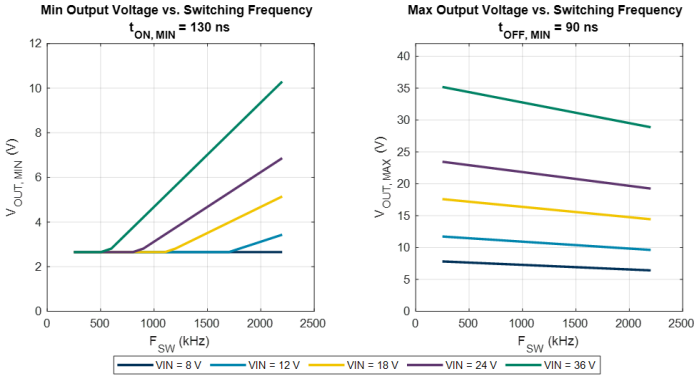

Figure 15: Minimum and Maximum Output Voltage

If the required output voltage is less than that permitted by the minimum on-time, the controller automatically extends the off-time to maintain the correct duty cycle. The result is that the switching frequency reduces more when necessary to keep the LED current in regulation.

If the LED string is completely shorted and V_{OUT} = 0 V, the controller enters hiccup mode and switches at the minimum on-time.

Boot Circuit

The APM80905 includes a bootstrap charging circuit with internal capacitor, C_{BOOT}. The internal boot capacitor is charged every switch cycle to ensure typical operation of the LED driver. Leave the BOOT pin open.

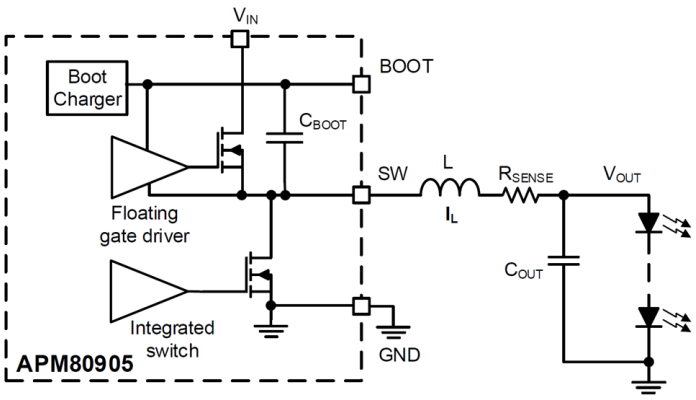

Figure 16: Boot Circuit

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Thermal Budgeting

The APM80905 can supply up to 4 A of output current, but system designers must ensure the total internal power dissipation does not induce thermal shutdown. The maximum power dissipation of the device is:

Equation 9:

$$P_{DISS(MAX)} = \frac{\Delta T}{\Theta_{JA}} = \frac{T_{J(MAX)} - T_{AMB}}{\Theta_{JA}}$$

For example, on a standard four-layer JEDEC board with 29°C/W thermal resistance, if the maximum ambient temperature is 100°C at the device case surface, the maximum internal power dissipation is 1.7 W.

Protection Functions

The APM80905 is designed to handle the following faults:

- Any pin-to-ground short
- Any pin-to-neighboring-pin short
- Any pin open
- External component open or short (inductor, resistors, capacitors, LEDs)
- Output-to-ground short
- LED PWM dimming signal on-time and duty cycle limits

Built-In Self-Test

The APM80905 includes a built-in self-test (BIST) that checks the internal monitoring circuits for correct operation. If the BIST fails, the APM80905 does not start and the FFn flag asserts low.

Fault Protection for Extreme Applications

In some applications, such as those with long cables harnesses or inductive loads, additional protection diodes as shown in Figure 13 may be necessary to prevent the voltage at the CSH and CSL pins from exceeding the absolute maximum ratings of the pins. Diode D1 adds protection during an output short-to-ground, and diode D2 adds protection during an output open fault. It is the responsibility of the application designer to determine if the output faults could present voltage beyond the absolute maximum ratings and to add D1 and D2 if necessary.

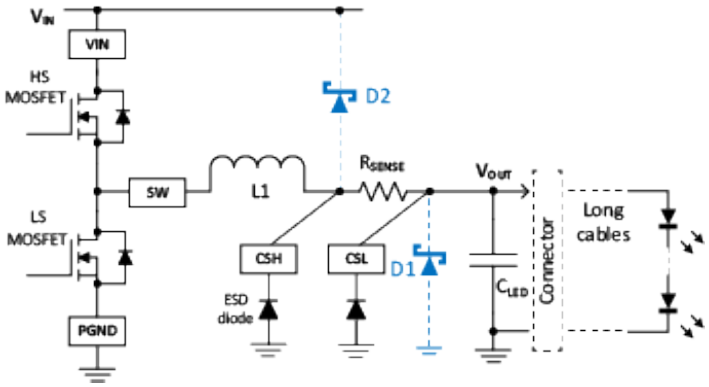

Figure 17: Optional Clamp Diodes

LED Faults

The APM80905 can detect open and short-to-ground LED strings. The diagram in Figure 18 shows the logic tree to report an open or short LED fault, as well as R_{TMAX}, R_{DMAX}, and R_{TON} open or short-to-ground.

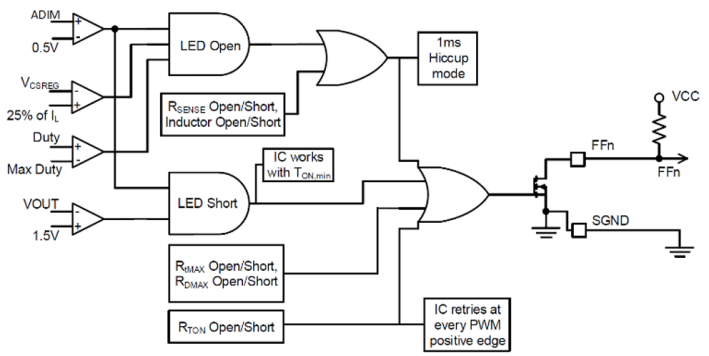

Figure 18: LED Open/Short Fault Block Diagram

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Open LED Fault

The APM80905 can detect when the LED string connection is opened. The fault must be present longer than the fault deglitch timer, t_{FDG}, and must exist after the PWM dimming mask timer at the start of each PWM cycle, t_{MASK}, expires to be detected. If the PWM on-time is less than t_{MASK}, the open LED fault is not detected. If the ADIM pin is less than 500 mV, the open LED fault is masked. To detect an open LED fault, ADIM must be greater than 500 mV, the regulation voltage V_{CSREG} must be less than 25% of the inductor current, and the converter duty cycle must be switching at its maximum duty cycle.

Upon open LED fault detection, the APM80905 asserts the fault flag by driving the FFn pin low and enters hiccup mode. When the fault condition is removed, the device recovers one hiccup period after the next PWM cycle by releasing the FFn pin to clear the fault flag and resumes typical regulation.

If the device is in a fault state and then ADIM reduces to less than 500 mV, the fault remains asserted. When PWM goes low, the fault flag is latched and maintains its state until the next PWM rising edge. See Figure 19.

Table 2: LED Open Fault Truth Table

ADIM	FFn^n	LED Open Fault?	Next PWM Rising Edge	FFn^{n+1}
High	x	No	↑	High
High	x	Yes	↑	Low
Low	Low	No	↑	High
Low	Low	Yes	x	Low
Low	1	x	x	1

ADIM high means V_{ADIM} > 500 mV; ADIM low means V_{ADIM} < 500 mV.

Output Short Fault

An output short condition, such as LED shorted to GND or output capacitor shorted to GND, is detected when V_{OUT} < 1.5 V. The fault must be present longer than the fault deglitch timer, t_{FDG}, and must exist after PWM dimming mask timer at the start of each PWM cycle, t_{MASK}, to be detected. If the PWM on-time is less than t_{MASK}, the output short fault is not detected. During an output short fault condition, the regulator does not enter hiccup mode, but only switches the power stage at the minimum on-time, and the fault flag is asserted by driving FFn low. When the fault condition is removed, the device resumes typical regulation and clears the fault flag by releasing the FFn pin. If V_{ADIM} < 500 mV, the output short fault is masked. When PWM goes low, the fault flag is latched and maintains its state until the next PWM rising edge. See Figure 19.

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Fault Detection Timers

The APM80905 has a fault deglitch timer, t_{FDG}, and a fault mask timer, t_{MASK}, which work together to prevent fault reporting for short, transient system events. The mask timer is typically twice as long as the deglitch timer.

Both timers are disabled when the PWM pin is low. The mask timer starts upon the PWM rising edge and prevents fault reporting for the beginning of each PWM pulse. The deglitch timer starts when PWM is high and a fault is detected. The two timers are independent and can overlap if a fault is detected while the mask timer is active. The FFn pin asserts low if a fault is present after both timers have expired.

The basic timing configurations are detailed in Figure 19. For each case, the TMAX and DMAX conditions are satisfied with no faults, and ADIM is greater than 500 mV.

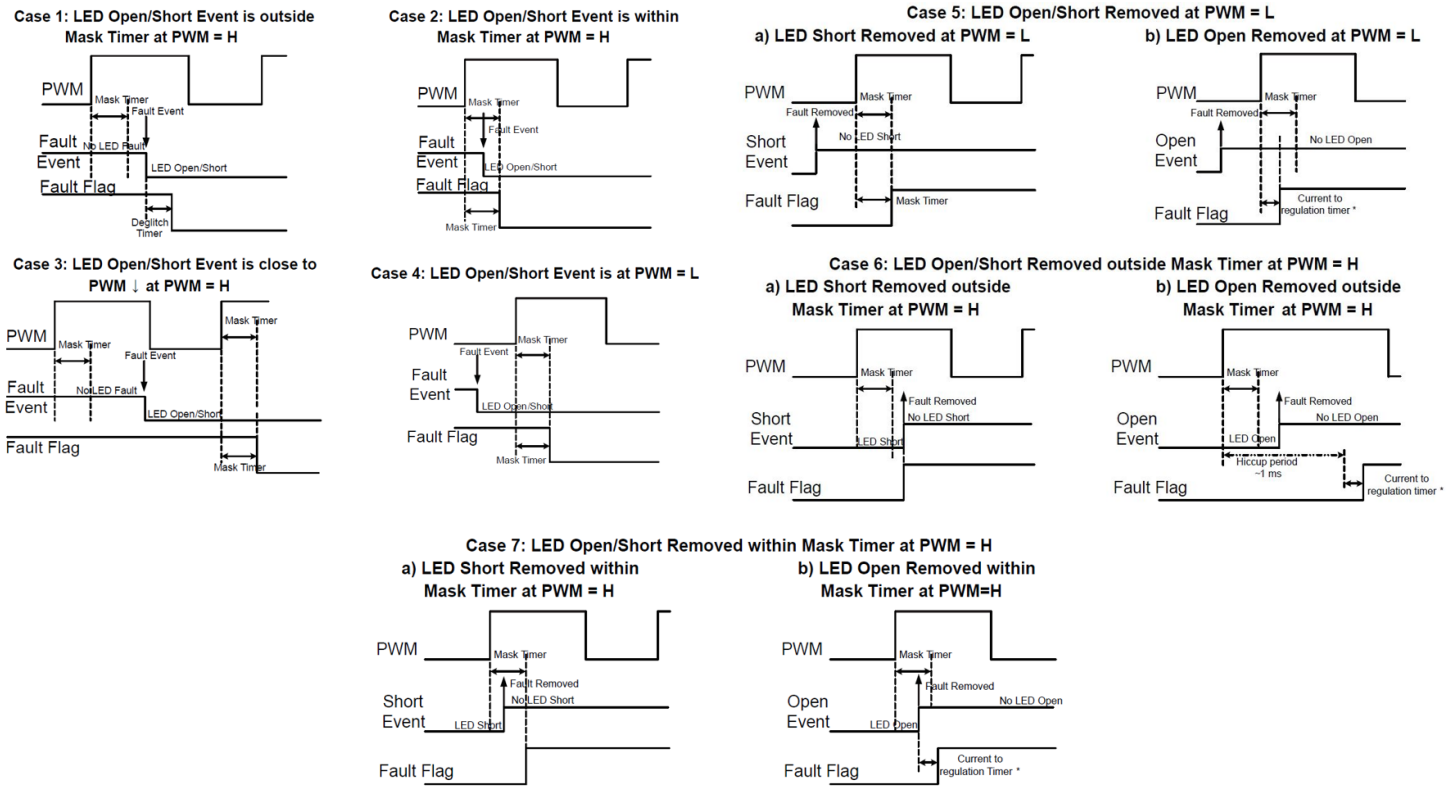

Figure 19: LED Short and Open Fault Timing Diagrams

*Current to regulation timer is 256 (Typical) switching cycles.

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Table 3: System Failure Mode Table

Failure Mode	Symptom Observed	FAULT Flag Asserted?	APM80905 Response
Inductor open	No light from LEDs	Yes [1]	Enter hiccup mode with 1 ms retry period.
Inductor shorted	Dim light from LEDs	Yes	Current through high-side MOSFET exceeds power switch current limit causing overcurrent fault. Switching stops and hiccup mode starts with 1 ms retry period.
Sense resistor open	Dim light from LEDs	Yes	Device switches with small switching duty cycle.
Sense resistor shorted	Dim light from LEDs	Yes	Triggers SW OCP fault, entering hiccup mode with 1 ms retry period.
LED string open	No light from LEDs	Yes [1]	Enters hiccup mode with 1 ms retry period.
LED strings shorted (Either LED shorted to GND or output capacitor shorted to GND) < 1.5 V	No light from LEDs	Yes [2]	Continues switching at minimum t_{ON}; regulator will not enter hiccup mode.
Output/CSL capacitor open	Typical light from LEDs	No	Possible decreased performance.
TON resistor open or short	Dim light from LEDs	Yes	Part will retry and recover on fault removal.
TMAX pin open or shorted to GND	No light from LEDs	Yes	LEDs remain off while pin is open or shorted to GND, will recover when fault is removed.
DMAX pin open or shorted to VCC or GND	No light from LEDs	Yes	LEDs remain off while pin is open or shorted to GND, will recover when fault is removed.
VCC shorted to GND	IC does not operate	[2]	Device cannot operate without V_{CC}. V_{CC} is internal protected against short to GND.
Undervoltage lockout	No light from LEDs	[3]	Device is in shutdown.

[1] For LED open or output short faults, a fault flag is not asserted when the V_{ADIM} < 500 mV or PWM dimming pulse width is less than fault mask timer.
[2] For VCC short-to-GND fault, the internal logic circuit does not operate. The FFn pin is floating.
[3] For UVLO, APM80905 enters shutdown mode. The FFn pin is floating.

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APPLICATION INFORMATION

Power Inductor Selection

To ensure stable operation while the LED current is on, the APM80905 should have a ripple voltage across the current sense resistor of at least 5 mV peak-to-peak. The voltage across the sense resistor must always be greater than 0 V, including at the valley of the inductor current ripple.

The recommended maximum inductor value can be calculated with Equation 10 at the minimum input voltage and maximum output voltage.

Equation 10:

$$L_{MAX} = \frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{f_{SW} \times \Delta I_{L(pp)}}$$

where $\Delta I_{L(pp)}$ is set to 10% of I_{OUT}.

The minimum recommended inductance by application is shown in Table 4. If the calculated $L_{MAX} < L_{MIN}$, use the L_{MIN} from Table 4.

The inductor current ripple, $\Delta I_{L(pp)}$, can be calculated with Equation 11.

Equation 11:

$$\Delta I_{L(pp)} = \frac{(V_{IN} - V_{OUT})\, t_{ON}}{L}$$

The inductor values in Table 4 represent suggested inductor values when $V_{SENSE} \geq 100$ mV, where $V_{SENSE} = V_{CSH} - V_{CSL}$.

Table 4: Minimum Inductor Value by Application

f_{SW} (kHz)	L_{MIN} (µH)	I_{OUT} (A)	V_{IN}-V_{OUT} Minimum Headroom (V)	V_{OUT} (V)
2250	3.3	4	4	2.65 to 5
			3	5 to 12
			3	12 to 32
		3	3.5	2.65 to 32
		2	2	
		1	2	
1500	3.6	1-4	3	2.65 to 32
1000	3.9	1-4	3	2.65 to 32
750	6.8	1-4	3	2.65 to 32
400	10	1-4	3	2.65 to 32

Output Filter Capacitor

The APM80905 is designed to operate in current regulation mode. Therefore, it does not require a large output capacitor to stabilize the output voltage. This results in lower solution cost and reduced PCB area requirements. The use of a large output capacitor is not recommended. In most applications, however, it is beneficial to add a small filter capacitor, approximately 0.47 µF, across the LED string to serve as a filter and eliminate any switching spikes that may be observed by the LED string, helping to reduce EMI. Avoid placing a capacitor at the CSH node of the current sense resistor to maintain higher ripple across the current sense resistor. A 0.1 µF ceramic capacitor placed very close to the CSL pin is also recommended.

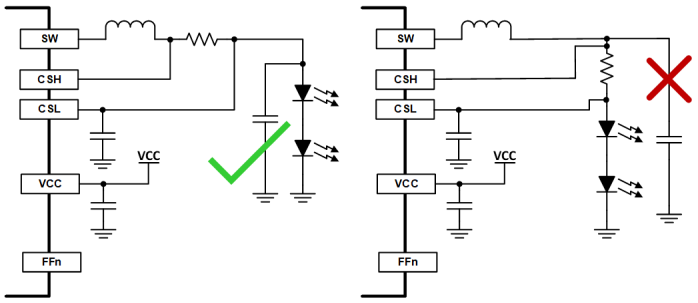

Figure 20: Recommended Output Capacitor Placement

Use of EN Pin for Input Undervoltage Protection

The EN pin is an input to a hysteretic comparator with 1.2 V (typ) threshold to enable the device. Once enabled, the EN comparator has a typical hysteresis of 100 mV and, if EN reduces to less than the 1.1 V (typ) turn-off threshold, the APM80905 enters shutdown.

The EN pin can be used with a voltage divider from VIN to create a configurable undervoltage lockout threshold, as shown in Figure 21.

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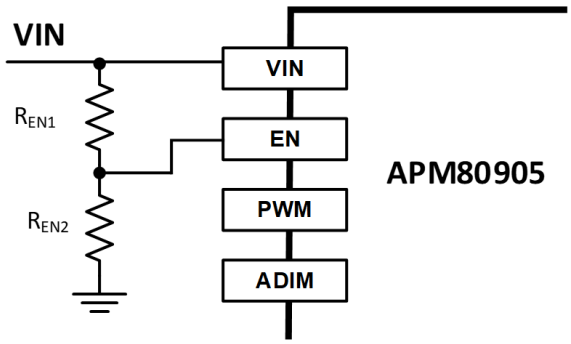

Figure 21: Input Undervoltage Lockout with EN pin

Select a convenient value for R_{EN2} and use Equation 12 to calculate R_{EN1} to estimate the rising enable threshold level. Use Equation 13 to estimate the falling input voltage threshold level once both resistors are known. Refer to the Electrical Characteristics section for $V_{EN(HI)}$, $V_{EN(HYS)}$, and I_{EN}.

Equation 12:

$$R_{EN1} = \frac{V_{INTH(RISE)} - V_{EN(HI)}}{I_{EN} + \frac{V_{EN(HI)}}{R_{EN2}}}$$

where $V_{INTH(RISE)}$ is the desired threshold of rising input voltage to enable the device and I_{EN} is the EN pin input current.

Equation 13:

$$V_{INTH(FALL)} = (V_{EN(HI)} - V_{EN(HYS)}) \times \left(\frac{R_{EN1} + R_{EN2}}{R_{EN2}} \right) + I_{EN}\, R_{EN1}$$

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APPLICATION CIRCUIT DIAGRAM

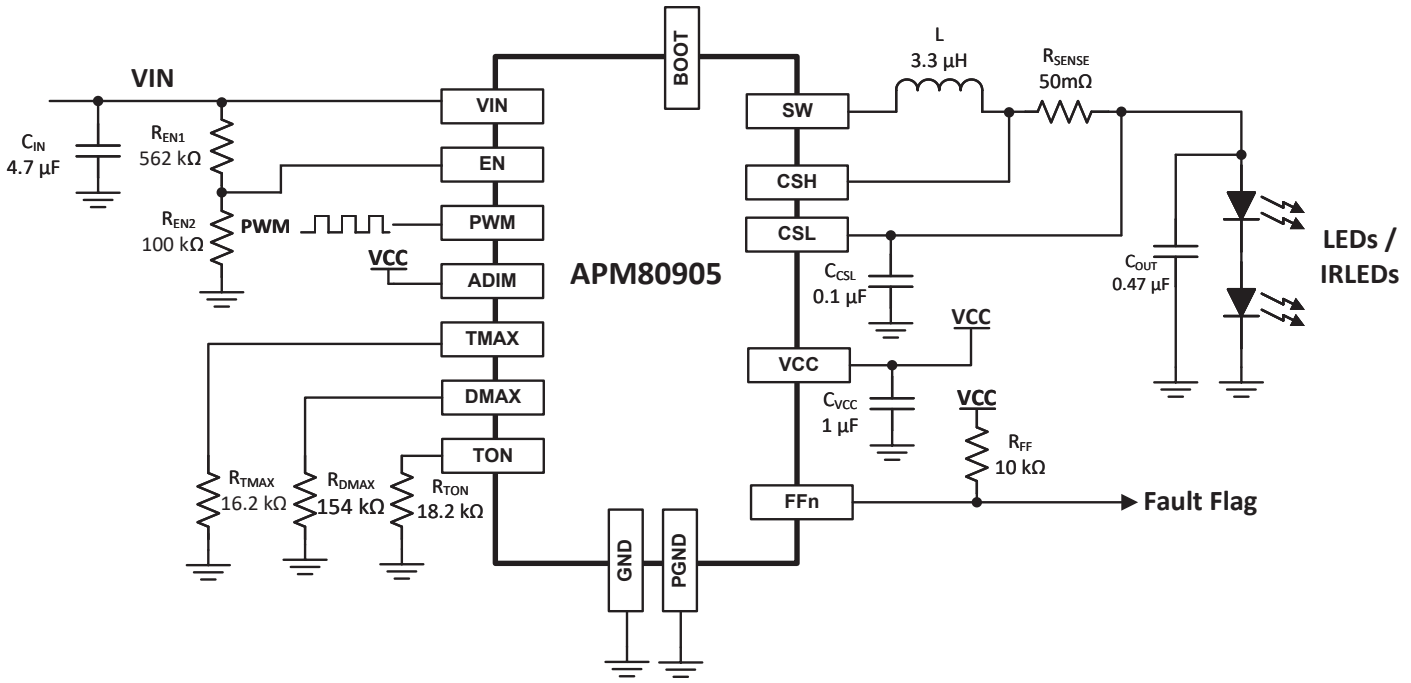

Figure 22: Application Circuit Diagram

Table 5: Design Requirements

Requirement		Symbol	Value	Unit
Input Voltage	Min	$V_{IN(MIN)}$	8	V
	Nominal	$V_{IN(NOM)}$	12	V
	Max	$V_{IN(MAX)}$	24	V
UVLO Power On		$V_{UVLO(ON)}$	8.5	V
Switching Frequency		f_{SW}	2.15	MHz
Output Current		I_{LED}	4	A
Infrared LED Forward Voltage Drop		V_{LEDF}	2.3	V
Number of IR LEDs		–	2	–
Analog Dimming		–	100	%
PWM LED Dimming Frequency		f_{PWM}	60	Hz
PWM LED Dimming Duty Cycle		D_{PWM}	10	%
PWM Max On-Time Protection		$t_{PWM(MAX)}$	3	ms
PWM Max Duty Cycle Protection		$D_{PWM(MAX)}$	15	%

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DESIGN PROCEDURE

This design procedure works through the component selection process for the two infrared LEDs with 60 Hz PWM application shown in the Application Circuit Diagram (Figure 22).

Output Current Sense Resistor

Use Equation 1 to calculate the sense resistor.

$$R_{SENSE} = \frac{195\ mV}{I_{LED}} = \frac{195\ mV}{4\ A} = 0.0488\ \Omega$$

Select a standard value of 50 mΩ.

Power Stage Switching Frequency

Use Equation 4 to calculate R_{TON}.

$$R_{TON} = \frac{1}{0.028 \times f_{SW(MHz)}} = 16.6\ k\Omega$$

Select a 1% standard value that is lower than calculated to keep the switching frequency slightly higher and away from the AM radio band, 16.2 kΩ .

Power Inductor

Use Equation 10 to calculate the inductor value at nominal V_{IN} with 10% output current ripple.

$$L_{MAX} = \frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{f_{SW} \times \Delta I_{L(pp)}} = \frac{4.6}{12} \times \frac{(12 - 4.6)}{2.15\ MHz \times 0.4} = 3.3\ \mu H$$

Referring to Table 4, the minimum inductance for applications switching at 2 MHz is 3.3 µH. Because $L_{MIN} = L_{MAX}$, continue with the value of 3.3 µH.

Using the same equation again at the minimum, V_{IN} yields L_{MAX} = 2.2 µH; however, the L_{MIN} requirement from Table 4 must be met first, so the selected inductor value remains 3.3 µH.

Use Equation 12 to calculate the output current ripple at each V_{IN} level for the selected inductor value.

Table 6: Output Ripple for Selected Inductor Value

V_{IN}	Inductor Value	Output Current Ripple	R_{SENSE}	Output Voltage Ripple
8 V	3.3 µH	278 mA (6.96 %)	50 mΩ	14 mV
12 V	3.3 µH	404 mA (10.1 %)	50 mΩ	20 mV
24 V	3.3 µH	529 mA (13.2 %)	50 mΩ	26 mV

This design meets the output voltage ripple requirement of greater than 5 mV peak-to-peak at all input voltages.

PWM Protections

Use Equation 4 to calculate R_{TMAX}.

$$R_{TMAX} = 2.5413(t_{MAX})^2 + 25.527\ t_{MAX} = 99.5\ k\Omega$$

Select a 1% standard value of 100 kΩ.

Use Equation 5 and Equation 6 to calculate R_{DMAX}.

$$t_{BLANK} = t_{MAX}\left(\frac{1}{D_{MAX}} - 1\right) = 0.017\ seconds$$

$$R_{DMAX} = 0.1529 \times t_{BLANK}^2 + 6.5112 \times t_{BLANK} - 0.1486 = 155\ k\Omega$$

Select a standard 1% value of 154 kΩ.

Analog Dimming

To disable analog dimming and regulate to 100% of the nominal output current, tie the ADIM pin to VCC.

Undervoltage Lockout

Use a voltage divider on the EN pin from VIN to customize the undervoltage lockout thresholds. Use Equation 12 to calculate the top resistor of the voltage divider. Set the bottom resistor, R_{EN2}, to 100 kΩ.

$$R_{EN1} = \frac{V_{INTH(RISE)} - 1.2\ V}{I_{EN} + \frac{1.2\ V}{R_{EN2}}} = \frac{8.5\ V - 1.2\ V}{1\ \mu A + \frac{1.2\ V}{100\ k\Omega}} = 561.5\ k\Omega$$

Select a standard 1% tolerance value of 562 kΩ.

Use R_{EN1}, R_{EN2}, and Equation 13 to calculate the UVLO turn-off threshold.

$$V_{INTH(FALL)} = (1.2\ V - 100\ mV) \times \left(\frac{R_{EN1} + R_{EN2}}{R_{EN2}}\right) + I_{EN}\ R_{EN1}$$

$$= 1.1\ V \times \left(\frac{662\ k\Omega}{100\ k\Omega}\right) + (1\ \mu A \times 562\ k\Omega) = 7.85\ V$$

With R_{EN1} of 60.4 kΩ and R_{EN2} of 10 kΩ, the device becomes enabled at an input voltage of 8.5 V and disabled at an input voltage of approximately 7.85 V (typical). At the nominal input voltage, 12 V, the resistor divider consumes approximately 18 µA.

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Output Capacitor

Add the recommended output filter capacitor of 0.47 µF after the sense resistor, across the LED string.

Additionally, a 0.1 µF ceramic capacitor close to the CSL pin is recommended for control-loop stability. A diode from CSL to ground can optionally be added.

Table 7: Application Component Values

Parameter	Symbol	Value	Unit
Output Current Sense Resistor	R_{SENSE}	50	mΩ
Power Stage On-Time Selection Resistor	R_{TON}	16.2	kΩ
Power Inductor	L	3.3	µH
PWM On-Time Protection Selection Resistor	R_{TMAX}	100	kΩ
PWM Duty Cycle Protection Selection Resistor	R_{DMAX}	154	kΩ
Undervoltage Lockout Top Resistor	R_{EN1}	562	kΩ
Undervoltage Lockout Bottom Resistor	R_{EN2}	100	kΩ
Output Capacitor	C_{OUT}	0.47	µF
CSL Stability Capacitor	C_{CSL}	0.1	µF

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PCB LAYOUT GUIDELINES

The APM80905 is designed to minimize electromagnetic (EM) emissions when proper PCB layout techniques are adopted. A good PCB layout is also critical for the APM80905 to provide clean and stable output voltages and current. Design guidelines for EMI/EMC-aware PCB layout and minimum $R_{\theta JA}$ are presented below. Figure 23 shows a sample PCB layout for the APM80905.

- Place the ceramic input capacitors as close as practical to the VIN pin and PGND pins to minimize the loop area; the traces of the input capacitors to the VIN pin should be short and wide to minimize the inductance. A bulk/electrolytic input capacitor can be located farther away from the VIN pin. The APM809805, input capacitors, and VIN traces should be on the same side of the board.
- The loop from the input supply and capacitors, through the high-side MOSFET and output inductor, to the output capacitors and back to ground, should be minimized and should use relatively wide traces.
- Place the output capacitor(s) across the LED load, after the sense resistor, to maintain ripple current through the sense resistor for the control loop. The output capacitor(s) must use a ground plane to make a very-low-inductance connection to the PCB GND.
- The output inductor, current sense resistor, and the APM80905 should be on the same board layer. Connect the output inductor and the current sense resistor with a wide trace.
- The current sense resistor should be placed close to the APM80905 CSH and CSL pins to minimize offset and gain error due to PCB parasitics. A ceramic capacitor, C_{CSL}, must be placed close to the CSL pin.
- Place the output inductor as close as practical to the SW pin with short and wide traces. The voltage at the SW node transitions from 0 V to V_{IN} with a high dV/dt rate. This node is the root cause of many noise issues. It is suggested to minimize the SW copper area to minimize the coupling capacitance between the SW node and other noise-sensitive nodes; however, the SW node area must be large enough to conduct high current. A copper ground area can be placed underneath the SW node to provide additional shielding.
- Place R_{TON}, R_{TMAX}, and R_{DMAX} as close as practical to their respective pins and avoid tying them to GND where large currents flow.
- Allegro recommends a four-layer PCB (top, L2, L3, bottom). Heavier copper layers, reduced material between layers, and a good amount of thermal vias are the keys to improved thermal performance. Use the top layer for routing high-current traces, the L2 layer for a solid GND plane, the L3 layer for most other routing, and the bottom layer for solid GND plane or, optionally, other components without low-impedance traces constraints—the FFn pull-up resistor could be on the bottom plane if desired.
- If a two-layer PCB (i.e., top and bottom layers only) is mandatory, place all components on the top layer and limit the routing only to the top layer. Use the bottom layer as the GND plane.
- When connecting the input and output ceramic capacitors, use multiple vias to GND planes and place the vias as close as practical to the pads of the components. Do not use thermal reliefs around the pads for the input and output ceramic capacitors.
- To minimize thermal resistance ($R_{\theta JA}$), extend ground planes on the top layer as much as practical, and use plenty of thermal vias to connect them to the GND plane in the bottom layer.
- To minimize PCB losses and improve system efficiency, the power traces should be as wide as reasonably possible.

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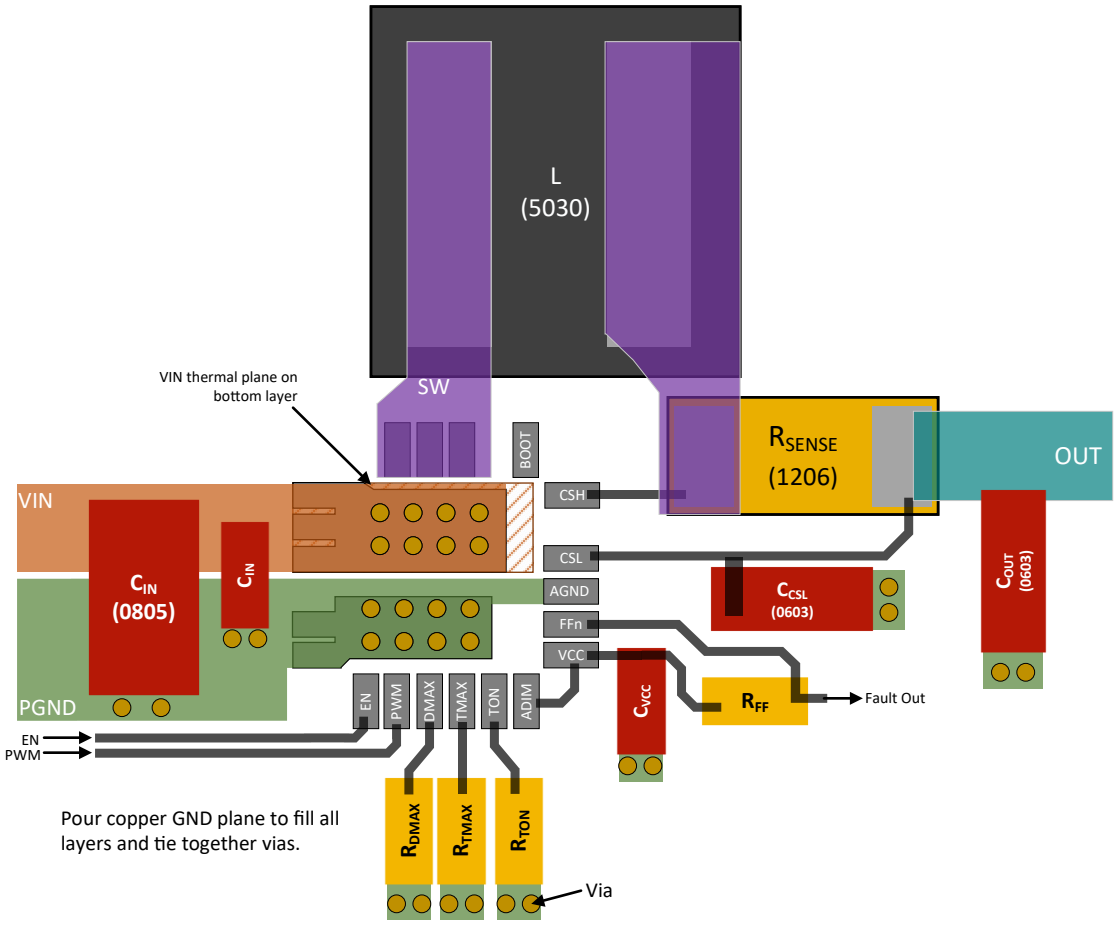

Figure 23: Sample PCB Layout

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PACKAGE OUTLINE DRAWING AND RECOMMENDED PCB FOOTPRINT

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000820, Rev. 2, incl. Appendix: APM80905)

NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

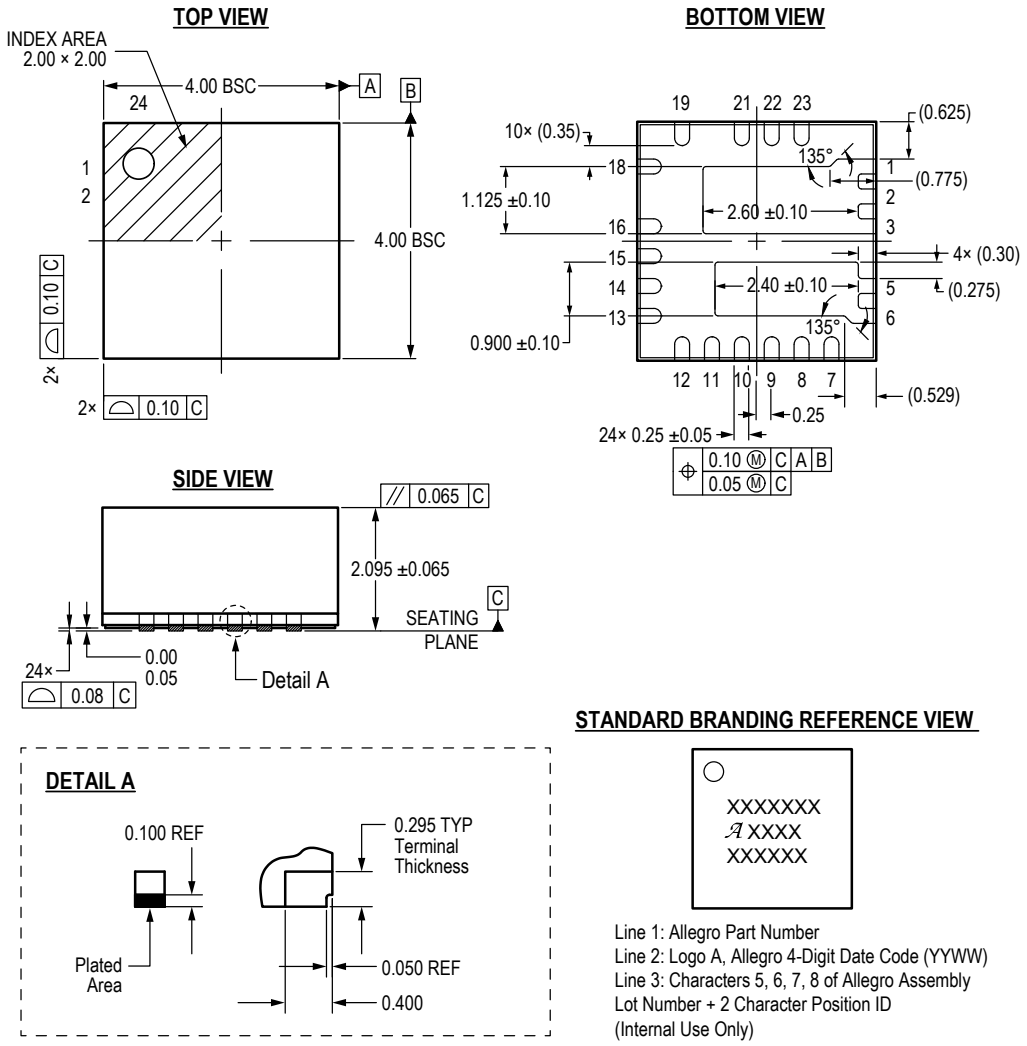

Figure 24: 24-Lead 4 mm × 4 mm QFN (Suffix NB)

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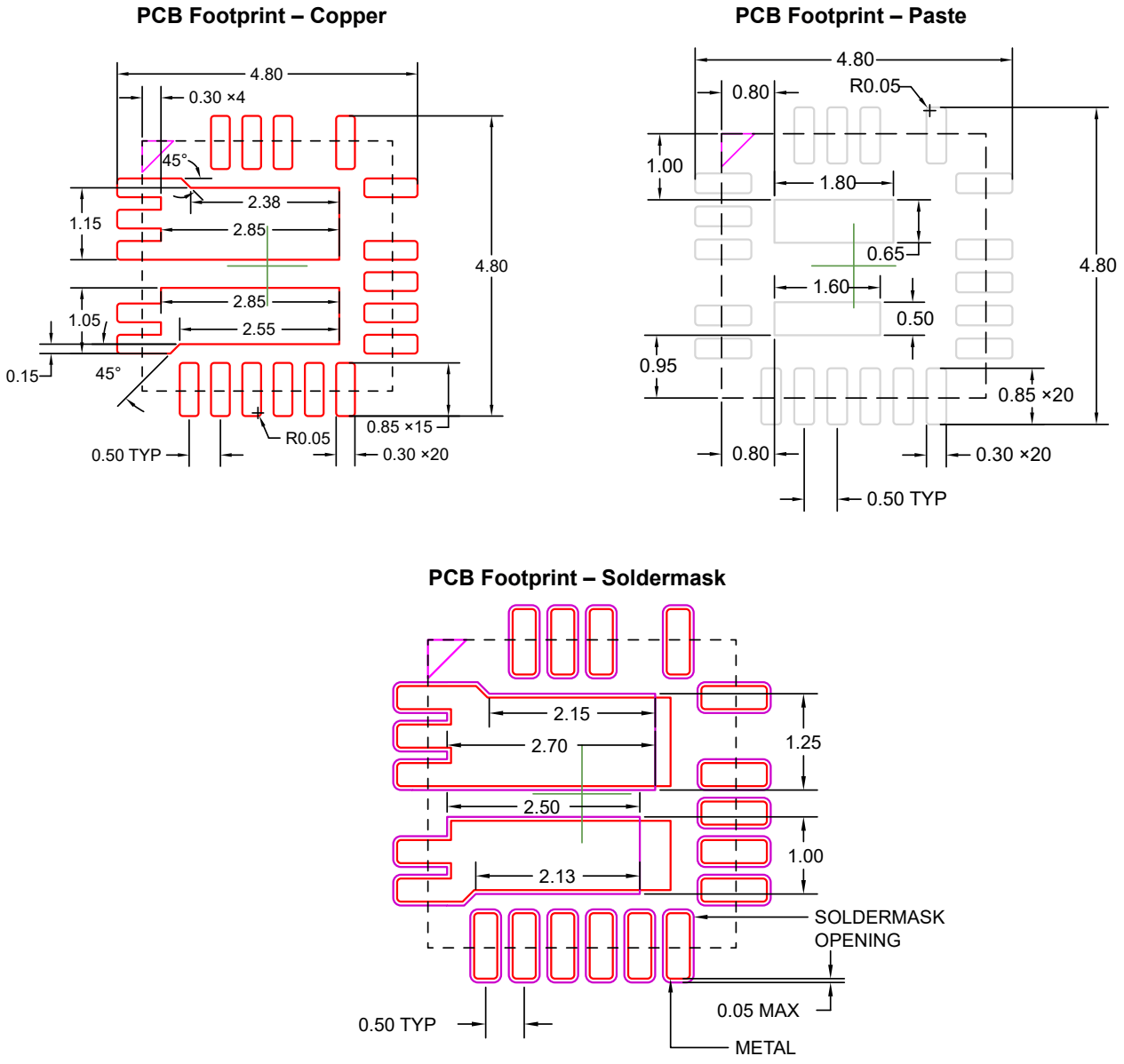

Figure 25: Recommended PCB Footprint

Altium and Cadence schematic and layout library files for the APM80905 are provided on the APM80905 product page at AllegroMicro.com.

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Revision History

Number	Date	Description
–	August 9, 2023	Initial release
1	September 19, 2023	Updated VCC to PGND pin capacitor ratings (pages 4 and 10)
2	October 10, 2023	Corrected package dimensions (page 1)
3	June 18, 2024	Amended part number to end in “-1” (headings, page 1, and page 3), updated product photo (page 1) updated branding reference view (page 25) and made minor editorial corrections throughout, including amending footnote numbers in characteristic tables to align with the order presented, changing future tense (“will”) to present tense, and changing the term “normal” to “typical”.

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