ARG81403

Automotive PMIC for Safety-Related Systems, with Synchronous Buck Pre-Regulator, 5× Post Regulators, 3× 2-Wire Speed Sensor IOs, 7× Level Shifter I/F, and SPI

FEATURES AND BENEFITS

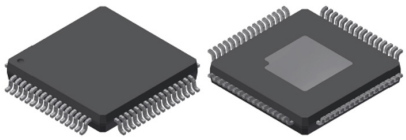
- Automotive AEC-Q100 qualified
- A²-SIL™ product—device features for safety-critical systems
- 6 to 36 V_{IN} operating range, 40 V_{IN} maximum
- 2.2 MHz synchronous buck pre-regulator (VREG)
- Adjustable synchronous buck regulator (1.275 V or 1.25 V typ)
- 3.3 V (3V3) and 5 V (V5) internal LDO regulators with foldback short-circuit protection
- 5 V (V5P1 and V5P2) internal tracking LDO regulator with foldback short-circuit and short-to-battery protections
- Power-on reset (NPOR) with fixed delay of 15 ms
- Selectable watchdog (single-ended or window timer)
- Active-low watchdog timer enable input (WDENn)
- Dual band gaps for increased reliability: BG_{VREF}, BG_{FAULT}
- Fixed POK5V undervoltage threshold for V5
- Three 2-wire speed (rotational) sensor IOs
- Seven logic level shifter I/F
- Logic enable input (ENB) for microprocessor control
- Ignition enable inputs (ENBAT and VIGN-IN)
- Control and Diagnostic reporting through a serial peripheral interface (SPI)
- Frequency dithering (SSCG) helps reduce EMI/EMC
- Overvoltage and undervoltage protection for all supply rails
- Thermal shutdown protection
- −40°C to 165°C junction temperature range

APPLICATIONS

- Transmission Control Units (TCU)
- Advanced Braking Systems (ABS)
- Electronic Power Steering (EPS)

PACKAGE:

64-Pin QFP (suffix JB)



Not to scale

DESCRIPTION

The ARG81403 is power management IC that uses a 2.2 MHz synchronous buck pre-regulator to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage, complete with control, diagnostics, and protections. The output of the pre-regulator supplies two 5 V / 100 mA tracking/protected LDOs, a 3.3 V / 150 mA LDO, a 5 V / 300 mA LDO, and an adjustable output synchronous buck regulator (1.275 V or 1.25 V_{TYP} / 1600 mA). Designed to supply power for microprocessors, sensors, and CAN transceivers, the ARG81403 is ideal for underhood applications.

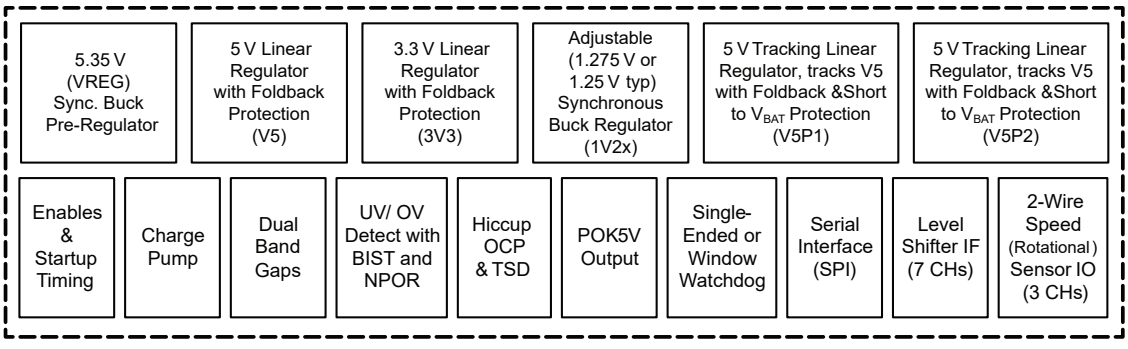
Enable inputs to the ARG81403 include a logic-level (ENB) input and high-voltage (ENBAT and VIGN-IN) inputs.

Diagnostic outputs from the ARG81403 include a power-on-reset output (NPOR) and a fault flag output (FFn) to alert the microprocessor that a fault has occurred. The microprocessor can read fault status through a serial peripheral interface (SPI). Dual band gaps, one for regulation and one for fault checking, improve safety coverage and fault detection of the ARG81403.

The ARG81403 implements three channels of 2-wire speed (rotational) sensor IOs with dedicated VIN terminal and seven channels of level shifter interfaces. The ARG81403 contains a selectable watchdog (single-ended timer and window timer) that can be programmed to accept a wide range of clock frequencies. The watchdog timer has a fixed activation delay to accommodate processor startup. The watchdog function has an enable/disable pin (active low, WDENn) to facilitate initial factory programming or field reflash programming.

Protection features include under- and overvoltage detection on all five supply rails. In case of a shorted output, all linear regulators feature foldback overcurrent protection. In addition, the V5Px output is protected from a short-to-battery event. Both switching regulators include pulse-by-pulse current limit, hiccup mode short-circuit protection and LX short-circuit protection.

The ARG81403 is supplied in a 64-lead low-profile quad flat package (suffix “JB”) with exposed thermal pad.



ARG81403 Simplified Block Diagram

SELECTION GUIDE

Part Number	Output Voltage of 1V2x (V_{TYP})	Package	Packing	Lead Frame
ARG81403KJBATR	1.275	64-pin QFP with thermal pad	900 pieces per 13-inch reel	100% matte tin
ARG81403KJBATR-1	1.25			

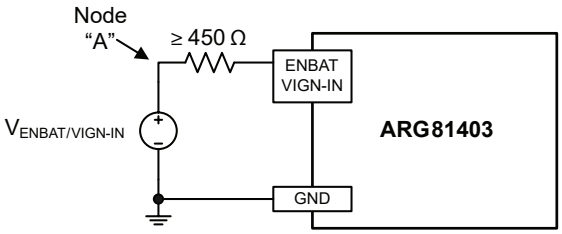
ABSOLUTE MAXIMUM RATINGS [1]

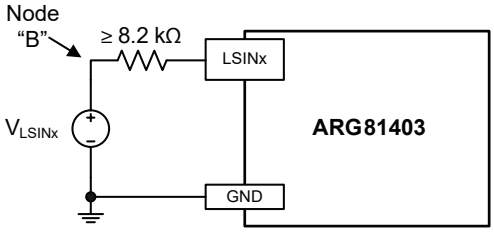
Characteristic	Symbol	Notes	Rating	Unit
Input Voltages	V_{VIN}, V_{SNSVIN}		–0.3 to 40	V
Ignition Enable Inputs	V_{ENBAT}, $V_{VIGN-IN}$	With current limiting resistor [2]	–13 to 40	V
			–0.3 to 8	V
	I_{ENBAT}, $I_{VIGN-IN}$		±75	mA
LX1	V_{LX1}		–0.3 to V_{VIN} + 0.3	V
		t < 250 ns	–1.5	V
		t < 50 ns	V_{VIN} + 3	V
VCP, CP2	V_{CP}, V_{CP2}		–0.3 to 50	V
CP1	V_{CP1}		–0.3 to 40	V
V5P1, V5P2	V_{V5Px}	Independent of V_{VIN}	–1 to 40	V
Rotational Sensor Inputs	V_{SNSxP}, V_{SNSxN}	Independent of V_{VIN}	–0.3 to 40	V
Level Shifter Inputs	V_{LSINx}		–0.3 to 40	V
		With current limiting resistor [3]	–13 to 40	V
All other pins			−0.3 to 7	V
Junction Temperature	$T_{J(max)}$		165	°C
Transient Junction Temperature	T_{JT}	Over temperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, determined by design characterization	175	°C
Storage Temperature Range	T_{stg}		−55 to 150	°C

[1]] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The higher ENBAT/VIGN-IN rating are measured at node “A” in the following circuit configuration.

[3] The higher LSINx rating are measured at node “B” in the following circuit configuration.





THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [4]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard footprint	27	°C/W

[4] Additional thermal information available on the Allegro website.

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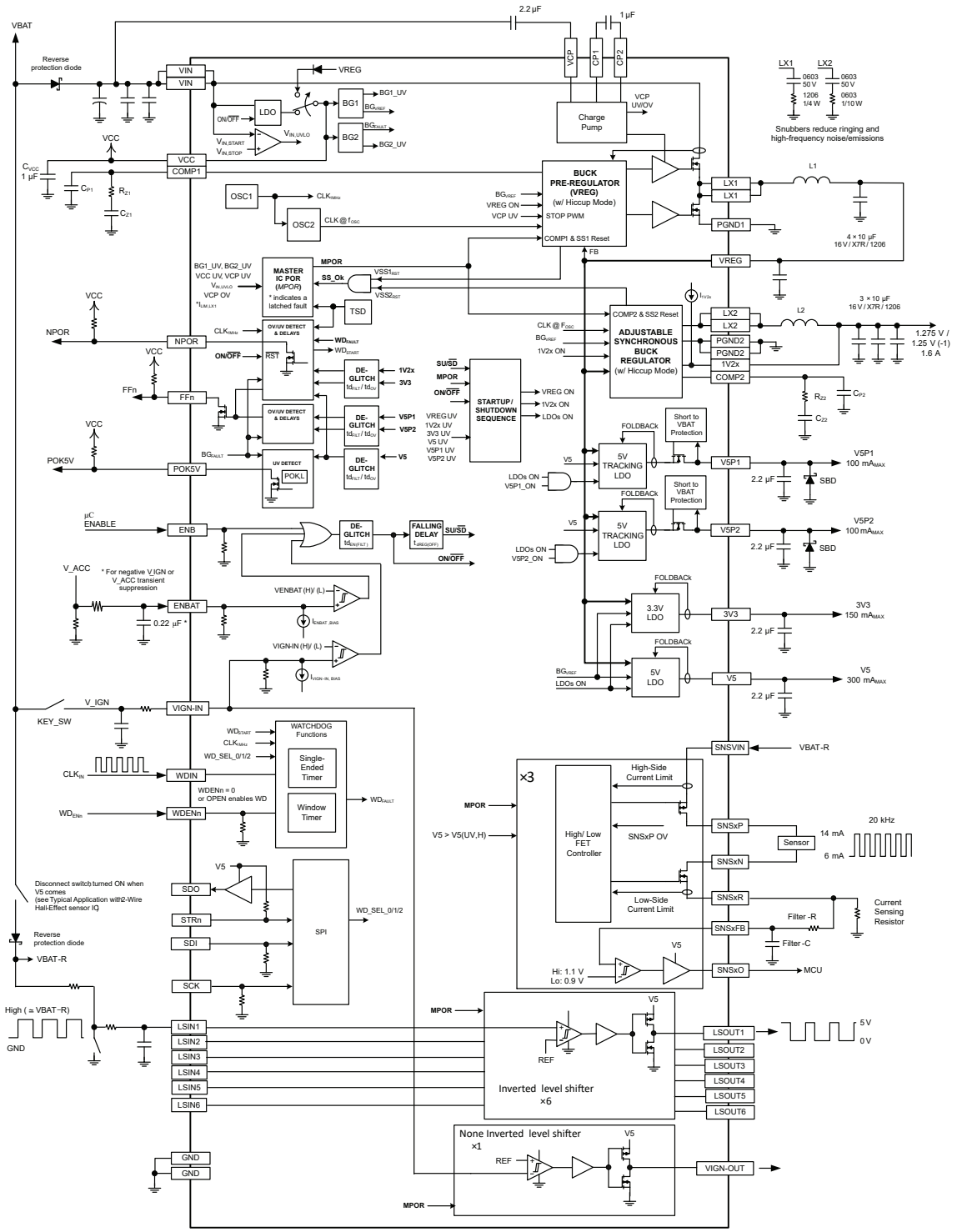
FUNCTIONAL BLOCK DIAGRAM



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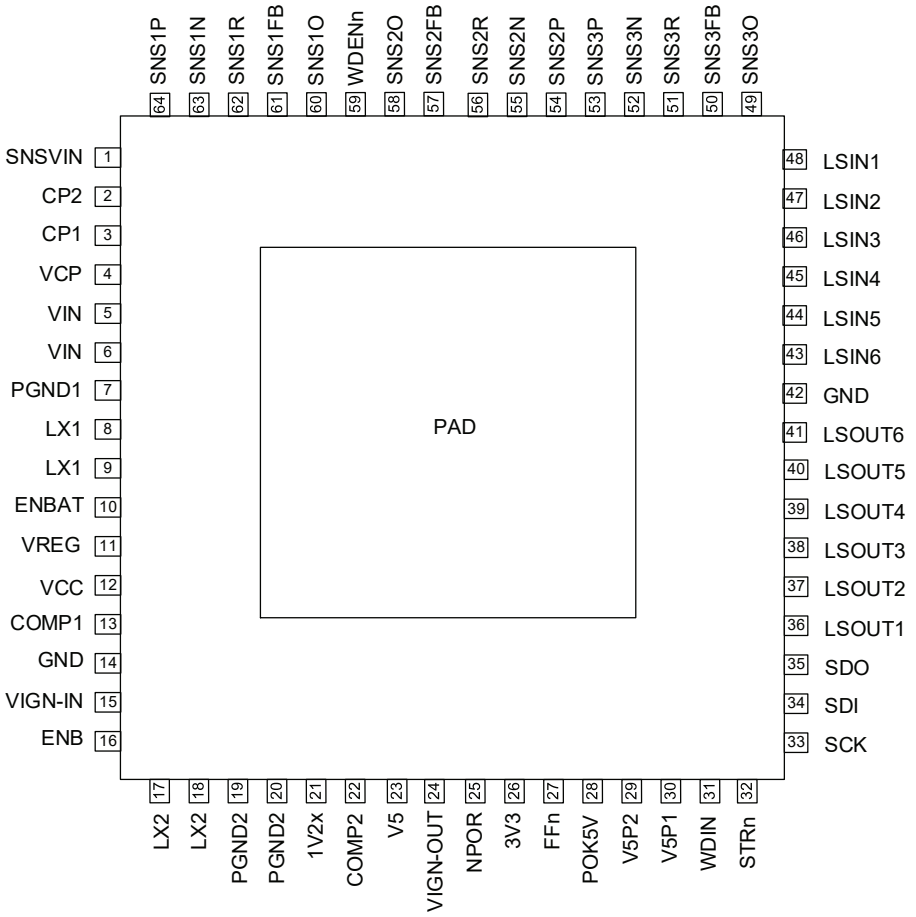
PINOUT DIAGRAM AND TERMINAL LIST



Package JB, 64-Pin QFP
Pinout Diagram

(Contact Allegro before
committing to PCB layout)

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Terminal List Table

Number	Name	Function
1	SNSVIN	Input voltage pin for rotational sensor IOs
2	CP2	Charge pump capacitor connection 2
3	CP1	Charge pump capacitor connection 1
4	VCP	Charge pump reservoir capacitor connection
5	VIN	Input voltage pin
6	VIN	Input voltage pin
7	PGND1	Power ground for SR buck pre-regulator
8	LX1	Switching node for SR buck pre-regulator
9	LX1	Switching node for SR buck pre-regulator
10	ENBAT	Ignition enable input from key/switch via a series resistor
11	VREG	Voltage feedback input of SR buck pre-regulator and input for LDOs and adjustable synchronous buck regulator
12	VCC	Internal voltage regulator bypass capacitor connection
13	COMP1	Error amplifier compensation network connection pin for SR buck pre-regulator
14	GND	Ground
15	VIGN-IN	Ignition enable and Level Shifter Input pin
16	ENB	Logic enable input from microcontroller
17	LX2	Switching node for adjustable synchronous buck regulator
18	LX2	Switching node for adjustable synchronous buck regulator
19	PGND2	Power ground for adjustable synchronous buck regulator
20	PGND2	Power ground for adjustable synchronous buck regulator
21	1V2x	Feedback pin for adjustable synchronous buck regulator
22	COMP2	Error amplifier compensation network connection pin for adjustable synchronous buck regulator
23	V5	5 V regulator output
24	VIGN-OUT	Ignition Level Shifter Logic Level output pin
25	NPOR	Active-low, open-drain regulator fault detection output
26	3V3	3.3 V regulator output
27	FFn	Active-low, open-drain Fault flag for microcontroller
28	POK5V	Power OK output indicating when V5 rail is out of regulation but not hitting undervoltage, threshold is $V_{V5(POK,L)}$
29	V5P2	5 V tracking/protected regulator output
30	V5P1	5 V tracking/protected regulator output
31	WDIN	Watchdog refresh input (rising edge triggered) from microcontroller or DSP
32	STRn	SPI Chip Select input for microcontroller
33	SCK	SPI Clock Input from microcontroller
34	SDI	SPI Data Input from microcontroller
35	SDO	SPI Data Output to microcontroller
36	LSOUT1	Level Shifter #1, Logic Level Output pin
37	LSOUT2	Level Shifter #2, Logic Level Output pin
38	LSOUT3	Level Shifter #3, Logic Level Output pin
39	LSOUT4	Level Shifter #4, Logic Level Output pin
40	LSOUT5	Level Shifter #5, Logic Level Output pin
41	LSOUT6	Level Shifter #6, Logic Level Output pin
42	GND	Ground
43	LSIN6	Level Shifter #6, Input pin
44	LSIN5	Level Shifter #5, Input pin
45	LSIN4	Level Shifter #4, Input pin
46	LSIN3	Level Shifter #3, Input pin
47	LSIN2	Level Shifter #2, Input pin
48	LSIN1	Level Shifter #1, Input pin
49	SNS3O	Rotational sensor #3, Logic Level Output
50	SNS3FB	Rotational sensor #3, Sensing Resistor feedback input
51	SNS3R	Rotational sensor #3, Sensing Resistor connection
52	SNS3N	Rotational sensor #3, Low Side Input connection
53	SNS3P	Rotational sensor #3, High Side Input connection
54	SNS2P	Rotational sensor #2, High Side Input connection
55	SNS2N	Rotational sensor #2, Low Side Input connection
56	SNS2R	Rotational sensor #2, Sensing Resistor connection
57	SNS2FB	Rotational sensor #2, Sensing Resistor feedback input
58	SNS2O	Rotational sensor #2, Logic Level Output
59	WDENn	Watchdog enable pin: Open/Low – WD is enabled; High – WD is disabled
60	SNS1O	Rotational sensor #1, Logic Level Output
61	SNS1FB	Rotational sensor #1, Sensing Resistor feedback input
62	SNS1R	Rotational sensor #1, Sensing Resistor connection
63	SNS1N	Rotational sensor #1, Low Side Input connection
64	SNS1P	Rotational sensor #1, High Side Input connection

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 6 V ≤ V_{VIN} / V_{SNSVIN} ≤ 36 V, T_J = 25°C; ● indicates specifications guaranteed –40°C ≤ T_J ≤ 150°C, ENB = High or ENBAT = High or VIGN-IN = High, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT VOLTAGE SPECIFICATIONS							
Operating Input Voltage [2][3]	V_{VIN}		●	6.0	13.5	36	V
VIN UVLO START Voltage	$V_{VIN(START)}$	V_{VIN} rising	●	5.45	5.7	5.95	V
VIN UVLO STOP Voltage	$V_{VIN(STOP)}$	V_{VIN} falling	●	2.95	3.2	3.45	V
VIN UVLO Hysteresis	$V_{VIN(HYS)}$	$V_{VIN(START)} – V_{VIN(STOP)}$	●	–	2.5	–	V
INPUT SUPPLY CURRENT							
Quiescent Current [1]	I_Q	V_{VIN} = 13.5 V, V_{VREG} = 5.6 V (no switching)	●	–	13	–	mA
Shutdown Current [1]	$I_{Q(SD)}$	V_{VIN} = 13.5 V, ENB = ENBAT = VIGN-IN = Low, T_J = 25°C		–	–	10	µA
		V_{VIN} = 13.5 V, ENB = ENBAT = VIGN-IN = Low, T_J = 85°C [3]		–	–	50	µA
PWM SWITCHING FREQUENCY AND DITHERING (SSCG)							
Switching Frequency	f_{OSC}	Dithering disabled	●	2.0	2.2	2.4	MHz
Dithering Frequency Range	f_{DITH}	As a percent of f_{OSC}	●	–	±12	–	%
Dither START VIN Threshold	$V_{INDS(ON-R)}$	V_{VIN} rising	●	8.5	9.0	9.5	V
	$V_{INDS(ON-F)}$	V_{VIN} falling	●	16	16.5	17	V
Dither STOP VIN Threshold	$V_{INDS(OFF-R)}$	V_{VIN} falling	●	7.8	8.3	8.8	V
	$V_{INDS(OFF-F)}$	V_{VIN} rising	●	16.5	17.2	17.8	V
PWM Frequency Foldback (VREG) VIN Threshold [3]	$V_{IN(FB)-R}$	V_{VIN} rising, 100% ON to $f_{OSC}/8$	●	5.2	5.4	5.6	V
		V_{VIN} rising, $f_{OSC}/8$ to $f_{OSC}/4$	●	6.2	6.4	6.6	V
		V_{VIN} rising, $f_{OSC}/4$ to $f_{OSC}/2$	●	6.6	6.8	7	V
		V_{VIN} rising, $f_{OSC}/2$ to f_{OSC}	●	7	7.3	7.5	V
		V_{VIN} rising, f_{OSC} to $f_{OSC}/2$	●	16.5	17.2	17.8	V
	$V_{IN(FB)-F}$	V_{VIN} falling, $f_{OSC}/2$ to f_{OSC}	●	16	16.5	17	V
		V_{VIN} falling, f_{OSC} to $f_{OSC}/2$	●	6.9	7.1	7.4	V
		V_{VIN} falling, $f_{OSC}/2$ to $f_{OSC}/4$	●	6.5	6.7	6.9	V
		V_{VIN} falling, $f_{OSC}/4$ to $f_{OSC}/8$	●	6.1	6.3	6.5	V
		V_{VIN} falling, $f_{OSC}/8$ to 100% ON	●	5.1	5.3	5.5	V
CHARGE PUMP (VCP)							
Output Voltage	V_{VCP}	V_{VCP} voltage w.r.t. VIN, V_{VIN} = 13.5 V	●	4.1	6.6	–	V
		V_{VCP} voltage w.r.t. VIN, V_{VIN} = 6 V	●	3.6	4.4	–	V
		V_{VCP} voltage w.r.t. VIN, V_{VIN} = 3.5 V	●	2.4	–	–	V
Switching Frequency	$f_{SW(CP)}$		●	–	65	–	kHz
Output Current Limit	$I_{LIM(VCP)}$	V_{VIN} = 13.5 V, $V_{VCP} – V_{VIN}$ = 2.5 V	●	–25	–50	–	mA
VCC VOLTAGE							
Output Voltage	V_{VCC}	V_{VREG} = 5.35 V	●	–	4.3	–	V

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[3] Ensured by design and characterization, not production tested.

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
PRE-REGULATOR OUTPUT VOLTAGE (VREG)							
VREG Feedback Voltage Accuracy	V_{VREG}	V_{VIN} = 13.5 V	●	–	5.35	–	V
			●	–1.9	–	+1.9	%
PULSE WIDTH MODULATION (VREG-PWM)							
Minimum Controllable SW On-Time	$t_{ON(MIN1)}$		●	–	90	120	ns
Minimum SW Off-Time	$t_{OFF(MIN1)}$		●	–	90	120	ns
Maximum Duty Cycle [3]	D_{MAX}	V_{VIN} < 7.8 V	●	–	–	100	%
COMP1 to LX1 Current Gain	gm_{POWER1}		●	–	4.57	–	A/V
Slope Compensation [3]	S_{E1}		●	1.1	1.43	2.15	A/µs
PWM Ramp Offset	$V_{PWM1(OFFS)}$	V_{COMP1} for 0% duty cycle	●	–	500	–	mV
ERROR AMPLIFIER (VREG-COMP1)							
Open Loop Voltage Gain [3]	A_{VOL1}		●	–	60	–	dB
Transconductance	gm_{EA1}	After startup	●	520	820	1120	µA/V
Output Current	I_{EA1}		●	–	±75	–	µA
Maximum Output Voltage	$V_{EA1VO(max)}$		●	0.9	1.6	2.1	V
COMP1 Pull-Down Resistance	R_{COMP1}		●	–	1	–	kΩ
INTERNAL MOSFET PARAMETERS (VREG: LX1)							
High-Side MOSFET On-Resistance	$R_{ds(on)HS}$	V_{VIN} = 13.5 V, T_J = –40°C [3], I_{DS1} = 0.9 A		–	75	95	mΩ
		V_{VIN} = 13.5 V, T_J = 25°C [3], I_{DS1} = 0.9 A		–	110	140	mΩ
		V_{VIN} = 13.5 V, T_J = 150°C, I_{DS1} = 0.9 A		–	180	210	mΩ
Low-Side MOSFET On-Resistance	$R_{ds(on)LS}$	V_{VIN} = 13.5 V, T_J = –40°C [3], I_{DS1} = 0.9 A		–	85	110	mΩ
		V_{VIN} = 13.5 V, T_J = 25°C [3], I_{DS1} = 0.9 A		–	130	165	mΩ
		V_{VIN} = 13.5 V, T_J = 150°C, I_{DS1} = 0.9 A		–	230	280	mΩ
High-Side Leakage Current	$I_{LKG(HS1)}$	V_{LX1} = 0V, V_{VIN} = 13.5 V, –40°C < T_J < 85°C [3]		–	–	10	µA
Low-Side Leakage Current	$I_{LKG(LS1)}$	V_{LX1} = 5.35V, V_{VIN} = 13.5 V, –40°C < T_J < 85°C [3]		–	–	10	µA
LX Rising Slew Rate Control [3]	$LX1_{RISE}$	V_{VIN} = 13.5V, 10% to 90%, I_{VREG} = 0.6 A	●	–	1.4	–	V/ns
LX Falling Slew Rate [3]	$LX1_{FALL}$	V_{VIN} = 13.5V, 10% to 90%, I_{VREG} = 0.6 A	●	–	1.5	–	V/ns

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
SOFT START (VREG)							
VREG Soft Start Ramp Time [3]	t_{SS1}		●	–	1	–	ms
PWM FREQUENCY FOLDBACK (VREG)							
PWM Frequency Foldback (VREG)	$f_{SW1(FB)}$	V_{VREG} < 1.3 V_{TYP}, V_{COMP1} = $V_{EA1VO(max)}$	●	–	f_{OSC}/8	–	–
		V_{VREG} < 1.3 V_{TYP}, V_{COMP1} < $V_{EA1VO(max)}$	●	–	f_{OSC}/4	–	–
		1.3 V_{TYP} < V_{VREG} < 2.7 V_{TYP}, V_{COMP1} < $V_{EA1VO(max)}$	●	–	f_{OSC}/2	–	–
		V_{VREG} > 2.7 V_{TYP}, V_{COMP1} < $V_{EA1VO(max)}$	●	–	f_{OSC}	–	–
HICCUP MODE (VREG)							
Hiccup OCP PWM Counts	$t_{HIC1(OCP)L}$	V_{VREG} < 1.3 V_{TYP}, V_{COMP1} = $V_{EA1VO(max)}$	●	–	30	–	PWM cycles
	$t_{HIC1(OCP)H}$	V_{VREG} > 1.3 V_{TYP}, V_{COMP1} = $V_{EA1VO(max)}$	●	–	120	–	PWM cycles
CURRENT PROTECTION (VREG)							
Pulse-by-Pulse Current Limit	$I_{LIM1(ton,min)}$		●	2.5	2.8	3.3	A
LX1 Short-Circuit Current Limit	$I_{LIM(LX1)}$	Latched fault after 3rd detection	●	6.0	7.0	–	A
Low-Side MOSFET Reverse Current Limit (Drain to Source)	$I_{LIM(LX1)Lo}$		●	–	1	–	A

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Characteristic	Symbol	Test Conditions			Min.	Typ.	Max.	Unit
ADJUSTABLE SYNCHRONOUS BUCK REGULATOR (1V2X)								
1V2x Feedback Voltage Accuracy	V_{1V2x}	V_{VREG} = 5.35 V	ARG81403	●	–	1.275	–	V
				●	–2	–	+2	%
			ARG81403-1	●		1.25		V
				●	–2	–	+2	%
PULSE WIDTH MODULATION (1V2X-PWM)								
Minimum Controllable SW On-Time	$t_{ON(MIN2)}$			●	–	65	105	ns
Minimum SW Off-Time	$t_{OFF(MIN2)}$			●	–	100	125	ns
Gate Drive Non-Overlap Time [3]	t_{NO2}			●	–	8	–	ns
COMP2 to LX2 Current Gain	gm_{POWER2}			●	–	3.7	–	A/V
Slope Compensation [3]	SE_2			●	0.45	0.7	0.95	A/µs
PWM Ramp Offset	$V_{PWM2(OFFS)}$	V_{COMP2} for 0% duty cycle		●	–	400	–	mV
ERROR AMPLIFIER (1V2X-COMP2)								
Feedback Input Bias Current [3]	I_{1V2x}	V_{COMP2} = 0.8 V, 1V2x regulated so that I_{COMP2} = 0 A		●	–	–150	–350	nA
Open Loop Voltage Gain [3]	A_{VOL2}			●	–	60	–	dB
Transconductance	gm_{EA2H}	I_{COMP2} = 0 µA, V_{SS2} > 500 mV, internal signal		●	515	900	1350	µA/V
	gm_{EA2L}	V_{SS2} < 500 mV, internal signal		●	–	250	–	µA/V
Source and Sink Current	I_{EA2}			●	–	±50	–	µA
Maximum Output Voltage	$V_{EA2VO(max)}$			●	1.0	1.3	1.7	V
COMP2 Pull-Down Resistance	R_{COMP2}	When 1V2x is in OFF state		●	–	1.5	–	kΩ

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 6 V ≤ V_{VIN} / V_{SNSVIN} ≤ 36 V, T_J = 25°C; ● indicates specifications guaranteed –40°C ≤ T_J ≤ 150°C, ENB = High or ENBAT = High or VIGN-IN = High, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INTERNAL MOSFET PARAMETERS (1V2X: LX2)							
High-Side On Resistance	$R_{ds(on)HS2}$	V_{VREG} = 5.35 V, T_J = 25°C [3], I_{DS2} = 0.1 A		–	275	350	mΩ
		V_{VREG} = 5.35 V, I_{DS2} = 0.1 A	●	–	–	550	mΩ
Low-Side On Resistance	$R_{ds(on)LS2}$	V_{VREG} = 5.35 V, T_J = 25°C [3], I_{DS2} = 0.1 A		–	135	175	mΩ
		V_{VREG} = 5.35 V, I_{DS2} = 0.1 A	●	–	–	270	mΩ
High-Side Leakage Current	$I_{LKG(HS2)}$	V_{LX2} = 0 V, V_{VREG} = 5.35 V, −40°C < T_J < 85°C [3]		–	–	2	µA
		V_{LX2} = 0 V, V_{VREG} = 5.35 V	●	–	–	15	µA
Low-Side Leakage Current	$I_{LKG(LS2)}$	V_{LX2} = 5.35 V, V_{VIN} = 13.5 V, −40°C < T_J < 85°C [3]		–	–	2	µA
		V_{LX2} = 5.35 V, V_{VIN} = 13.5 V	●	–	–	30	µA
LX2 Rise Time [3]	$t_{LX2RISE}$	V_{VREG} = 5.35 V, 10% to 90%, I_{1V2} = 0.1 A	●	–	7	–	ns
LX2 Fall Time [3]	$t_{LX2FALL}$	V_{VREG} = 5.35 V, 10% to 90%, I_{1V2} = 0.1 A	●	–	6	–	ns
SOFT START (1V2X)							
1V2x Soft Start Ramp Time [3]	t_{SS2}		●	–	1	–	ms
PWM FREQUENCY FOLDBACK (1V2X)							
1V2x PWM Frequency Foldback	$f_{SW2(FB)}$	V_{1V2x} < 450 mV_{TYP}	●	–	f_{OSC}/4	–	–
		450 mV_{TYP} < V_{1V2x} < 780 mV_{TYP}	●	–	f_{OSC}/2	–	–
		V_{1V2x} > 780 mV_{TYP}	●	–	f_{OSC}	–	–
HICCUP MODE (1V2X)							
Hiccup2 OCP PWM Counts	$t_{HIC2(OCP)L}$	V_{1V2x} < 450 mV_{TYP}	●	–	30	–	PWM cycles
	$t_{HIC2(OCP)H}$	V_{1V2x} > 450 mV_{TYP}	●	–	120	–	PWM cycles
CURRENT PROTECTION (1V2X)							
High-Side MOSFET Pulse-by-Pulse Current Limit	$I_{LIM2(ton,min)H}$		●	1.8	2.6	3.3	A
Low-Side MOSFET Reverse Current Limit (Drain to Source)	$I_{LIM(LX2)Lo}$		●	–	1	–	A

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
V5 LINEAR REGULATORS							
V5 Accuracy and Load Regulation	V_{V5}	10 mA < I_{V5} < 300 mA, V_{VREG} = 5.25 V	●	4.9	5.0	5.1	V
V5 Dropout 1	$V_{V5(DO)1}$	T_J = –40°C, V_{VIN} = 3.5 V, I_{V5} = 230 mA, I_{V5P1} = 10 mA, I_{V5P2} = 10 mA, I_{3V3} = 50 mA, I_{1V2x} = 800 mA,		$V_{V5(UV,L)max}$	–	–	V
V5 Dropout 2	$V_{V5(DO)2}$	T_J =150°C, V_{VIN} = 3.65 V, I_{V5} = 230 mA, I_{V5P1} = 10 mA, I_{V5P2} = 10 mA, I_{3V3} = 50 mA, I_{1V2x} = 1200 mA		$V_{V5(UV,L)max}$	–	–	V
V5 Dropout 3	$V_{V5(DO)3}$	T_J = –40°C, V_{VIN} = 5.2 V, I_{V5} = 230 mA, I_{V5P1} =10 mA, I_{V5P2} = 10 mA, I_{3V3} = 50 mA, I_{1V2x} = 800 mA		$V_{V5(POK,L)max}$	–	–	V
V5 Dropout 4	$V_{V5(DO)4}$	T_J = 150°C, V_{VIN} = 5.2 V, I_{V5} = 230 mA, I_{V5P1} = 10 mA, I_{V5P2} = 10 mA, I_{3V3} = 50 mA, I_{1V2x} = 1200 mA		$V_{V5(POK,L)max}$	–	–	V
V5 Output Capacitance [3]	$C_{OUT(V5)}$		●	1.0	–	22	µF
V5 Current Limit [1]	$I_{LIM(V5)}$	V_{V5} = 5 V	●	–330	–470	–	mA
V5 Foldback Current [1]	$I_{FBK(V5)}$	V_{V5} = 0 V	●	–60	–120	–180	mA
V5 Startup Time [3]	$t_{SU(V5)}$	C_{V5} ≤ 2.9 µF, Load = 33 Ω ±5% (150 mA)	●	–	–	1	ms
V5P1 LINEAR REGULATORS							
V5P1 Accuracy and Load Regulation	V_{V5P1}	10 mA < I_{V5P1} < 100 mA, V_{VREG} = 5.25 V	●	4.9	5.0	5.1	V
V5P1/V5 Tracking Accuracy	$V_{V5P1(TRACK)}$	I_{V5P1} = 50 mA, I_{V5} = 50 mA	●	–25	–	25	mV
V5P1 Output Capacitance [3]	$C_{OUT(V5P1)}$		●	1.0	–	22	µF
V5P1 Current Limit [1]	$I_{LIM(V5P1)}$	V_{V5P1} = 5 V	●	–110	–155	–	mA
V5P1 Foldback Current [1]	$I_{FBK(V5P1)}$	V_{V5P1} = 0 V	●	–20	–40	–70	mA
V5P1 Startup Time [3]	$t_{SU(V5P1)}$	C_{V5P1} ≤ 2.9 µF, R_{Load} = 100 Ω ±5% (50 mA)	●	–	–	1	ms
V5P2 LINEAR REGULATORS							
V5P2 Accuracy and Load Regulation	V_{V5P2}	10 mA < I_{V5P2} < 100 mA, V_{VREG} = 5.25 V	●	4.9	5.0	5.1	V
V5P2/ V5 Tracking Accuracy	$V_{V5P2(TRACK)}$	I_{V5P2} = 50 mA, I_{V5} = 50 mA	●	–25	–	25	mV
V5P2 Output Capacitance [3]	$C_{OUT(V5P2)}$		●	1.0	–	22	µF
V5P2 Current Limit [1]	$I_{LIM(V5P2)}$	V_{V5P2} = 5 V	●	–110	–155	–	mA
V5P2 Foldback Current [1]	$I_{FBK(V5P2)}$	V_{V5P2} = 0 V	●	–20	–40	–70	mA
V5P2 Startup Time [3]	$t_{SU(V5P2)}$	C_{V5P2} ≤ 2.9 µF, R_{Load} = 100 Ω ±5% (50 mA)	●	–	–	1	ms

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
3V3 LINEAR REGULATOR							
3V3 Accuracy and Load Regulation	V_{3V3}	10 mA < I_{3V3} < 150 mA, V_{VREG} = 5.25 V	●	3.23	3.3	3.37	V
3V3 Dropout 1	$V_{3V3(DO)1}$	T_J = –40°C, V_{VIN} = 3.5 V, I_{V5} = 230 mA, I_{V5P1} =10 mA, I_{V5P2} = 10 mA , I_{3V3} = 50 mA, I_{1V2x} = 800 mA		$V_{3V3(UV,L)max}$	–	–	V
3V3 Dropout 2	$V_{3V3(DO)2}$	T_J = 150°C, V_{VIN} = 3.65V, I_{V5} = 230 mA, I_{V5P1} = 10 mA, I_{V5P2} = 10 mA , I_{3V3} = 50 mA, I_{1V2x} = 1200 mA		$V_{3V3(UV,L)max}$	–	–	V
3V3 Output Capacitance [3]	$C_{OUT(3V3)}$		●	1.0	–	22	µF
3V3 Current Limit [1]	$I_{LIM(3V3)}$	V_{3V3} = 3.3 V	●	–165	–235	–	mA
3V3 Foldback Current [1]	$I_{FBK(3V3)}$	V_{3V3} = 0 V	●	–30	–60	–90	mA
3V3 Startup Time [3]	$t_{SU(3V3)}$	C_{3V3} ≤ 2.9 µF, R_{Load} = 22 Ω ±5% (150 mA)	●	–	–	1	ms
IGNITION ENABLE (ENBAT) INPUT							
ENBAT Threshold	$V_{ENBAT(H)}$	V_{ENBAT} rising	●	–	2.8	3.0	V
	$V_{ENBAT(L)}$	V_{ENBAT} falling	●	1.7	2.1	–	V
ENBAT Hysteresis	$V_{ENBAT(HYS)}$	$V_{ENBAT(H)}$ – $V_{ENBAT(L)}$	●	–	700	–	mV
ENBAT Bias Current	$I_{ENBAT(BIAS)}$	T_J = 25°C [3], V_{ENBAT} = 3.5 V		–	28	45	uA
		T_J = 150°C, V_{ENBAT} = 3.5 V		–	35	55	µA
ENBAT Resistance	R_{ENBAT}	V_{ENBAT} < 1.2 V	●	200	650	900	kΩ
LOGIC ENABLE (ENB) INPUT							
ENB Thresholds	$V_{ENB(H)}$	V_{ENB} rising	●	–	–	2.0	V
	$V_{ENB(L)}$	V_{ENB} falling	●	0.8	–	–	V
ENB Bias Current	$I_{ENB(BIAS)}$	V_{ENB} = 3.3 V	●	–	–	175	µA
ENB Resistance	R_{ENB}	V_{ENB} = 0.8 V	●	25	35	50	kΩ
ENB/ENBAT/VIGN-IN FILTER/DEGLITCH							
Enable Filter/Deglitch Time	$t_{dEN(FILT)}$		●	–	30	40	µs
ENB/ENBAT/VIGN-IN SHUTDOWN DELAY							
Regulator (1V2x) Shutdown delay	$t_{dREG(OFF)}$	Period from NPOR is low (when ENB, ENBAT, and VIGN-IN are low) to COMP2 begins to decay (see Figure 4)	●	5	15	30	µs

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
NPOR OV/UV PROTECTION THRESHOLDS							
V5 OV Thresholds	$V_{V5(OV,H)}$	V_{V5} rising	●	5.15	5.33	5.50	V
	$V_{V5(OV,L)}$	V_{V5} falling	●	–	5.30	–	V
V5 OV Hysteresis	$V_{V5(OV,HYS)}$	$V_{V5(OV,H)} – V_{V5(OV,L)}$	●	15	30	50	mV
V5 UV Thresholds	$V_{V5(UV,H)}$	V_{V5} rising	●	–	4.68	–	V
	$V_{V5(UV,L)}$	V_{V5} falling	●	3.00	3.13	3.27	V
V5Px Output Disconnect Threshold	$V_{V5Px(DISC)}$	V_{V5Px} rising, turning off disconnect FET	●	–	6.5	–	V
V5Px OV Thresholds	$V_{V5Px(OV,H)}$	V_{V5Px} rising	●	5.15	5.33	5.50	V
	$V_{V5Px(OV,L)}$	V_{V5Px} falling	●	–	5.30	–	V
V5Px OV Hysteresis	$V_{V5Px(OV,HYS)}$	$V_{V5Px(OV,H)} – V_{V5Px(OV,L)}$	●	15	30	50	mV
V5Px UV Thresholds	$V_{V5Px(UV,H)}$	V_{V5Px} rising	●	–	4.68	–	V
	$V_{V5Px(UV,L)}$	V_{V5Px} falling	●	3.00	3.13	3.27	V
3V3 OV Thresholds	$V_{3V3(OV,H)}$	V_{3V3} rising	●	3.41	3.52	3.60	V
	$V_{3V3(OV,L)}$	V_{3V3} falling	●	–	3.48	–	V
3V3 OV Hysteresis	$V_{3V3(OV,HYS)}$	$V_{3V3(OV,H)} – V_{3V3(OV,L)}$	●	25	35	50	mV
3V3 UV Thresholds	$V_{3V3(UV,H)}$	V_{3V3} rising	●	–	3.12	–	V
	$V_{3V3(UV,L)}$	V_{3V3} falling	●	3.0	3.07	3.17	V
3V3 UV Hysteresis	$V_{3V3(UV,HYS)}$	$V_{3V3(UV,H)} – V_{3V3(UV,L)}$	●	40	50	60	mV
1V2x OV Thresholds (ARG81403)	$V_{1V2x(OV,H)}$	V_{1V2x} rising	●	1.316	1.35	1.377	V
	$V_{1V2x(OV,L)}$	V_{1V2x} falling	●	1.31	1.33	1.36	V
1V2x OV Hysteresis (ARG81403)	$V_{1V2x(OV,HYS)}$	$V_{1V2x(OV,H)} – V_{1V2x(OV,L)}$	●	–	17	–	mV
1V2x UV Thresholds (ARG81403)	$V_{1V2x(UV,H)}$	V_{1V2x} rising	●	1.19	1.22	1.24	V
	$V_{1V2x(UV,L)}$	V_{1V2x} falling	●	1.173	1.20	1.234	V
1V2x UV Hysteresis (ARG81403)	$V_{1V2x(UV,HYS)}$	$V_{1V2x(UV,H)} – V_{1V2x(UV,L)}$	●	–	17	–	mV
1V2x OV Thresholds (ARG81403-1)	$V_{1V2x(OV,H)}$	V_{1V2x} rising	●	1.29	1.32	1.35	V
	$V_{1V2x(OV,L)}$	V_{1V2x} falling	●	1.28	1.30	1.32	V
1V2x OV Hysteresis (ARG81403-1)	$V_{1V2x(OV,HYS)}$	$V_{1V2x(OV,H)} – V_{1V2x(OV,L)}$	●	–	17	–	mV
1V2x UV Thresholds (ARG81403-1)	$V_{1V2x(UV,H)}$	V_{1V2x} rising	●	1.17	1.20	1.22	V
	$V_{1V2x(UV,L)}$	V_{1V2x} falling	●	1.15	1.18	1.21	V
1V2x UV Hysteresis (ARG81403-1)	$V_{1V2x(UV,HYS)}$	$V_{1V2x(UV,H)} – V_{1V2x(UV,L)}$	●	–	17	–	mV

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
OVERVOLTAGE (OV) DETECTION FILTERING TIME							
Overvoltage Detection Filtering Time	t_{dOV}	V5Px, 3V3, and 1V2x overvoltage detection filtering time (OV detection is masked during this period)	●	5	15	25	µs
Overvoltage Detection Filtering Time, V5 Rising	$t_{dOV(V5R)}$	V5 overvoltage detection filtering time at V5 rising (OV detection is masked during this period)	●	0.7	1	1.3	ms
Overvoltage Detection Filtering Time, V5 Falling	$t_{dOV(V5F)}$	V5 overvoltage detection filtering time at V5 falling (OV detection is masked during this period)	●	5	15	25	µs
NPOR TURN-ON DELAY							
NPOR Turn-On Delay	$t_{dNPOR(ON)}$		●	12	15	18	ms
NPOR OUTPUT							
NPOR Output Low Voltage	$V_{NPOR(L)}$	I_{NPOR} = 4 mA	●	–	150	400	mV
NPOR Leakage Current [1]	$I_{NPOR(LKG)}$	V_{NPOR} = 3.3 V	●	–	–	2	µA
UNDERVOLTAGE (UV) FILTERING TIME							
Undervoltage Detection Filtering Time	t_{dFILT}	V5Px, V5, 3V3, and 1V2x undervoltage detection filtering time (UV detection is masked during this period)	●	5	–	25	µs
POK5V UV PROTECTION THRESHOLDS							
V5-POK5V Rising Thresholds	$V_{V5(POK,H)}$	V_{V5} rising	●	–	4.75	–	V
V5-POK5V Falling Thresholds	$V_{V5(POK,L)}$	V_{V5} falling	●	4.50	4.65	4.80	V
POK5V OUTPUT							
POK5V Output Voltage	$V_{POK5V(L)}$	I_{POK5V} = 4 mA	●	–	150	400	mV
POK5V Leakage Current	$I_{POK5V(LKG)}$	V_{POK5V} = 3.3 V	●	–	–	2	µA
FFN OUTPUT							
FFn Output Voltage	$V_{FFn(L)}$	I_{FFn} = 4 mA	●	–	150	400	mV
FFn Leakage Current	$I_{FFn(LKG)}$	V_{FFn} = 3.3 V	●	–	–	2	µA
VIN 2ND UV DETECTION THRESHOLDS							
VIN 2nd UV Thresholds	$V_{VIN(UV2,L)}$	V_{VIN} falling, set “VIN_2nd _UV” bit “1” See “VIN 2nd UV DETECTION in Functional Description”	●	5.3	5.6	5.9	V
THERMAL PROTECTION							
Thermal Shutdown Threshold [3]	T_{TSD}	T_J rising		165	–	–	°C
Thermal Shutdown Hysteresis [3]	T_{HYS}			–	15	–	°C

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
VREG, VCP, AND BG THRESHOLDS							
VREG OV Thresholds	$V_{VREG(OV,H)}$	V_{VREG} rising, LX1 PWM disabled	●	5.48	5.65	5.90	V
	$V_{VREG(OV,L)}$	V_{VREG} falling, LX1 PWM enabled	●	–	5.55	–	V
VREG OV Hysteresis	$V_{REG(OV,HYS)}$	$V_{VREG(OV,H)}$ – $V_{VREG(OV,L)}$	●	–	100	–	mV
VREG UV Thresholds	$V_{VREG(UV,H)}$	V_{VREG} rising	●	4.14	4.38	4.62	V
	$V_{VREG(UV,L)}$	V_{VREG} falling	●	–	3.2	–	V
VREG UV Hysteresis	$V_{VREG(UV,HYS)}$	$V_{VREG(UV,H)}$ – $V_{VREG(UV,L)}$	●	–	1.2	–	V
VCP OV Thresholds	$V_{VCP(OV,H)}$	V_{VCP} rising	●	11.0	12.5	14.0	V
VCP UV Thresholds	$V_{VCP(UV,H)}$	V_{VCP} rising, PWM enabled	●	–	4.3	–	V
	$V_{VCP(UV,L)}$	V_{VCP} falling, PWM disabled	●	–	2.8	–	V
VCP UV Hysteresis	$V_{VCP(UV,HYS)}$	$V_{VCP(UV,H)}$ – $V_{VCP(UV,L)}$	●	–	1.4	–	V
BGREF and BGFAULT UV Thresholds [3]	$V_{BGx(UV)}$	V_{BGVREF} or $V_{BGFAULT}$ rising	●	1.00	1.05	1.10	V
VCC UV Thresholds [3]	$V_{VCC(UV, H)}$	V_{VCC} rising	●	2.9	3.05	3.2	V
	$V_{VCC(UV, L)}$	V_{VCC} falling	●	2.6	2.8	3	V
VCC OV Thresholds [3]	$V_{VCC(OV, H)}$	V_{VCC} rising	●	5.1	5.3	5.5	V
	$V_{VCC(OV, L)}$	V_{VCC} falling	●	4.7	4.95	5.2	V

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
WD ENABLE / INPUT (WDENn)							
WDENn Voltage Thresholds	$V_{WDENn(LO)}$	V_{WDENn} falling, WDT enabled	●	0.8	–	–	V
	$V_{WDENn(HI)}$	V_{WDENn} rising, WDT disabled	●	–	–	2.0	V
WDENn Input Resistance	$R_{WD(ENn)}$		●	–	60	–	kΩ
WDIN VOLTAGE THRESHOLDS AND CURRENT							
WDIN Input Voltage Thresholds	$V_{WDIN(LO)}$	V_{WDIN} falling	●	0.8	–	–	V
	$V_{WDIN(HI)}$	V_{WDIN} rising	●	–	–	2.0	V
WDIN Input Current [1]	I_{WDIN}	V_{WDIN} = 5 V	●	−10	–	10	µA
WDIN TIMING SPECIFICATION							
Watchdog Activation Delay (Startup)	$t_{dWD(START)}$		●	120	140	160	ms
Watchdog Activation Delay (Operation)	$t_{dWD(OP)}$		●	–	64	–	ms
WD ONE-SHOT TIME							
WD Pulse Time after WD Fault	$t_{WD(FAULT)}$		●	1.6	2.0	2.4	ms

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[3] Ensured by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 6 V ≤ V_{VIN} / V_{SNSVIN} ≤ 36 V, T_J = 25°C; ● indicates specifications guaranteed –40°C ≤ T_J ≤ 150°C, ENB = High or ENBAT = High or VIGN-IN = High, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
ROTATIONAL SENSOR: VOLTAGE DROP OF HIGH / LOW-SIDE SWITCH							
Voltage Drop, High-Side Switch	$V_{DROP(H-SW)}$	V_{SNSVIN} – V_{SNSxP}, I_{SNSxP} = 20 mA,	●	–	–	280	mV
Voltage Drop, Low-Side Switch	$V_{DROP(L-SW)}$	V_{SNSxN} – V_{SNSxR}, I_{SNSxN} = 20 mA	●	–	–	50	mV
ROTATIONAL SENSOR: REFERENCE VOLTAGE							
SNSxFB Reference High Threshold	$V_{REF(SNSxFB,H)}$		●	1.04	1.1	1.16	V
SNSxFB Reference Low Threshold	$V_{REF(SNSxFB,L)}$		●	0.83	0.9	0.95	V
SNSxFB Reference Hysteresis	$V_{REF(SNSxFB,HYS)}$		●	–	0.2	–	V
ROTATIONAL SENSOR: LEAKAGE CURRENT							
SNSxFB Leakage Current	I_{SNSxFB}	V_{SNSxFB} = 2 V	●	–	–	1	µA
ROTATIONAL SENSOR: OUTPUT VOLTAGE / DELAY TIME							
SNSxO Output High Voltage	$V_{SNSxO(H)}$	V_{V5} = 5 V, V_{SNSxFB} = 2 V, I_{SNSxO} = 200 µA	●	4.5	4.9	–	V
SNSxO Output Low Voltage	$V_{SNSxO(L)}$	V_{V5} = 5 V, V_{SNSxFB} = 0 V, I_{SNSxO} = 200 µA	●	–	0.4	0.8	V
SNSxO response time	$t_{SNSxO(RES)}$	V_{V5} = 5 V; from SNSxFB input rising above $V_{REF(SNSxFB,H)}$ to SNSxO output rising (10%); from SNSxFB input falling below $V_{REF(SNSxFB,H)}$ to SNSxO output falling (90%); SNSxFB input overdrive = 0.8 V; input capacitance of MCU = 10 pF; see Figure 1	●	–	–	2	µs
SNSxO rise time	$t_{SNSxO(RISE)}$	Output rising from 10% to 90% SNSxFB input overdrive = 0.8 V, input capacitance of MCU = 10 pF; see Figure 1	●	–	–	1	µs
SNSxO fall time	$t_{SNSxO(RISE)}$	Output falling from 90% to 10% SNSxFB input overdrive = 0.8 V, input capacitance of MCU = 10 pF; see Figure 1	●	–	–	1	µs

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[2] Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
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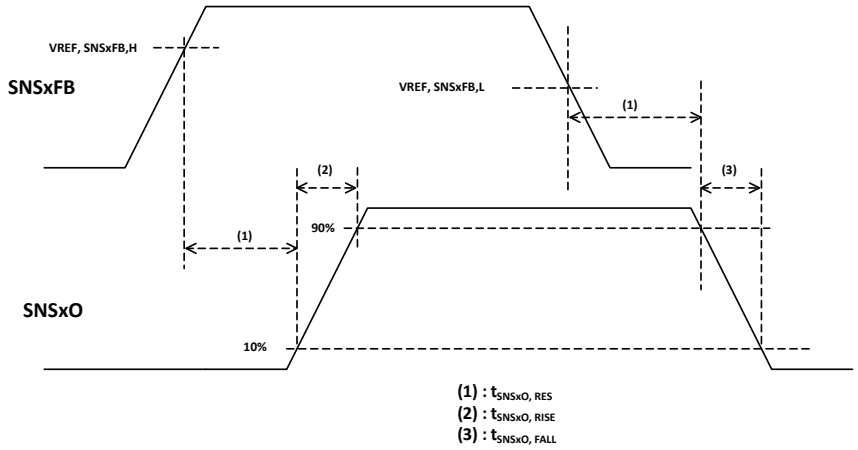

Figure 1: Rotational Sensor Response, Rising and Falling Time

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
ROTATIONAL SENSOR OVERVOLTAGE PROTECTION							
SNSxP OV Threshold	$V_{SNSxP(OV,H)}$	Rising, Monitoring SNSxP to GND, high-side SW disabled (non-latch)	●	21	22	23	V
	$V_{SNSxP(OV,L)}$	Falling, Monitoring SNSxP to GND, high-side SW enabled	●	18	19	20	V
SNSxP OV Detection Delay [3]	$t_{dSNS-OV}$		●	–	8	–	µs
ROTATIONAL SENSOR OVERCURRENT PROTECTION							
SNSxP High-Side SW Current Limit	$I_{LIM\ (SNSxP)}$	Increasing, Monitoring SNSVIN to SNSxP, high-side SW operation is hiccup (non-latch)	●	–75	–50	–25	mA
SNSxN Low-Side SW Current Limit	$I_{LIM\ (SNSxN)}$	Increasing, Monitoring SNSxN to SNSxR, low-side SW operation is hiccup (non-latch), resistor (SNSxR to GND) = 100 Ω	●	25	50	75	mA
SNSVIN							
SNSVIN Quiescent Current [1]	$I_{Q(SNSVIN)}$	V_{SNSVIN} = 13.5 V	●	–	–	10	mA
SNSXR							
SNSxR Leakage Current [3]	I_{SNSxR}	V_{SNSxR} = 2 V	●	–	–	0.1	µA
LEVEL SHIFTERS INPUT THRESHOLDS							
LSINx High Threshold	$V_{LSINx(H)}$		●	–	0.6 × V_{SNSVIN}	0.7 × V_{SNSVIN}	V
LSINx Low Threshold	$V_{LSINx(L)}$		●	0.33 × V_{SNSVIN}	0.4 × V_{SNSVIN}	–	V
LSINx Hysteresis	$V_{LSINx(HYS)}$		●	0.1 × V_{SNSVIN}	0.2 × V_{SNSVIN}	–	V
LSINx Bias Current	$I_{B-LSINx}$		●	–	–	10	µA
LEVEL SHIFTERS OUTPUT VOLTAGE / DELAY TIME							
LSOUTx High	$V_{LSOUTx(H)}$	V_{V5} = 5 V, I_{LSOUTx} = 100 µA	●	4.6	–	–	V
LSOUTx Low	$V_{LSOUTx(L)}$	V_{V5} = 5 V, I_{LSOUTx} = 100 µA	●	–	–	0.4	V
LSOUTx Delay time	$t_{LSOUTx(DLY)}$	High to Low / Low to High	●	–	–	3	µs
VIGN INPUT THRESHOLDS							
VIGN-IN High Threshold	$V_{IGN-IN(H)}$	V_{IGN-IN} rising	●	–	2.8	3.0	V
VIGN-IN Low Threshold	$V_{IGN-IN(L)}$	V_{IGN-IN} falling	●	1.7	2.1	–	V
VIGN-IN Hysteresis	$V_{IGN-IN\ (HYS)}$	$V_{IGN-IN(H)}$ – $V_{IGN-IN(L)}$	●	–	700	–	mV
VIGN-IN Bias Current	$I_{IGN-IN\ (BIAS)}$	T_J = 25°C [3], V_{IGN-IN} = 3.5 V		–	28	45	µA
		T_J = 150°C, V_{IGN-IN} = 3.5 V		–	35	55	µA
VIGN-IN Resistance	R_{IGN-IN}	V_{IGN-IN} < 1.2 V	●	200	650	900	kΩ
VIGN OUTPUT VOLTAGE/ DELAY TIME							
VIGN-OUT High	$V_{IGN-OUT(H)}$	V_{V5} = 5 V, $I_{IGN-OUT}$ = 100 µA	●	4.6	–	–	V
VIGN-OUT Low	$V_{IGN-OUT(L)}$	V_{V5} = 5 V, $I_{IGN-OUT}$ = 100 µA	●	–	–	0.4	V
VIGN-OUT Delay Time	$t_{dIGN-OUT}$	From VIGN-IN input rising above $V_{IGN-OUT(H)}$ + 0.8 V overdrive to VIGN-OUT output rising (10%). From VIGN-IN input falling below $V_{IGN-OUT(L)}$ – 0.8 V to VIGN-OUT output falling (90%)	●	–	–	3	µs

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
SERIAL INTERFACE (STRn, SDI, SDO, SCK)							
Input Low Voltage	V_{IL}		●	–	–	0.8	V
Input High Voltage	V_{IH}	All logic inputs	●	2.0	–	–	V
Input Hysteresis	V_{Ihys}	All logic inputs	●	250	550	–	mV
Input Pull-Down SDI, SCK	R_{PDS}	0 V < V_{INPUT} < 5 V	●	–	50	–	kΩ
Input Pull-Up To VCC	I_{PU}	STRn	●	–	50	–	kΩ
Output Low Voltage	V_{OL}	I_{OL} = 1 mA [1]	●	–	–	0.3	V
Output High Voltage	V_{OH}	I_{OL} = 1 mA [1], V_{V5} = 5 V	●	4.5 (V_{V5} – 0.5 V)	–	–	V
Clock High Time	t_{SCKH}	A in Figure 2	●	50	–	–	ns
Clock Low Time	t_{SCKL}	B in Figure 2	●	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in Figure 2	●	30	–	–	ns
Strobe Lag Time	t_{STLG}	D in Figure 2	●	30	–	–	ns
Strobe High Time	t_{STRH}	E in Figure 2	●	300	–	–	ns
Data Out Enable Time [3]	t_{SDOE}	F in Figure 2	●	–	–	40	ns
Data Out Disable Time [3]	t_{SDOD}	G in Figure 2	●	–	–	30	ns
Data Out Valid Time From Clock Falling [3]	t_{SDOV}	H in Figure 2	●	–	–	40	ns
Data Out Hold Time From Clock Falling [3]	t_{SDOH}	J in Figure 2	●	5	–	–	ns
Data In Setup Time To Clock Rising	t_{SDIS}	K in Figure 2	●	15	–	–	ns
Data In Hold Time From Clock Rising	t_{SDIH}	L in Figure 2	●	10	–	–	ns

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
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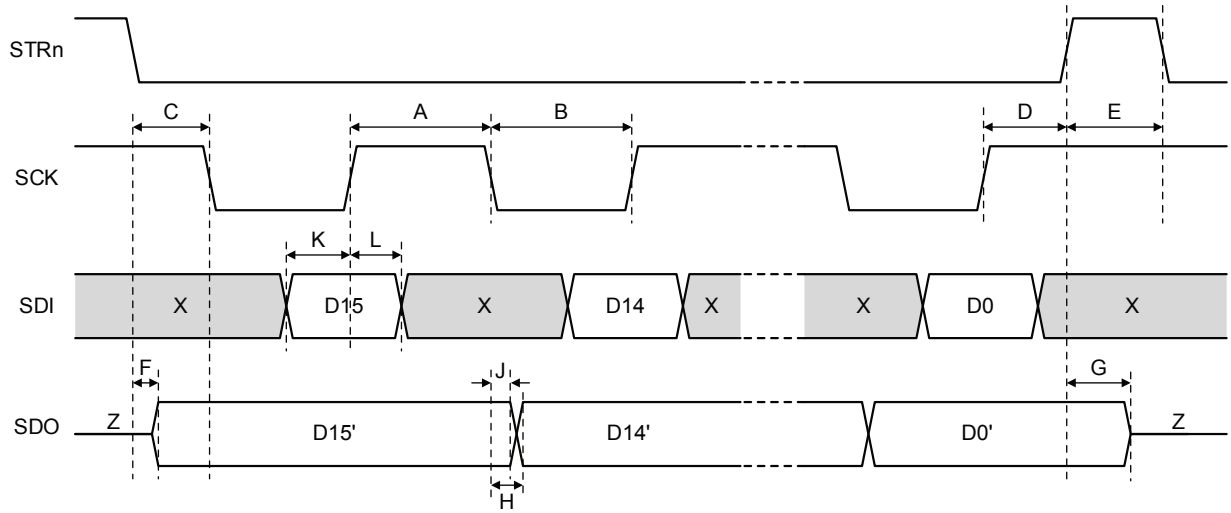

Figure 2: Serial Interface Timing
X = don't exceed WD Config timeout, Z = high impedance (tri-state)

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Table 1: Summary of Fault Mode Operation

Fault Type and Condition	ARG81403 Response to Fault	NPOR	FFn	POK5V	V5, 3V3, 1V2x	V5Px	Reset Method
LATCHING FAULTS							
LX1 Shorted to Ground	If high-side MOSFET current exceeding $I_{LIM(LX1)}$ results in MPOR [1], then all regulators are turned off.	Low	Low	Low	Off	Off	Remove short, then cycle EN or VIN
NON-LATCHING FAULTS							
V5P1 Short to VBAT (> 6.5 V_{typ})	V5P1 disconnect occurs.	No effect	Low	No effect	No effect	V5P1: Turning OFF disconnect FET V5P2: No effect	Check for short circuits on V5P1
V5P2 Short to VBAT (> 6.5 V_{typ})	V5P2 disconnect occurs.	No effect	Low	No effect	No effect	V5P1: No effect V5P2: Turning OFF disconnect FET	Check for short circuits on V5P2
V5P1 Overvoltage	If OV condition persists for more than t_{dOV}, then set FFn low.	No effect	Low	No effect	No effect	V5P2: No effect	Check for short circuits on V5P1
V5P2 Overvoltage	If OV condition persists for more than t_{dOV}, then set FFn low.	No effect	Low	No effect	No effect	V5P1: No effect	Check for short circuits on V5P2
V5P1 Overcurrent	Foldback current limit will reduce output voltage.	No effect	Low if $V_{V5P1} < V_{V5Px(UV,L)}$	No effect	No effect	V5P2: No effect	Remove short circuit or decrease load
V5P2 Overcurrent	Foldback current limit will reduce output voltage.	No effect	Low if $V_{V5P2} < V_{V5Px(UV,L)}$	No effect	No effect	V5P1: No effect	Remove short circuit or decrease load
V5P1 Undervoltage	Closed-loop control will try to raise voltage, but may be constrained by foldback current limit.	No effect	Low	No effect	No effect	V5P2: No effect	Remove short circuit or decrease load
V5P2 Undervoltage	Closed-loop control will try to raise voltage, but may be constrained by foldback current limit.	No effect	Low	No effect	No effect	V5P1: No effect	Remove the short circuit or decrease the load
V5 Overvoltage	If OV condition persists for more than t_{dOV}, then set NPOR and FFn low.	Low	Low	No effect	3V3: No effect 1V2x: No effect	Track to V5	Check for short circuits on V5
V5 Overcurrent	Foldback current limit will reduce output voltage.	Low if $V_{V5} < V_{V5(UV,L)}$	Low if $V_{V5} < V_{V5(UV,L)}$	Low if $V_{V5} < V_{V5(POK,L)}$	3V3: No effect 1V2x: No effect	Track to V5	Remove short circuit or decrease load
V5 Undervoltage $V_{V5} > V_{V5(UV,L)}$	Closed-loop control will try to raise voltage, but may be constrained by foldback current limit.	No effect	No effect	Low if $V_{V5} < V_{V5(POK,L)}$	3V3: No effect 1V2x: No effect	Track to V5	Remove short circuit or decrease load
V5 Undervoltage $V_{V5} < V_{V5(UV,L)}$	Closed-loop control will try to raise voltage, but may be constrained by foldback current limit.	Low	Low	Low	3V3: No effect 1V2x: No effect	Track to V5	Remove short circuit or decrease load
3V3 Overvoltage	If OV condition persists for more than t_{dOV}, then set NPOR and FFn low.	Low	Low	No effect	V5: No effect 1V2x: No effect	No effect	Check for short circuits on 3V3
3V3 Overcurrent	Foldback current limit will reduce output voltage.	Low if $V_{3V3} < V_{3V3(UV,L)}$	Low if $V_{3V3} < V_{3V3(UV,L)}$	No effect	V5: No effect 1V2x: No effect	No effect	Remove short circuit or decrease load
3V3 Undervoltage	Closed-loop control will try to raise voltage, but may be constrained by foldback current limit.	Low	Low	No effect	V5: No effect 1V2x: No effect	No effect	Remove short circuit or decrease load
1V2x Overvoltage	If OV condition persists for more than t_{dOV}, then set NPOR and FFn low.	Low	Low	No effect	V5: No effect 3V3: No effect	No effect	Check for short circuits on 1V2x
1V2x Overcurrent	Foldback current limit will reduce output voltage.	Low if $V_{1V2x} < V_{1V2x(UV,L)}$	Low if $V_{1V2x} < V_{1V2x(UV,L)}$	No effect	V5: No effect 3V3: No effect	No effect	Remove short circuit or decrease load
1V2x Undervoltage	Closed-loop control will try to raise voltage, but may be constrained by foldback current limit.	Low	Low	No effect	V5: No effect 3V3: No effect	No effect	Remove short circuit or decrease load
1V2x Pin Open Circuit	1V2x pin will be pulled high by internal current source, COMP2 will respond by going low, LX2 will operate at zero cycle, and synchronous buck output ≈ 0 V.	Low	Low	No effect	V5: No effect 3V3: No effect	No effect	Repair open circuit, check 1V2x circuitry
1V2x Output Shorted to Ground, V_{1V2x} < 450 mV (during soft-start)	Continues to PWM, but turns off LX2 when high-side MOSFET current exceeds $I_{LIM2(ton,min)H}$.	Low	Low	Low (V5 could not wake up)	V5: No effect 3V3: No effect	No effect	Remove short circuit
1V2x Output Overcurrent, V_{1V2x} < 450 mV	Enters hiccup mode after 30 OCP faults.	Low	Low	No effect	V5: No effect 3V3: No effect	No effect	Decrease the load
1V2x output Overcurrent, V_{1V2x} > 450 mV	Enters hiccup mode after 120 OCP faults.	Low if $V_{1V2x} < V_{1V2x(UV,L)}$	Low	No effect	V5: No effect 3V3: No effect	No effect	Decrease the load
LX2 Shorted to Ground	If high- side MOSFET current exceeding $I_{LIM2(ton,min)H}$, 1V2x regulator is turned off.	Low if $V_{1V2x} < V_{1V2x(UV,L)}$	Low	No effect	V5: No effect 3V3: No effect	No effect	Remove short circuit
VREG Pin Open Circuit	V_{VREG} will decay to 0 V; LX1 will switch at maximum duty cycle so the voltage on the output capacitors will be very close to V_{VIN}.	Low if V5, 3V3, or 1V2x detects UV	Low if VREG, V5, 3V3, or 1V2x detects UV	Low if $V_{V5} < V_{V5(POK,L)}$	Decay to 0 V due to no VREG input	Decay to 0 V due to no VREG input	Connect VREG pin

[1] MPOR: Master Power-On Reset.

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Table 1: Summary of Fault Mode Operation (continued)

Fault Type and Condition	ARG81403 Response to Fault	NPOR	FFn	POK5V	V5, 3V3, 1V2x	V5Px	Reset Method
VREG Overcurrent V_{VREG} < 1.3 V, $V_{COMP1} = V_{EA1(VO,MAX)}$	Enters hiccup mode after 30 OCP faults.	Low if V5, 3V3, or 1V2x detects UV)	Low if VREG, V5, 3V3, or 1V2x detects UV	Low if $V_{V5} < V_{V5(POK,L)}$	Decay	Decay	Decrease load
VREG Overcurrent V_{VREG} > 1.3 V, $V_{COMP1} = V_{EA1(VO,MAX)}$	Enters hiccup mode after 120 OCP faults.	Low if V5, 3V3, or 1V2x detects UV)	Low if VREG, V5, 3V3, or 1V2x detects UV	Low if $V_{V5} < V_{V5(POK,L)}$	May decay depending on VREG voltage	May decay depending on VREG voltage	Decrease load
VREG Overvoltage $V_{VREG} > V_{VREG(OV,H)}$	Temporarily stop PWM switching of LX1.	No effect	Low	No effect	No effect	No effect	Check for short circuits on VREG
VREG Undervoltage $V_{VREG} > V_{VREG(UV,L)}$	Closed-loop control will try to raise voltage, but may be constrained by foldback current limit.	Low if V5, 3V3, or 1V2x detects UV)	Low	Low if $V_{V5} < V_{V5(POK,L)}$	May decay depending on VREG voltage	May decay depending on VREG voltage	Remove short circuit or decrease load
Charge Pump (VCP) Overvoltage	Results in MPOR [1], so all regulators are off.	Low	Low	Low	OFF	OFF	Check VCP/CP1/ CP2
Charge Pump (VCP) Overcurrent	Results in VCP-UV and MPOR [1], so all regulators are off.	Low	Low	Low	OFF	OFF	Check VCP/CP1/ CP2
Charge Pump (VCP) Undervoltage	Results in MPOR [1], so all regulators are off.	Low	Low	Low	OFF	OFF	Check VCP/CP1/ CP2
VCP Pin Open Circuit	Results in VCP-UV and MPOR [1], so all regulators are off.	Low	Low	Low	OFF	OFF	Connect the VCP pin or populate C_{CP}
VCP Pin Shorted to Ground	Results in high current from charge pump and (intentional) fusing of internal trace. Also results in MPOR [1], so all regulators are off.	Low	Low	Low	OFF	OFF	Remove short circuit and replace device
CP1 or CP2 Pin Open Circuit	Results in VCP-UV and MPOR [1], so all regulators are off.	Low	Low	Low	OFF	OFF	Connect the CP1 or CP2 pins
CP1 Pin Shorted to Ground	Results in VCP-UV and MPOR [1], so all regulators are off.	Low	Low	Low	OFF	OFF	Remove short circuit
CP2 Pin Shorted to Ground	Results in high current from charge pump and (intentional) fusing of internal trace. Also results in MPOR [1], so all regulators are off.	Low	Low	Low	OFF	OFF	Remove short circuit and replace device
BG_{VREF} or BG_{FAULT} Undervoltage	Results in MPOR [1], so all regulators are off.	Low	Low	Low	OFF	OFF	Raise VIN or wait for BGs to power up
BG_{VREF} Overvoltage	If BG_{VREF} is too high, all regulators will appear to be OV (because BGFAULT is good).	Low	Low	Low	OV	OV	Replace the device
BG_{FAULT} Overvoltage	If BG_{FAULT} is too high, all regulators will appear to be UV (because BGVREF is good).	Low	Low	Low	UV	UV	Replace the device
VCC Undervoltage or Shorted to Ground	Results in MPOR [1], so all regulators are off.	Low	Low	Low	OFF	OFF	Raise VIN or remove short from VCC pin
VCC Overvoltage	Set FFn Low.	No effect	Low	No effect	No effect	No effect	Replace the device
Thermal Shutdown	Results in MPOR [1], so all regulators are off.	Low	Low	Low	OFF	OFF	Let the device cool
Rotational Sensor SNSxP High-Side SW Current Limit	Respective channel results in foldback current limit.	No effect	Low	No effect	No effect	No effect	Remove short circuit
Rotational Sensor SNSxN Low-Side SW Current Limit	Respective channel results in foldback current limit.	No effect	Low	No effect	No effect	No effect	Remove short circuit
Rotational Sensor SNSxP Overvoltage	Respective high-side SW will be disabled.	No effect	Low	No effect	No effect	No effect	Remove short circuit
Internal Clock (8 MHz) Stuck High	Set FFn Low.	No effect	Low	No effect	No effect	No effect	Replace the device
Internal Clock (8 MHz) Stuck Low	Set FFn Low.	No effect	Low	No effect	No effect	No effect	Replace the device
Internal Clock (1 MHz) Stuck High	Results in MPOR [1], so all regulators are off.	Low	Low	Low	OFF	OFF	Replace the device
Internal Clock (1 MHz) Stuck Low	Results in MPOR [1], so all regulators are off.	Low	Low	Low	OFF	OFF	Replace the device

[1] MPOR: Master Power-On Reset.

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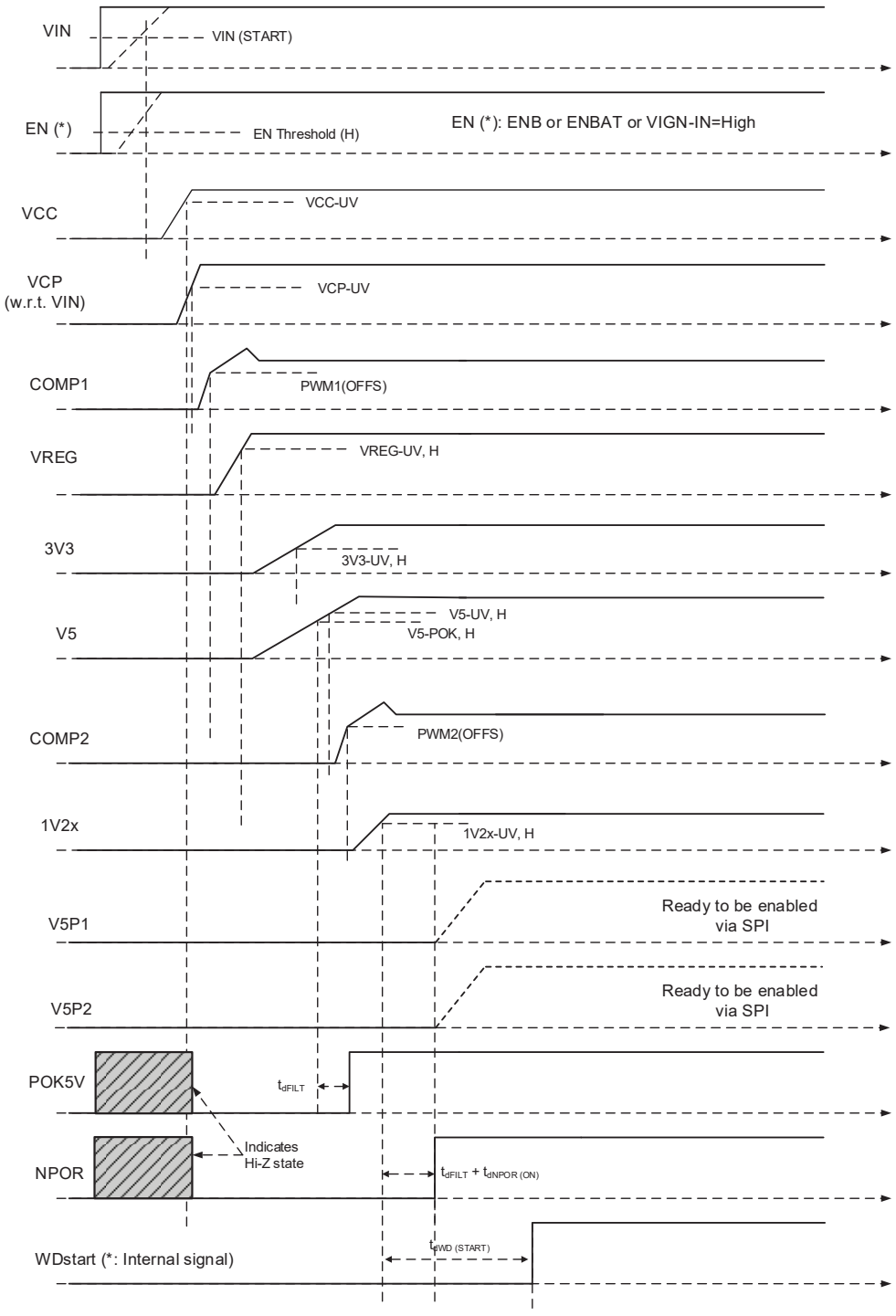

Figure 3: Startup Sequence

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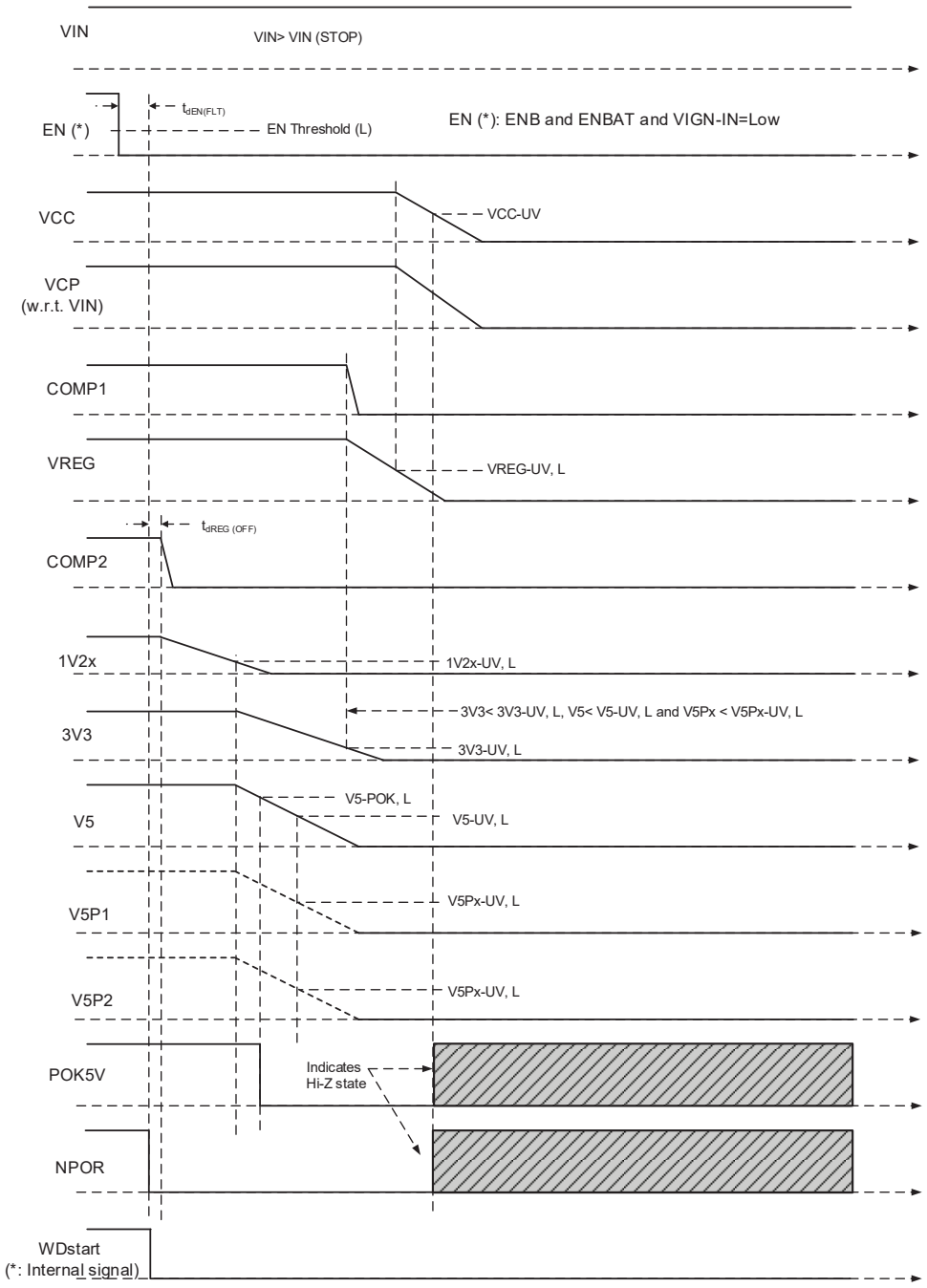

Time for outputs to drop to zero various for each output and depends on load current and capacitance.
Note: When shutting down by some fault (including VIN-UVLO), all regulators simultaneously start to decay.

Figure 4: Shutdown Sequence

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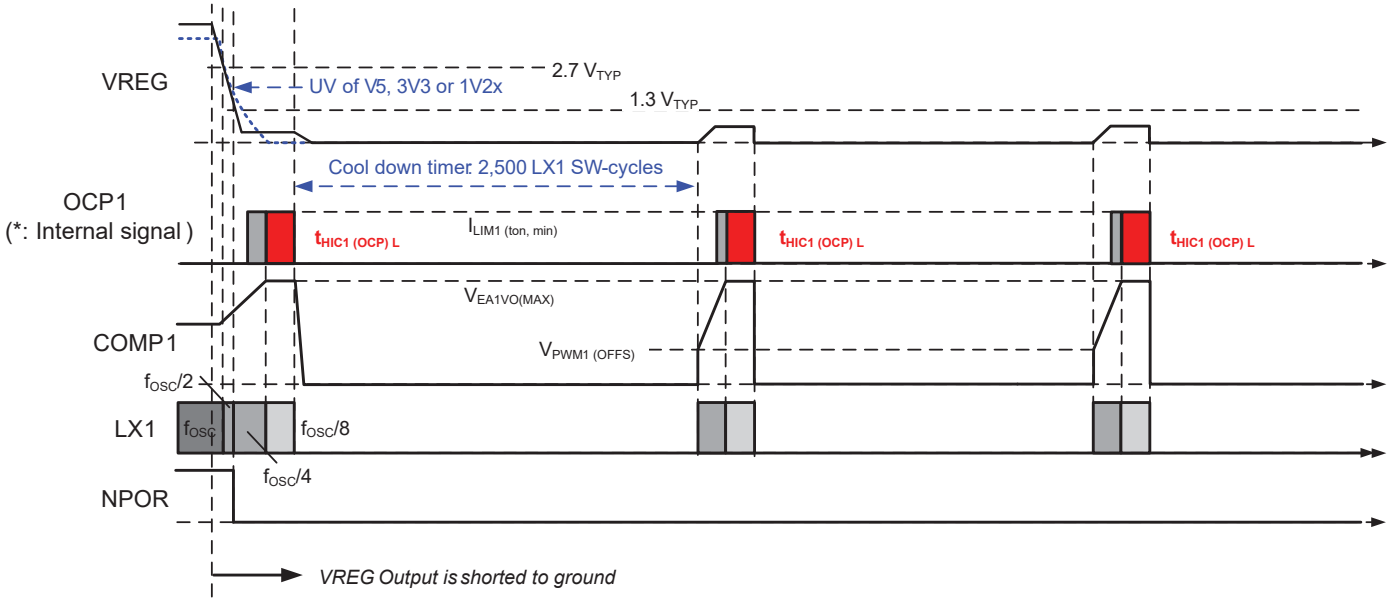

Figure 5: Hiccup Mode Operation when VREG output is shorted to GND

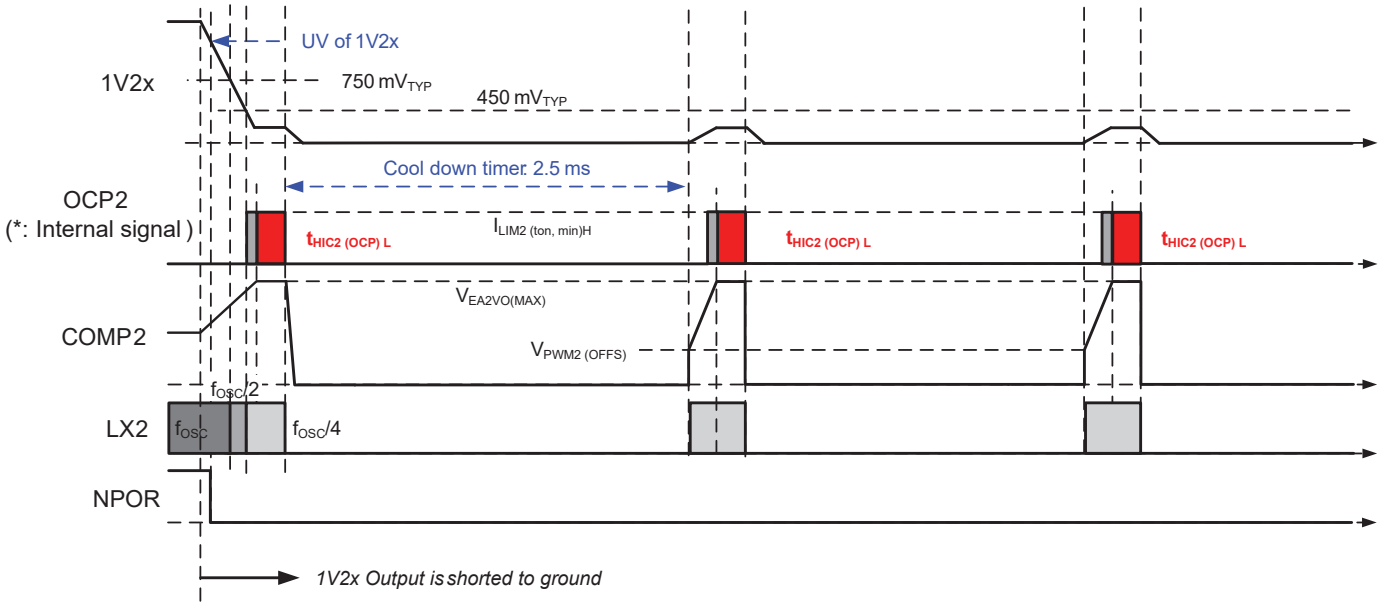

Figure 6: Hiccup Mode Operation when 1V2x output is shorted to GND

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FUNCTIONAL DESCRIPTION

Overview

The ARG81403 is a power management IC designed for safety-critical applications. It contains two switching and four linear regulators to create the voltages necessary for typical automotive applications such as automatic transmission.

The ARG81403 pre-regulator is a synchronous buck converter. This pre-regulator generates a fixed 5.35 V to power the internal post-regulators. These post-regulators generate the various voltage levels for the end system.

Pre-Regulator (VREG)

The pre-regulator incorporates internal high-side and low-side switches for buck configuration. An output LC filter is required to complete the buck converter.

The pre-regulator provides many protection and diagnostic functions:

1. Pulse-by-pulse and hiccup mode current limit
2. Undervoltage and overvoltage detection and reporting
3. Shorted switch node to ground
4. High voltage rating for load dump

Hiccup short-circuit protection will be enabled when V_{VREG} is less than 1.3 V_{TYP}; the number of overcurrent pulses (OCP) is limited to only 30. If V_{VREG} is greater than 1.3 V_{TYP}, the number of OCP pulses is increased to 120 to accommodate the possibility of starting into a relatively high output capacitance. The cooldown timer is 2500 switching cycles; at 2.2 MHz, this is around 1.14 ms.

PWM SWITCHING FREQUENCY

The switching frequency of the ARG81403 is fixed at 2.2 MHz nominal (f_{OSC}). The pre-regulator (VREG) includes a frequency foldback scheme shown in Table 2.

Table 2: EG PWM Frequency Foldback, VIN Threshold

VIN Rising	f_{osc}		VIN Falling
5.4 V	100% ON to $f_{OSC}/8$	$f_{OSC}/8$ to 100% ON	5.3 V
6.4 V	$f_{OSC}/8$ to $f_{OSC}/4$	$f_{OSC}/4$ to $f_{OSC}/8$	6.3 V
6.8 V	$f_{OSC}/4$ to $f_{OSC}/2$	$f_{OSC}/2$ to $f_{OSC}/4$	6.7 V
7.3 V	$f_{OSC}/2$ to f_{OSC}	f_{OSC} to $f_{OSC}/2$	7.1 V
17.2 V	f_{OSC} to $f_{OSC}/2$	$f_{OSC}/2$ to f_{OSC}	16.5 V

Bias Supply (VCC)

The bias supply (VCC) is generated by an internal linear regulator. This supply is the first rail to start up. Most of the internal control circuitry is powered by this supply. The bias supply includes some unique features to ensure safe operation of the ARG81403.

These features include:

1. Output over voltage detection and reporting
2. Dual input, VIN and VREG, for low battery voltage operation

Charge Pump (VCP)

A charge pump doubler provides the voltage necessary to drive high-side n-channel MOSFETs in the pre-regulator and the linear regulators. Two external capacitors are required for charge pump operation.

The charge pump incorporates some safety features:

1. Undervoltage and overvoltage detection and reporting
2. Overcurrent safe mode protection

Bandgap

Dual bandgaps are implemented within the ARG81403. One bandgap is dedicated to the voltage regulation loops within each of the regulators, VCC, VCP, VREG, 1V2x, V5 and 3V3. The second bandgap is dedicated to the monitoring function of all the regulators undervoltage and overvoltage. This improves safety coverage and fault reporting from the ARG81403.

Should the regulation bandgap fail, then the outputs will be out of specification and the monitoring bandgap will report the fault.

If the monitoring bandgap fails, the outputs will remain in regulation but the monitoring circuits will report the outputs as out of specification and trip the fault flag.

Enable Inputs (ENB, ENBAT, VIGN-IN)

Three enable pins are available on the ARG81403. A high signal on either of these pins enables the regulated outputs of the ARG81403. One (ENB) is logic-level compatible. The others (ENBAT and VIGN-IN) are battery-level rated and can be connected to the ignition switch through a resistor.

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Adjustable Synchronous Buck Post Regulator (1V2x)

The ARG81403 integrates the high-side and low-side MOSFETs necessary for implementing an adjustable output synchronous buck post-regulator. It is powered by the pre-regulator output. The synchronous buck is optimized for 1.275 V output (ARG81403) or 1.25 V (ARG81403-1) but can produce higher output voltages if a feedback resistor divider is inserted between the output voltage node and the 1V2x pin.

The synchronous buck requires an LC filter on its switch node to complete the regulation function.

Protection and safety functions provided by the synchronous buck include:

1. Pulse-by-pulse and hiccup mode current limit
2. Undervoltage and overvoltage detection and reporting
3. Shorted switch node to ground

Hiccup short-circuit protection will be enabled when V_{1V2x} is less than 450 mV_{TYP}; the number of overcurrent pulses (OCP) is limited to only 30. If V_{1V2x} is greater than 450 mV_{TYP}, the number of OCP pulses increases to 120 to accommodate the possibility of starting into a relatively high output capacitance. The cooldown timer is 2.5 ms.

Linear Regulators (V5, 3V3, V5P1, V5P2)

The ARG81403 has four linear regulators: one 5 V (V5), one 3.3 V (3V3) and two tracking/protected 5 V (V5P1/2).

All linear regulators provide the following protection features:

1. Current limit with foldback
2. Undervoltage and overvoltage detection and reporting

The tracking/protected regulators (V5P1 and V5P2) track V5 voltage and include protection against connection to the battery voltage. This makes these outputs most suitable for powering remote sensors or circuitry where short to battery is possible.

The pre-regulator powers these linear regulators which reduces power dissipation and temperature.

Fault Detection and Reporting

There is extensive fault detection within the ARG81403, as discussed previously. There are two fault reporting mechanisms used by the ARG81403: through hardwired pins and through a serial communications interface (SPI).

Two hardwired pins on the ARG81403 are used for fault reporting. The first pin, NPOR, reports on the status of the V5, 3V3, and 1V2x output levels. This signal goes low if either of these outputs are out of regulation. The NPOR signal may also toggle low for 2 ms if a watchdog fault is detected. The second pin, FFn (Active Low Fault Flag), reports on all faults. FFn goes low if a fault within the ARG81403 exists. The FFn pin can be used by the processor as an alert to check the status of the ARG81403 via SPI and see where the fault occurred.

Built-In Self-Test (BIST)

The ARG81403 includes a self-test that is performed during the startup sequence. This self-test verifies the operation of the undervoltage and overvoltage detection circuits for the main outputs and overtemperature (thermal shutdown: TSD) detection circuit.

In the event the self-test fails, the ARG81403 will report the failure through SPI.

UNDERVOLTAGE DETECT SELF-TEST

The undervoltage (UV) detectors are verified during startup of the ARG81403. A voltage that is lower than the undervoltage threshold is applied to each UV comparator; this should cause the relative undervoltage fault bit in the diagnostic registers to change state. If the diagnostic UV register bits change state, the corresponding verify register bits will latch low. When the test of all UV detectors is complete, the verify register bits will remain low if the test passed. If any UV bits in the verify registers after test are not set low, then the verification has failed. The following UV detectors are tested: VREG, V5, 3V3, 1V2x, V5P1, and V5P2.

OVERVOLTAGE DETECT SELF-TEST

The overvoltage (OV) detectors are verified during startup of the ARG81403. A voltage is applied to each OV comparator that is higher than the overvoltage threshold; this should cause the relative overvoltage fault bit in the diagnostic registers to change state. If the diagnostic OV register bits change state, the corresponding verify register bits will latch low. When the test of all OV detectors is complete, the verify register bits will remain low if the test passed. If any OV bits in the verify registers after test are not set low, then the verification has failed. The following OV detectors are tested: VREG, V5, 3V3, 1V2x, V5P1, and V5P2.

OVERTEMPERATURE SHUTDOWN SELF-TEST

The overtemperature shutdown (TSD) detector is verified on startup of the ARG81403. A voltage is applied to the comparator that is lower than the overtemperature threshold, and should cause

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the general fault flag to be active and an overtemperature fault bit, TSD, to be latched in the Verify Result register 0. When the test is complete, the general fault flag will be cleared and the overtemperature fault will remain in the Verify Result register 0 until reset. If the TSD bit is not set low, then the verification has failed.

Level Shifter Interface

The ARG81403 implements seven channels of level shifter interfaces: LS1 through LS6 are inverted and VIGN is non-inverted.

The input threshold of LS1-6 is SNSVIN ratio-related and the VIGN input threshold is fixed value, as shown in the Electrical Characteristics table, and each output is driven by V5.

The following connection is recommended when a channel is not used:

- LSINx, VIGN-IN: tied to GND
- LSOUTx, VIGN-OUT: open

If the input is open, its operation will be the same as when low-level signal is applied.

Two-Wire Speed (Rotational) Sensor Interface

The ARG81403 implements three channels of rotational sensor IOs that are designed to interface between a microprocessor and a pair of two-wire Hall-effect sensor ICs.

The ARG81403 has one dedicated VIN terminal (SNSVIN) and three pairs of protected high-side and low-side low resistance MOSFET switches to deliver the supply voltage to the three Hall-effect devices.

Each switch is independently protected with current-limiting circuitry and the high-side switches have overvoltage protection. The output switches are able to source at least 25 mA per channel before current limiting.

Typical two-wire Hall device applications require the user to measure the supply current to determine whether the Hall IC is switched on (magnetic field present) or switched off (no magnetic field present). This is accomplished by using an external series shunt resistor and protection circuits for the microprocessor. In many systems, the sensed voltage is used as the input to a microprocessor analog-to-digital (A-to-D) input. This provides the system with an indication of the status of the two-wire switch, as well as providing capability for diagnostic information if there is an open or shorted Hall device.

The ARG81403 integrates the following terminals to support above function. (See Table 3 and Figure 7)

Switchable voltage supply high-side and low-side switches will be activated after the V5 regulator output exceeds the undervoltage rising thresholds ($V_{V5(UV,H)}$).

SNSVIN (VIN of the rotational sensor interface circuit):

The power input terminal; separated from regulator's power input; common for three rotational sensor IOs and used for the reference of level-shifter circuits.

SNSxP (Connection of the positive side of Hall-effect sensor IC):

Switchable voltage supply (high-side switch) output terminal to the Hall-effect sensor IC with overcurrent and overvoltage protection. (x = 1, 2, or 3)

SNSxN (Connection of the negative side of Hall-effect sensor IC):

Switchable voltage supply (low-side switch) input terminal to the Hall-effect sensor IC with overcurrent protection. (x = 1, 2, or 3)

SNSxR (Sensor/Resistor connection):

External series shunt resistor connection terminal. (x = 1, 2, or 3)

SNSxFB (Sensor/Feedback input):

Sensed voltage input terminal from an external series shunt resistor, can be added RC filter for EMC. (x = 1, 2, or 3)

SNSxO (Sensor/Output to MCU):

Output terminal for the input to a microprocessor. (x = 1, 2, or 3)

Unused terminal treatment:

When some channel is not tied to a sensor, the following connection is recommended.

- SNSxP: tied to SNSVIN
- SNSxN, FB, and R: tied to GND
- SNSxO: open

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Table 3: Protection function of the Rotational Sensor Interface

Functions	Detection Points	Actions	Latch or Non-Latch	Reset Method
High-Side SW Overvoltage	From SNSxP to GND	$V_{SNSxP} > V_{SNSxP(OV,H)}$: Turns off respective CH's high-side SW. $V_{SNSxP} < V_{SNSxP(OV,L)}$: Turns on respective CH's high-side SW. If OV condition happens, SNSxP voltage looks like hysteretic operation between $V_{SNSxP(OV,H)}$ and $V_{SNSxP(OV,L)}$. (the other CHs are not affected)	Non-latch	Decrease voltage
High-Side SW Overcurrent	From SNSVIN to SNSxP	Limit the output current as hiccup mode until the output load is reduced or V5 decays below $V_{V5(UV,L)}$ threshold. (the other CHs are not affected)	Non-latch	Decrease current
Low-Side SW Overcurrent	From SNSxN to SNSxR	Limit the output current as hiccup mode until the output load is reduced or V5 decays below $V_{V5(UV,L)}$ threshold. (the other CHs are not affected)	Non-latch	Decrease current

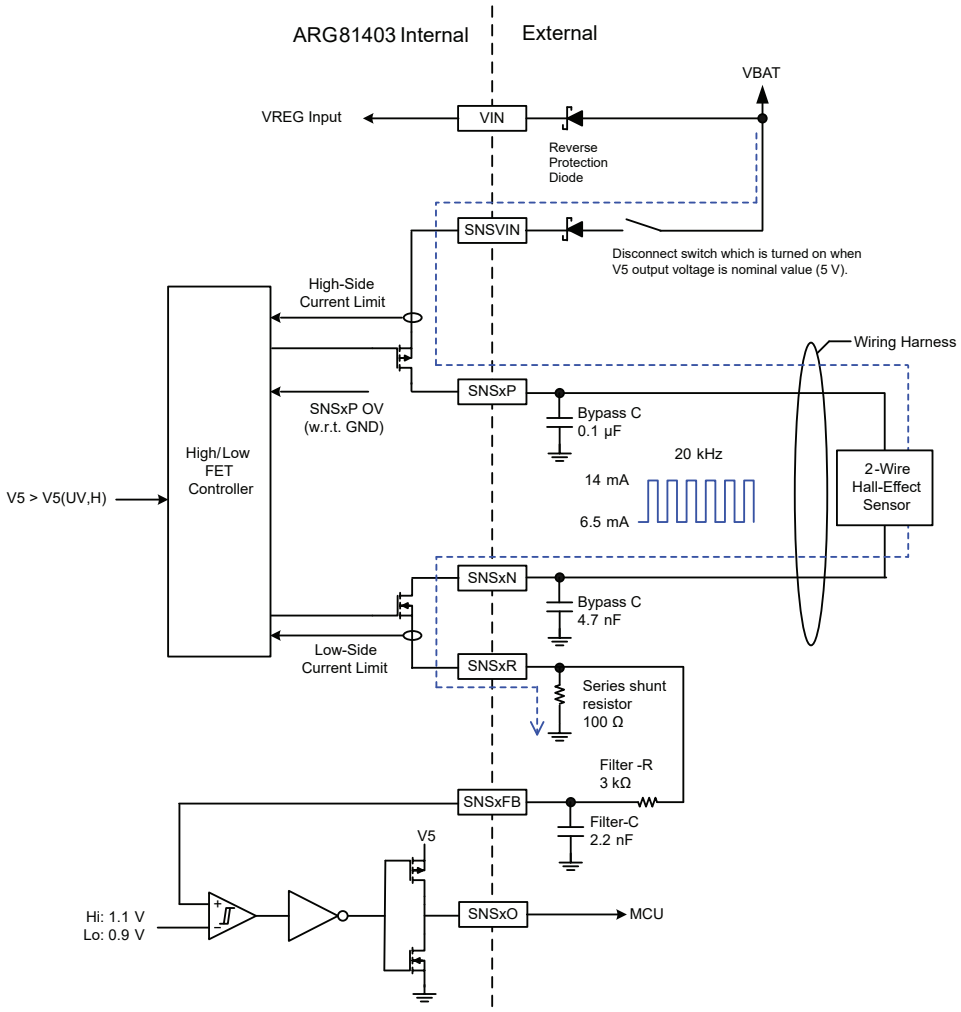

Figure 7: Typical Application with Two-Wire Hall-Effect Speed Sensor IC

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VIN 2nd UV Detection

The ARG81403 implements two VIN undervoltage detection thresholds: VIN UVLO Stop Threshold and VIN Undervoltage Detection Threshold. VIN UVLO Stop Threshold, $V_{VIN\ (STOP)}$, is the master detector to shut down the device before the device cannot operate due to low VIN. VIN undervoltage detection threshold is used for the alert/evidence of before/after fault detection. When VIN drops to less than VIN 2nd UV threshold but more than $V_{VIN(STOP)}$, VIN_2nd_UV bit will be set to "1" and each application's control unit can realize the VIN decay event via SPI.

Table 4: VIN 2nd UV Detection

VIN	VIN Rising	VIN Rising	VIN Rising	VIN Falling	VIN Falling
	VIN State #1: $0\ V < V_{VIN} < V_{VIN(START)}$	VIN State #2: $V_{VIN(START)} < V_{VIN} < V_{VIN(UV2,L)}$	VIN State #3: $V_{VIN(UV2,L)} < V_{VIN}$	VIN State #4: $V_{VIN(UV2,L)} > V_{VIN} > V_{VIN(STOP)}$	VIN State #5: $V_{VIN(STOP)} > V_{VIN} > 0\ V$
(SPI) VIN_2nd_UV	Device does not operate	0: Not detected		1: detected, latched until W1C or device shuts off.	Device does not operate
FFn (terminal)		No effect		Low since VIN_2nd_UV detection	
(SPI) FF		No effect		1: Fault since VIN_2nd_UV detection	

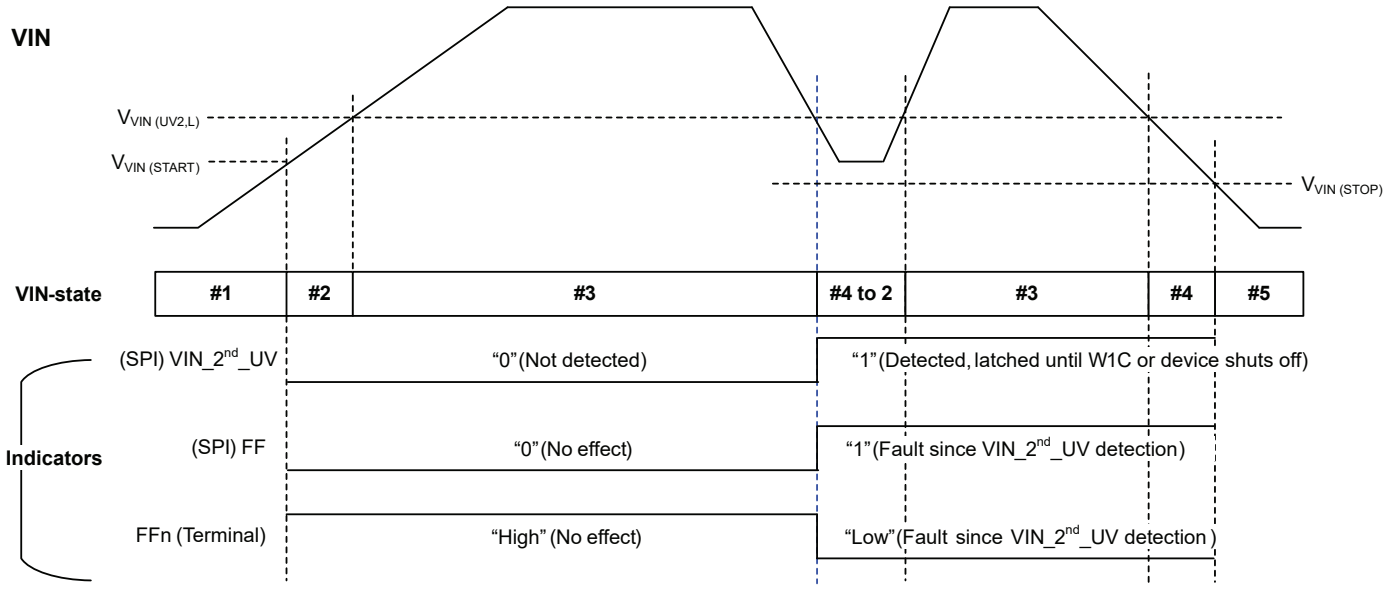

Figure 8: VIN 2nd UV detection

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Watchdog

The ARG81403 has two types of watchdog functions: single-ended timer and window timer. When the regulators (VREG, V5, 3V3, and 1V2x) have been above their undervoltage thresholds, watchdog activation delay (startup: $t_{dWD(START)}$) timer will be in initiated. When $t_{dWD(START)}$ is expired and WDENn is low or open, WD is activated, WD state will be in the configuration state ("Config") and watchdog activation delay (Operation: $t_{dWD(OP)}$) timer will be in initiated. When $t_{dWD(OP)}$ is expired, watchdog timer will be in normal operation. Moving back to Config mode requires secure SPI command (WD Secure Key register).

SINGLE-ENDED WATCHDOG TIMER

The ARG81403 single-ended watchdog circuit monitors an external clock applied to the WDIN pin. This clock should be generated by the microcontroller or DSP. The time between rising edges of the clock must fall within a SPI programmed Maximum (slow) timeout or a watchdog fault (WDT_F bit and FF bit) will be generated. A watchdog fault will set NPOR low for $t_{WD(FAULT)}$, typically 2 ms.

After startup, if no clock edges are detected at WDIN for watchdog activation delay (startup: $t_{dWD(START)}$) + maximum timeout (written in 0x07), the ARG81403 will generate watchdog fault and reset its counters. This process will repeat until the system recovers and clock edges are applied to WDIN.

WINDOW WATCHDOG TIMER

The ARG81403 window watchdog circuit monitors an external clock applied to the WDIN pin. This clock should be generated by the microcontroller or DSP. The time between rising edges of the clock must fall within a SPI-programmed window or a watchdog fault (WDT_F bit and FF bit) will be generated. A watchdog fault will set NPOR low for $t_{WD(FAULT)}$, typically 2 ms.

After startup, if no clock edges are detected at WDIN for watchdog activation delay (startup: $t_{dWD(START)}$) + maximum timeout (written in Config 0 register), the ARG81403 will generate watchdog fault and reset its counters. This process will repeat until the system recovers and clock edges are applied to WDIN.

Table 5: Watchdog Fault

WD Mode	WD Fault Conditions	Descriptions	Reporting Registers
Single-Ended	Timeout Fault (Slow fault)	Rising edges of WDIN signal are longer than maximum (slow) timeout value which is programmed via SPI: WIN_Timer [0:2].	WDT_F
Window Timer	Timeout Fault (Slow fault)	Rising edges of WDIN signal are longer than maximum (slow) timeout value which is programmed via SPI: WIN_Timer [0:2].	WDT_F
	Timeout Fault (Fast fault)	Rising edges of WDIN signal are shorter than minimum (fast) timeout value which is programmed via SPI: WIN_Timer [0:2] and WIN_Timer_R [0:1]. Minimum WD timeout (Fast) = "Maximum (Slow) TO" × "Ratio of Minimum (Fast)/Maximum (Slow)". e.g. Max-timeout (slow) = 64 ms (slow-TO) × 1/8 (Ratio: fast/slow) = 8 ms	WDT_F

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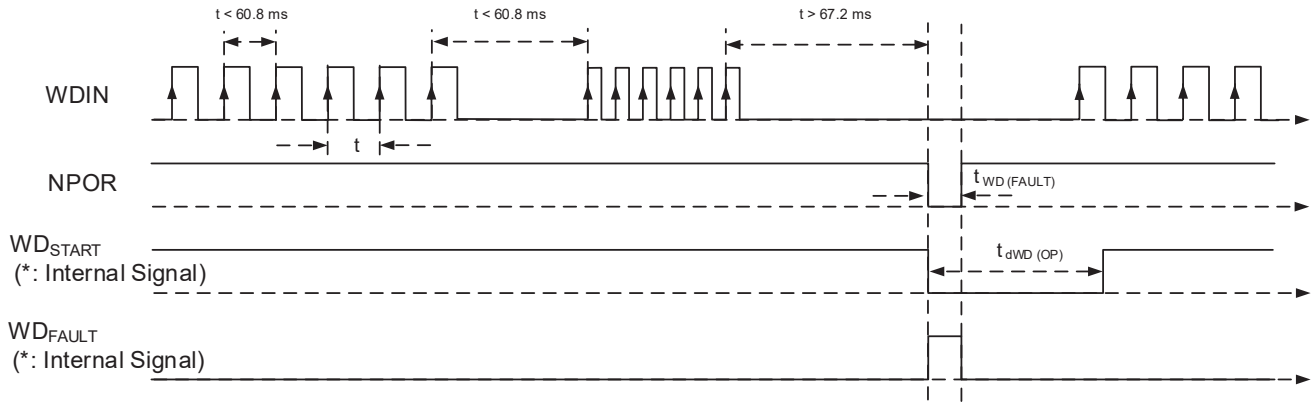

Figure 9: Typical Single-Ended Watchdog Timer Operation

Max (slow) WD Time out: 64 ms (±5%: 3.2 ms) case is shown.
WD will not indicate a fault if the rising edges of WDIN occur within 60.8 ms of each other.
WD will indicate a fault if the rising edges of WDIN occur more than 67.2 ms apart.

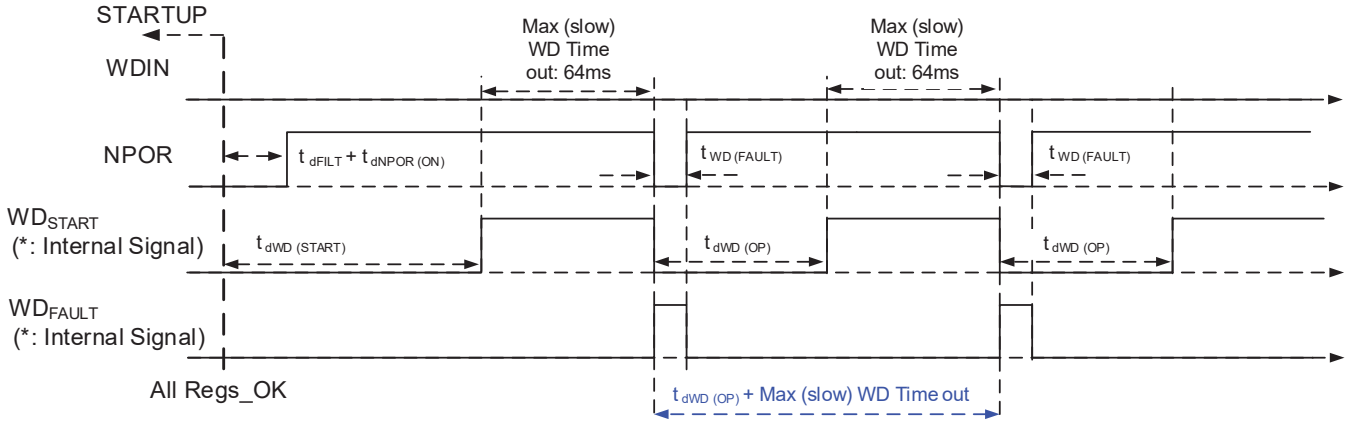

Figure 10: Single-Ended Watchdog Timer Operation Showing Start Delay and Missing WDIN signal

Max (slow) WD Time out: 64 ms (±5%: 3.2 ms) case is shown,
After startup, if WDIN is stuck low (or high), NPOR will periodically pulse LOW for 2 ms.
The time between NPOR fault indications will be $t_{dWD(OP)}$ + Max (slow) WD Timeout.

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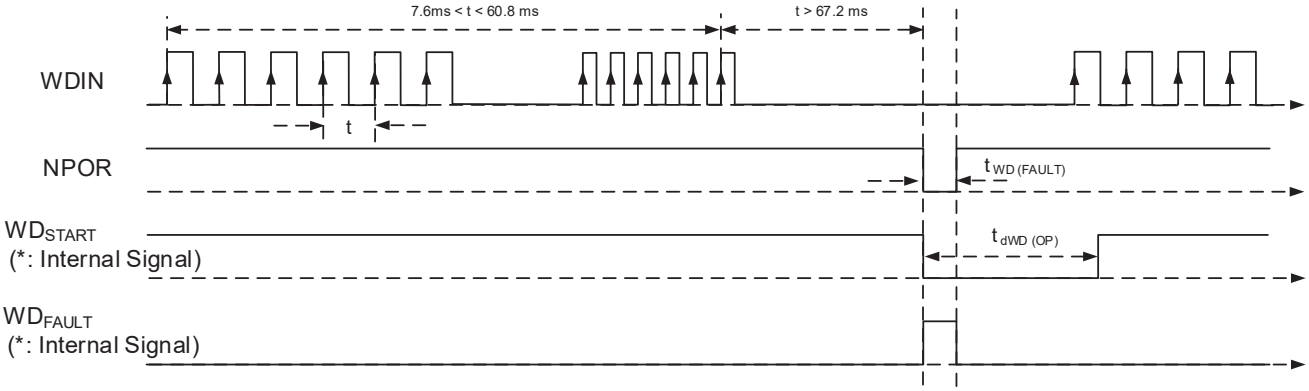

Figure 11: Typical Window Watchdog Timer Operation, Slow fault

Max (slow) WD Time out: 64 ms (±5%: 3.2 ms) and Timeout ratio: 1/8 case is shown.
WD will indicate a fault if the rising edges of WDIN occur more than 67.2 ms apart.

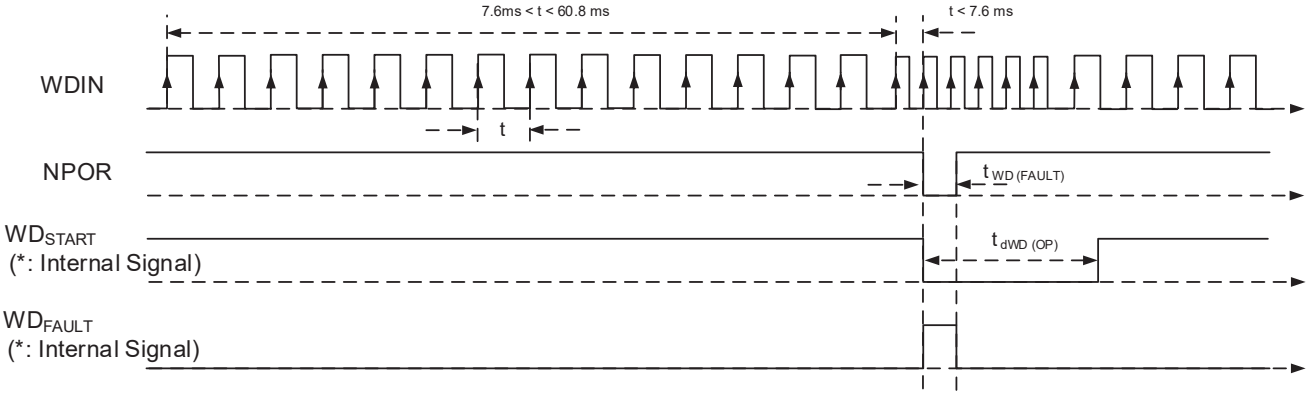

Figure 12: Typical Window Watchdog Timer Operation, Fast fault

Max (slow) WD Time out: 64 ms (±5%: 3.2 ms) and Timeout ratio: 1/8 case is shown.
WD will indicate a fault if the rising edges of WDIN occur less than 7.6 ms apart.

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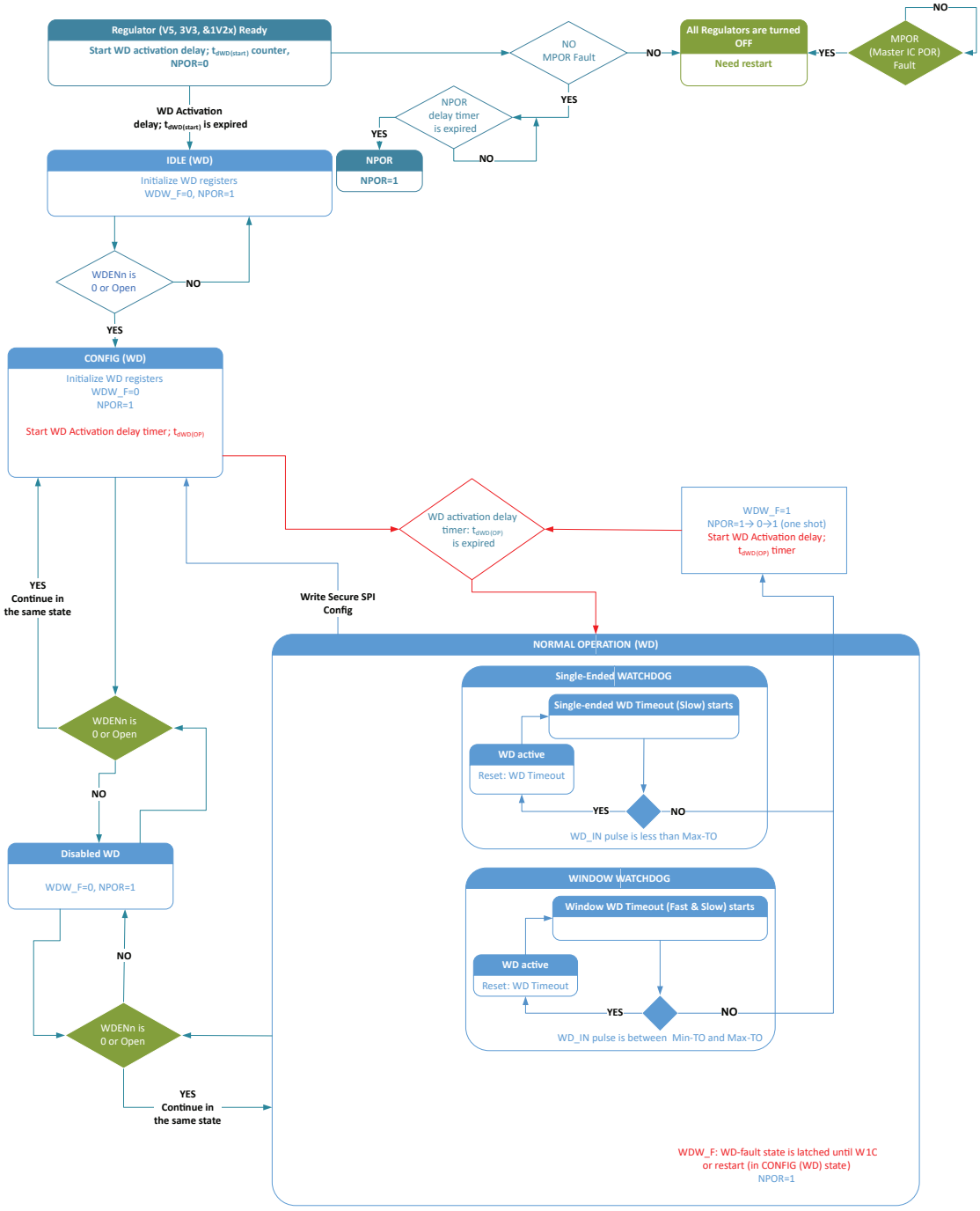

Figure 13: Watchdog State Diagram

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SERIAL COMMUNICATION INTERFACE

The ARG81403 provides the user with a three-wire synchronous serial interface that is compatible with SPI (Serial Peripheral Interface). A fourth wire can be used to provide diagnostic feedback and readback of the register content.

The serial interface timing requirements are specified in the Electrical Characteristics table and illustrated in the Serial Interface Timing diagram (Figure 2). Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. STRn is normally held high and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple SDI slave units to use common SDI, SCK, and SDO connections. Each slave then requires an independent STRn connection.

When 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the Diagnostic register is reset.

If there are more than 16 rising edges on SCK or if STRn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without writing data to the registers. In addition, the Diagnostic register will not be reset and the SE (serial error) bit will be set to indicate a data transfer error.

Diagnostic information or the contents of the configuration and control registers are output on the SDO terminal MSB first, while STRn is low, and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF (fault flag) bit from the Diagnostic register, is output as soon as STRn goes low.

Each of the programmable (configuration and control) registers has a write bit, WR (bit 10), as the first bit after the register address. This bit must be set to 1 to write the subsequent bits into the selected register. If WR is set to 0, then the remaining data bits (bits 9 to 0) are ignored. The state of the WR bit also determines the data output on SDO. If WR is set to 1 then the Diagnostic register is output. If WR is set to 0, then the contents of the register selected by the first five bits is output. In all cases, the first bit output on SDO will always be the FF bit from the Diagnostic Register.

The ARG81403 has 15 register banks. Bit <15:11> represents the register address for read and write. Bit <10> detects the read and write operation: for write operation, Bit <10> = 1, and for read operation, bit value is logic low. Bit <9> is an unused bit. Maximum data size is eight bits so Bit<8:1> represents the data word. The last bit in a serial transfer, Bit<0>, is a parity bit that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transmission should always be

Pattern at SDI Pin

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A4	A3	A2	A1	A0	W/R	NU	D7	D6	D5	D4	D3	D2	D1	D0	P
5-Bit Address							8-Bit Data								

Pattern at SDO Pin after SDI Write

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FF	SE	ENBAT_S	WDT_F	0	0	TSD_OK	DBE	VREG_OK	V5_OK	3V3_OK	1V2x_OK	V5P1_OK	V5P2_OK	0	P
Diagnostics															

Pattern at SDO Pin after SDI Read

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FF	SE	ENBAT_S	WDT_F	0	0	TSD_OK	D7	D6	D5	D4	D3	D2	D1	D0	P
Diagnostics							8-Bit Data								

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an odd number. This ensures that there is always at least one bit set to 1 and one bit set to 0 and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

Register data is output on the SDO terminal MSB first, while STRn is low, and changes to the next bit on each falling edge of the SCK. The first bit which is always the FF bit from the status register, is output as soon as STRn goes low.

If there are more than 16 rising edges on SCL, or if STRn goes high and there are fewer than 16 rising edges on SCK, then the write will be cancelled without writing data to the registers. In addition, the diagnostic register will not be reset; the SE bit will be set to indicate a data transfer error.

SDI: Serial data logic input with pull-down. 16-bit serial word, input MSB first.

SCK: Serial clock logic input with pull-down. Data is latched in from SDI on the rising edge of SCL. There must be 16 rising edges per write and SCK must be held high when STRn changes.

STRn: Serial data strobe and serial access enable logic input with pull-up. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

SDO: Serial data output. High impedance when STRn is high. Output bit 15 of the status register, the fault flag (FF), as soon as STRn goes low.

Register Mapping

STATUS REGISTERS

The ARG81403 provides five status registers. They provide real-time status of various functions within the ARG81403.

These registers report on the status of all five system rails. They also report on internal rail status, including the charge pump and VREG rails. In addition, rotational sensor status is reported. The general fault flag and watchdog fault state are also found in these status registers.

The logic that creates the power reset status is reported through these registers.

CONFIGURATION REGISTERS

The ARG81403 allows configuration of the watchdog validation parameters, disabling dithering function (SSCG: spread spectrum clock generator) and overvoltage detection of V5.

The watchdog can only be configured during Config state. This occurs when the ARG81403 is initially enabled or the watchdog is restarted through SPI.

The ARG81403 uses frequency dithering for pre-regulator to help reduce EMC noise. The user can disable this feature through the SPI. Default is enabled.

All WD Configuration must be entered before modifying the WD_SEL bits; this means write Config-1 before Config-0.

DIAGNOSTIC REGISTERS

There are multiple diagnostic registers in the ARG81403. These registers can be read to evaluate the status of the ARG81403. The high-level registers will tell which area a fault has occurred. Logic high on a data bit in this register implies that no fault has occurred. The following are monitored by these registers:

- All five outputs
- ARG81403 bias voltage
- Charge pump voltage
- Pre-regulator voltage
- Overtemperature
- Watchdog output
- Shorts on LX pin
- Input voltage (VIN)

Note some of these faults will cause the ARG81403 to shut down which might shutdown the microprocessor monitoring the SPI. In this event, the only way to read the fault would be to have alterative power to the microprocessor so it can read the registers. If VCC of the ARG81403 shuts down, all stored register information is lost and the registers revert to default values.

Other diagnostic registers store more detail on each fault; this includes:

- Overvoltage on a particular output or internal rail
- Undervoltage on a particular output or internal rail

The diagnostic registers are latched registers and will hold data if a fault has occurred but recovered. These registers are reset by writing a ‘1’ to them.

CONTROL REGISTER

The output enable/disable register provides the user control of the LDO outputs: V5P1 and V5P2.

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WATCHDOG MODE KEY REGISTER

At time, reconfiguration may be necessary. To do this, the user must put the watchdog into “Config Mode”. This is done by setting the writing a sequence of key words to the “watchdog_ mode_key” register. If the correct word sequence is not received, then the sequence must restart.

If VCC has not been removed from the ARG81403, the watchdog will restart with the current configuration.

VERIFY RESULT REGISTERS

On every startup, the ARG81403 performs a self-test of the UV and OV detection circuits. This test should cause the diagnostic registers to toggle state. If the diagnostic register successfully changes state, the verify result register will latch low. Upon completion of startup, the systems microprocessor can check the verify result registers to see if the self-test passed.

Table 6: Register Map

Register Name	15 to 11 (Address)	10	9	8	7	6	5	4	3	2	1	0
Status 0	0x00	RO		FF	SE	DBE	NPOR_S	NPOR_OK				P
		RW1C							WDT_F			
Status 1	0x01	RO		VCC_OK	VCP_OK	VREG_OK	V5_OK	3V3_OK	V5P1_OK	V5P2_OK	1V2x_OK	P
Status 2	0x02	RO				TSD_OK	LX1_OK	ENB_S	ENBAT_S	POK5V_S		P
		RW1C									RS1_OV	
Status 3	0x03	RW1C		RS3_H_OC	RS3_L_OC	RS3_OV	RS2_H_OC	RS2_L_OC	RS2_OV	RS1_H_OC	RS1_L_OC	P
Status 4	0x04	RO					FFn_OK	POK5V_OK	WD_state_2	WD_state_1	WD_state_0	P
Diag 0	0x05	RW1C		VCC_OV	VCP_OV	VCP_UV	VREG_OV	VREG_UV	V5_OV	V5_UV	VIN_2nd_UV	P
Diag 1	0x06	RW1C		3V3_OV	3V3_UV	V5P1_OV	V5P1_UV	V5P2_OV	V5P2_UV	1V2x_OV	1V2x_UV	P
Config 0	0x07	RW		WD_SEL_2	WD_SEL_1	WD_SEL_0	WIN_Timer_2	WIN_Timer_1	WIN_Timer_0	WIN_Timer_R1	WIN_Timer_R0	P
Config 1	0x08	RW		OV_DIS	DITH_DIS							P
Config 2	0x09	RW									SPI_TEST	P
n/a	0x0A	RW										P
WD Secure Key	0x0B	WO		Key code entry (Write Only)								P
Control	0x0C	RW		V5P2_EN	V5P1_EN							P
Verify result 0	0x0D	RW1C		BIST_FAIL	TSD_FAIL	VREG_OV_FAIL	VREG_UV_FAIL	V5_OV_FAIL	V5_UV_FAIL	3V3_OV_FAIL	3V3_UV_FAIL	P
Verify result 1	0x0E	RW1C			V5POK_UV_FAIL	V5P1_OV_FAIL	V5P1_UV_FAIL	V5P2_OV_FAIL	V5P2_UV_FAIL	1V2x_OV_FAIL	1V2x_UV_FAIL	P

Register Types:
RO = Read-Only
RW = Read or Write
RW1C = Read or Write 1 to clear
WO = Write-Only

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Status Register 0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status 0	0	0	0	0	0	RO		FF	SE	DBE	NPOR_S	NPOR_OK				P
						RW1C							WDT_F			
							0	0	0	0	0	0	0	0	0	

FF	Fault Flag	
0	No Fault	Default
1	Fault	

SE	Serial Error Flag [1]	
0	No Fault	Default
1	Fault	

DBE	EEPROM Dual Bit Error Flag [2]	
0	No Fault	Default
1	Fault	

NPOR_S	Power-On Reset Internal Logic Status	
0	NPOR is Low	Default
1	NPOR is High	

NPOR_OK	NPOR Signal Matches Device Demand	
0	Fault	Default
1	No Fault	

WDT_F	Watchdog Timer Fault Flag	
0	No Fault or Single ended or Window timer Watchdog is disabled	Default
1	Single-ended or Window timer Watchdog Timeout Fault	

[1] SE Fault: If more than sixteen rising edges on SCK are detected while STRn is LOW or if STRn goes HIGH and there are fewer than sixteen rising edges on SCK or parity bit error.

[2] DBE Fault: dual bit error occurred loading the trim data from EEPROM.

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Status Register 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status 1	0	0	0	0	1	RO		VCC_OK	VCP_OK	VREG_OK	V5_OK	3V3_OK	V5P1_OK	V5P2_OK	1V2x_OK	P
							0	0	0	0	0	0	0	0	0	

VCC_OK	VCC Output Rail OK	
0	Fault (OV)	Default
1	No Fault	

VCP_OK	Charge Pump Output Rail OK	
0	Fault (UV or OV)	Default
1	No Fault	

VREG_OK	VREG Output Rail OK	
0	Fault (UV or OV)	Default
1	No Fault	

V5_OK	V5 Output Rail OK	
0	Fault (UV or OV)	Default
1	No Fault	

3V3_OK	3V3 Output Rail OK	
0	Fault (UV or OV)	Default
1	No Fault	

V5P1_OK	V5P1 Output Rail OK	
0	Fault (UV or OV)	Default
1	No Fault	

V5P2_OK	V5P2 Output Rail OK	
0	Fault (UV or OV)	Default
1	No Fault	

1V2x_OK	1V2x Output Rail OK	
0	Fault (UV or OV)	Default
1	No Fault	

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Status Register 2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status 2	0	0	0	1	0	RO				TSD_OK	LX1_OK	ENB_S	ENBAT_S	POK5V_S		P
						RW1C									RS1_OV	
							0	0	0	0	0	0	0	0	0	

TSD_OK	Thermal Shutdown (Overtemperature) Detection Flag	
0	Overtemperature is detected	Default
1	OK (Overtemperature is not detected)	

LX1_OK	Pre-Regulator SW-node (LX1) Fault Detection Flag	
0	Fault on LX1 is detected	Default
1	OK (LX1 is working correctly)	

ENB_S	Logic Enable (ENB) Status	
0	ENB is low	Default
1	ENB is high	

ENBAT_S	Battery Enable (ENBAT) Status	
0	ENBAT is low	Default
1	ENBAT is high	

POK5V_S	Power OK V5 Internal Logic Status	
0	POK5V is Low	Default
1	POK5V is High	

RS1_OV	Rotation Sensor 1 High-Side Input (SNS1P) Output Overvoltage Detection	
0	OK (Overvoltage is not detected)	Default
1	Overvoltage is detected	

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Status Register 3

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status 3	0	0	0	1	1	RW1C		RS3_H_OC	RS3_L_OC	RS3_OV	RS2_H_OC	RS2_L_OC	RS2_OV	RS1_H_OC	RS1_L_OC	P
							0	0	0	0	0	0	0	0	0	

RS3_H_OC	Rotation Sensor 3 High-Side Overcurrent Detection	
0	OK (Overcurrent is not detected)	Default
1	Overcurrent is detected	

RS3_L_OC	Rotation Sensor 3 Low-Side Overcurrent Detection	
0	OK (Overcurrent is not detected)	Default
1	Overcurrent is detected	

RS3_OV	Rotation Sensor 3 High-Side Input (SNS3P) Output Overvoltage Detection	
0	OK (Overvoltage is not detected)	Default
1	Overvoltage is detected	

RS2_H_OC	Rotation Sensor 2 High-Side Overcurrent Detection	
0	OK (Overcurrent is not detected)	Default
1	Overcurrent is detected	

RS2_L_OC	Rotation Sensor 2 Low-Side Overcurrent Detection	
0	OK (Overcurrent is not detected)	Default
1	Overcurrent is detected	

RS2_OV	Rotation Sensor 2 High-Side Input (SNS2P) Output Overvoltage Detection	
0	OK (Overvoltage is not detected)	Default
1	Overvoltage is detected	

RS1_H_OC	Rotation Sensor 1 High-Side Overcurrent Detection	
0	OK (Overcurrent is not detected)	Default
1	Overcurrent is detected	

RS1_L_OC	Rotation Sensor 1 Low-Side Overcurrent Detection	
0	OK (Overcurrent is not detected)	Default
1	Overcurrent is detected	

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Status Register 4

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status 4	0	0	1	0	0	RO					FFn_OK	POK5V_OK	WD_ state_2	WD_ state_1	WD_ state_0	P
							0	0	0	0	0	0	0	0	0	

FFn_OK	FFn Signal Matches Device Demand	
0	Fault	Default
1	No Fault	

POK5V_OK	POK5V Signal Matches Device Demand	
0	Fault	Default
1	No Fault	

WD_state_2	WD_state_1	WD_state_0	Watchdog State	
0	0	0	Idle	Default
0	0	1	Configure	
0	1	0	n/a	
0	1	1	Normal (Operation)	
1	0	0	n/a	
1	0	1	Disabled WD	
1	1	0	n/a	
1	1	1	n/a	

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Diag Register 0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Diag 0	0	0	1	0	1	RW1C		VCC_OV	VCP_OV	VCP_UV	VREG_OV	VREG_UV	V5_OV	V5_UV	VIN_2nd_UV	P
							0	0	0	0	0	0	0	0	0	

VCC_OV	VCC Output Overvoltage Detection	
0	OK (Overvoltage is not detected)	Default
1	Overvoltage is detected	

VCP_OV	VCP Output Overvoltage Detection	
0	OK (Overvoltage is not detected)	Default
1	Overvoltage is detected	

VCP_UV	VCP Output Undervoltage Detection	
0	OK (Undervoltage is not detected)	Default
1	Undervoltage is detected	

VREG_OV	VREG Output Overvoltage Detection	
0	OK (Overvoltage is not detected)	Default
1	Overvoltage is detected	

VREG_UV [1]	VREG Output Undervoltage Detection	
0	OK (Undervoltage is not detected)	Default
1	Undervoltage is detected	

V5_OV	V5 Output Overvoltage Detection	
0	OK (Overvoltage is not detected)	Default
1	Overvoltage is detected	

V5_UV [1]	V5 Output Undervoltage Detection	
0	OK (Undervoltage is not detected)	Default
1	Undervoltage is detected	

VIN_2nd_UV	VIN 2nd Undervoltage Detection	
0	OK (Undervoltage is not detected)	Default
1	Undervoltage is detected	

[1] VREG-UV/V5-UV/3V3-UV/1V2x-UV detection flag is masked (kept “0”) until NPOR turn-on delay timer: $t_{dNPOR(ON)}$ is expired at startup.

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Diag Register 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Diag 1	0	0	1	1	0	RW1C		3V3_OV	3V3_UV	V5P1_OV	V5P1_UV	V5P2_OV	V5P2_UV	1V2x_OV	1V2x_UV	P
							0	0	0	0	0	0	0	0	0	

3V3_OV	3V3 Output Overvoltage Detection	
0	OK (Overvoltage is not detected)	Default
1	Overvoltage is detected	

3V3_UV [1]	3V3 Output Undervoltage Detection	
0	OK (Undervoltage is not detected)	Default
1	Undervoltage is detected	

V5P1_OV	V5P1 Output Overvoltage Detection	
0	OK (Overvoltage is not detected)	Default
1	Overvoltage is detected	

V5P1_UV [2]	V5P1 Output Undervoltage Detection	
0	OK (Undervoltage is not detected or V5P1_EN-low)	Default
1	Undervoltage is detected	

V5P2_OV	V5P2 Output Overvoltage Detection	
0	OK (Overvoltage is not detected)	Default
1	Overvoltage is detected	

V5P2_UV [2]	V5P2 Output Undervoltage Detection	
0	OK (Undervoltage is not detected and V5P2_EN-low)	Default
1	Undervoltage is detected	

1V2x_OV	1V2x Output Overvoltage Detection	
0	OK (Overvoltage is not detected)	Default
1	Overvoltage is detected	

1V2x_UV [1]	1V2x Output Undervoltage Detection	
0	OK (Undervoltage is not detected)	Default
1	Undervoltage is detected	

[1] VREG-UV/V5-UV/3V3-UV/1V2x-UV detection flag is masked (kept “0”) until NPOR turn-on delay timer: $t_{dNPOR(ON)}$ is expired at startup.

[2] V5P1/2-UV detection flag is activated when V5P1_EN or V5P2_EN is set 1, when V5P1_EN or V5P2_EN is set 0, V5P1/ 2-UV detection flag is masked (kept “0”).

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Config Register 0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 0	0	0	1	1	1	RW		WD_ SEL_2	WD_ SEL_1	WD_ SEL_0	WIN_ Timer_2	WIN_ Timer_1	WIN_ Timer_0	WIN_ Timer_R1	WIN_ Timer_ R0	P
							0	1	0	0	0	1	1	0	0	

WD_SEL_2	WD_SEL_1	WD_SEL_0	Watchdog Mode Selection	
0	0	0	Waiting for Configuration	
0	0	1		
0	1	0		
0	1	1		
1	0	0	Single ended WD Timer Only	Default
1	0	1	Window WD Timer Only	
1	1	0	n/a	
1	1	1	n/a	

WIN_Timer_2	WIN_Timer_1	WIN_Timer_0	Maximum (Slow) WD Timeout of Single-Ended WD or Window-WD [1][2]	
0	0	0	4 ms	
0	0	1	16 ms	
0	1	0	32 ms	
0	1	1	64 ms	Default
1	0	0	72 ms	
1	0	1	80 ms	
1	1	0	96 ms	
1	1	1	128 ms	

WD_Timer_R1	WD_Timer_R0	Ratio of Minimum (Fast) / Maximum (Slow) WD Timeout [1][2]	
0	0	1/8	Default
0	1	1/4	
1	0	1/2	
1	1	3/4	

[1] When “Single-Ended WD Timer Only (WD_SEL_1=0 and WD_SEL_0 =”00”) is chosen, Maximum WD timeout (Slow) will be active. When “Window WD Timer (WD_SEL_1=0 and WD_SEL_0 = ”01” or “11”) is chosen, both Maximum WD timeout (Slow) and Ratio of Minimum (Fast) / Maximum (Slow) and will be active. For example, default case of Window Timer WD: max-timeout (slow) = 64 ms and min-timeout (slow) = 64 ms × 1/8 = 8 ms.

[2] Typical number at the internal clock is center value, need to keep enough margin for ±5% tolerance of the internal clock.

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Config Register 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 1	0	1	0	0	0	RW		OV_DIS	DITH_ DIS							P
							0	0	0	0	0	0	0	0	0	

OV_DIS	Disable Overvoltage Protection of V5	
0	Overvoltage protection of V5 is enabled	Default
1	Overvoltage protection of V5 is disabled	

DITH_DIS	Disable Dithering Function	
0	Dithering is enabled	Default
1	Dithering is disabled	

Config Register 2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 2	0	1	0	0	1	RW									SPI_TEST	P
							0	0	0	0	0	0	0	0	0	

SPI_TEST	SPI_TEST	
0	Test bit for customer	Default
1	Test bit for customer	

Watchdog Secure Key Register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD Secure Key	0	1	0	1	1	WO		KEY_7	KEY_6	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0	P
							0	0	0	0	0	0	0	0	0	

	Config mode
WORD1	0xD3
WORD2	0x33
WORD3	0xCD

Three 8-bit words must be sent in the correct order to enable config-mode. If an incorrect word is received, then the register resets and the first word has to be resent.

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Control Register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control	0	1	1	0	0	RW		V5P2_ EN	V5P1_ EN							P
							0	0	0	0	0	0	0	0	0	

V5P2_EN	Enable V5P2	
0	V5P2 is Disabled	Default
1	V5P2 is Enabled	

V5P1_EN	Enable V5P1	
0	V5P1 is Disabled	Default
1	V5P1 is Enabled	

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Verify Register 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Verify 0	0	1	1	0	1	RW1C		BIST_FAIL	TSD_ FAIL	VREG_ OV_FAIL	VREG_ UV_FAIL	V5_OV_FAIL	V5_UV_FAIL	3V3_OV_FAIL	3V3_UV_ FAIL	P
							0	1	1	1	1	1	1	1	1	

BIST_FAIL	Built-in Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

TSD_FAIL	Thermal Shutdown Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

VREG_OV_FAIL	VREG Overvoltage Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

VREG_UV_FAIL	VREG Undervoltage Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

V5_OV_FAIL	V5 Overvoltage Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

V5_UV_FAIL	V5 Undervoltage Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

3V3_OV_FAIL	3V3 Overvoltage Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

3V3_UV_FAIL	3V3 Undervoltage Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

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Verify Register 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Verify 1	0	1	1	1	0	RW1C	0	0	V5POK_UV_FAIL	V5P1_OV_FAIL	V5P1_UV_FAIL	V5P2_OV_FAIL	V5P2_UV_FAIL	1V2x_OV_FAIL	1V2x_UV_FAIL	P
									1	1	1	1	1	1	1	

V5POK_UV_FAIL	V5-POK5V Undervoltage Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

V5P1_UV_FAIL	V5P1 Undervoltage Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

V5P2_UV_FAIL	V5P2 Undervoltage Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

1V2x_UV_FAIL	1V2x Undervoltage Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

V5P1_OV_FAIL	V5P1 Overvoltage Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

V5P2_OV_FAIL	V5P2 Overvoltage Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

1V2x_OV_FAIL	1V2x Overvoltage Self-Test Result Flag	
0	Self-test passed	
1	Self-test failed	Default

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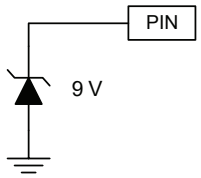
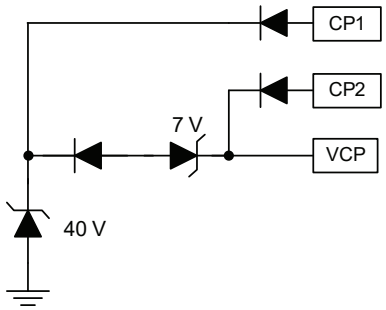
INPUT/OUTPUT STRUCTURES

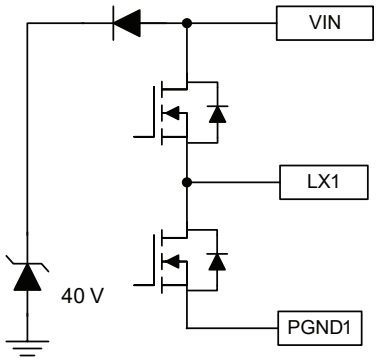
FFn, NPOR, 3V3, V5, 1V2x, ENB, COMP1, COMP2, WDIN, WDENn, VCC, VIGN-OUT, POK5V, LSOUTx, SNSxO, SNSxFB, SNSxR, SDO, SDI, SCK, STRn



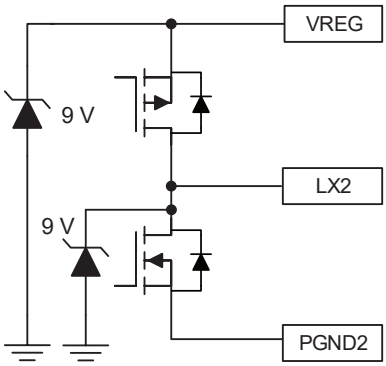
VCP, CP1, CP2



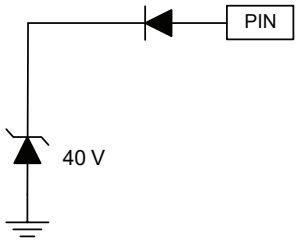
VIN, LX1



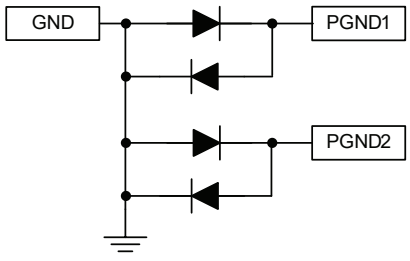
VREG, LX2



V5P1, V5P2, VIGN-IN, ENBAT, SNSVIN, SNSxP, SNSxN, LSINx



GND, PGND1, PGND2



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PCB LAYOUT GUIDELINES

1. Place the ceramic input capacitors as close as possible to the VIN pins and ground the capacitors at the PGND1 pin. In general, the smaller capacitors (0402, 0603) must be placed very close to the VIN pin. The larger ceramic capacitors should be placed within 0.5 inches of the VIN pin. There must not be any vias between the input capacitors and the VIN pins.
2. Place the pre-regulator (VREG) output inductor (L1) as close as possible to the LX1 pins. The inductor and the IC must be on the same layer. Connect the LX1 pins to the inductor with a relatively wide trace or polygon. For EMI/EMC reasons, it is best to minimize the area of this trace/polygon. Also, keep low-level analog signals (like COMP1) away from LX1.
3. Place the pre-regulator (VREG) output ceramic capacitors (COUT) relatively close to the output inductor and the IC. Ideally, the output capacitors, output inductor, and the IC should be on the same layer. The output capacitors must use a ground place to make a very low-inductance connection back to the PGND1 pin. There must be 1 or 2 smaller ceramic capacitors as close as possible to the VREG pin.
4. The two charge pump capacitors must be placed as close as possible to VCP and CP1/CP2.
5. Place the COMP1 network (CZ1, RZ1, and CP1) as close as possible to the COMP1 pin. Place vias to the GND plane as close as possible to these components.
6. The synchronous buck (1V2x) output inductor (L2) should be located near the LX2 pins. The trace from the LX2 pins to the output inductor (L2) should be relatively wide and preferably on the same layer as the IC. The output capacitors should be located near the load. The output voltage sense trace (to 1V2x) must connect at the load for the best regulation.
7. Place the COMP2 network (CZ2, RZ2, and CP2) as close as possible to the COMP2 pin. Place vias to the GND plane as close as possible to these components.
8. The ceramic capacitors for the LDOs (V5, 3V3, V5P1, and V5P2) must be placed near their output pins. The V5P1/V5P2 output must have a 1 A/40 V Schottky diode (or equivalent) located very close to its pin to limit negative voltages.
9. The VCC bypass capacitor must be placed very close to the VCC pin.
10. The thermal pad under the ARG81403 must connect to the ground plane(s) with multiple vias. More vias will ensure the lowest junction temperature and highest efficiency.

ALLEGRO microsystems

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use
(Reference DWG-0000386, Rev. 4, JEDEC MS-026BCDHD)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown

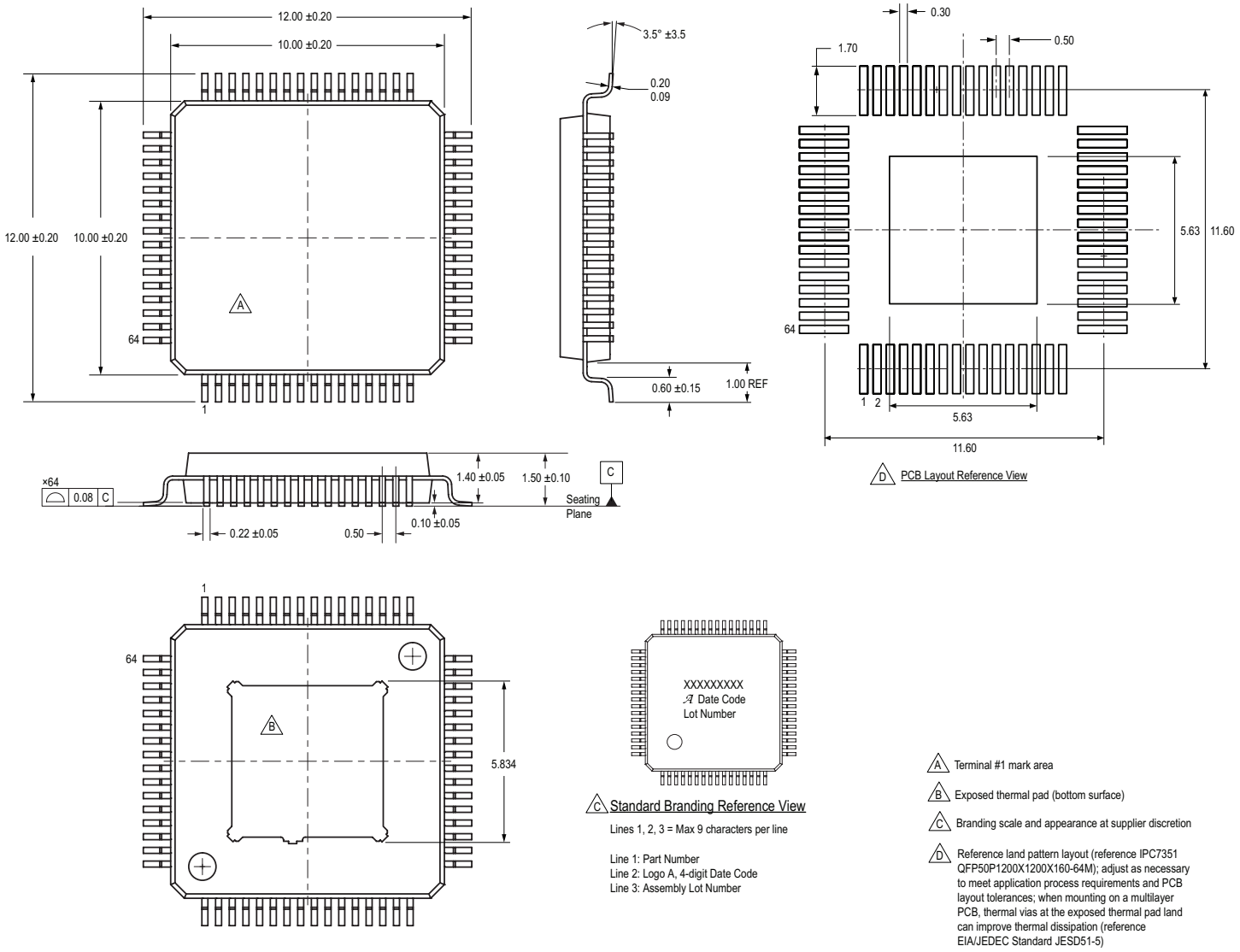

Figure 30: Package JB, 64-Pin QFP

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Revision History

Number	Date	Description
–	June 30, 2021	Initial release

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