CT4022 and CT4032

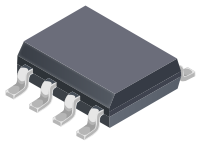
XtremeSense™ TMR Current Sensor
with High dV/dt Immunity and Common-Mode Field Rejection

FEATURES AND BENEFITS

- High operating 500 kHz bandwidth for fast control loops or where high-speed currents are monitored
- High performance for optimized energy applications
  - Ratiometric operation with V_{REF} output
  - Differential sensing rejects common-mode fields
  - No magnetic hysteresis
- 3.3 V or 5 V supply voltage variants
- Low 1 mΩ primary conductor resistance for low power dissipation and high-inrush current capability
- Optimized for high dV/dt applications
- UL 62368-1 (edition 3) certification (pending), highly isolated compact surface mount packages
- High-withstand surge power ratings
- Wide operating temperature, –40°C to 125°C
- Available in SOIC-8 (CT4022) and SOICW-16 (CT4032) packages
- AEC-Q100 Grade 1, automotive qualified (-A variants only)

PACKAGE

8-pin SOIC (SOIC-8)



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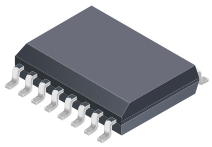
16-pin SOICW (SOICW-16)



Not to scale

DESCRIPTION

The CT4022/32 is a highly linear, XtremeSense™ TMR-based current sensor. The tunneling magnetoresistive (TMR) sensor is differential, which enables common-mode field rejection to cancel out stray magnetic fields. The primary conductor resistance is only 1 mΩ, which enables the sensor to withstand high inrush current and to minimize power loss. The current applied to the pin of the primary conductor generates an internal differential magnetic field. The TMR sensor provides a proportional voltage to the differential magnetic field while rejecting common-mode stray magnetic fields.

The pins of the primary conductive path and the sensor leads are galvanically isolated. This enables high-side current sensing without the need for additional isolation techniques.

The CT4022/32 is offered in an industry-standard 8-pin small-outline integrated circuit (SOIC) package (CT4022) and a 16-pin wide SOIC (SOICW) package (CT4032). Both packages are green and RoHS compliant. The small and low-profile footprint are well-suited for space-constrained applications.

APPLICATIONS

- Motor control
- Power inverters
- Uninterruptible power supply (UPS), switched-mode power supply (SMPS), and telecom power supply
- Consumer and enterprise electronics

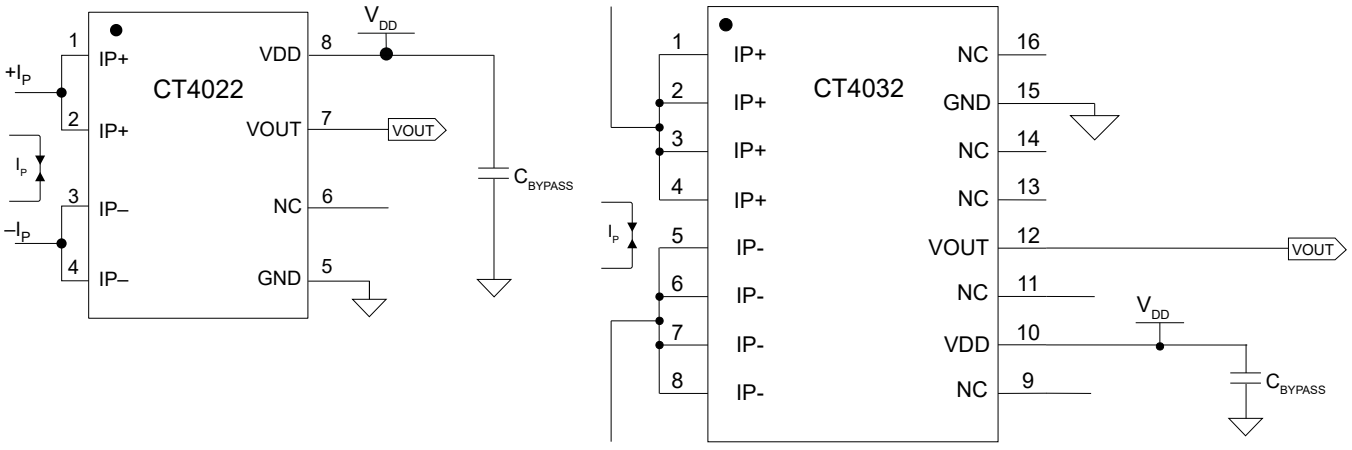


Figure 1: Typical Application Circuit of CT4022 (left) and CT4032 (right)

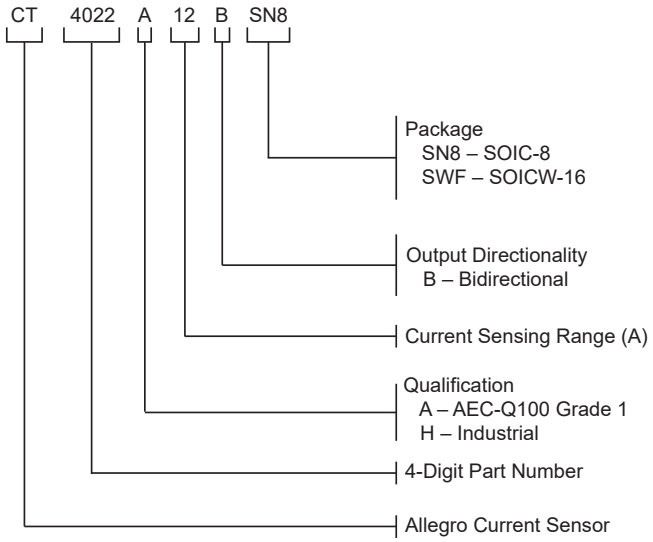
The CT4022/32 outputs an analog signal, V_{OUT}, that varies linearly with the primary current, I_P , within the specified ranges.

SELECTION GUIDE

Part Number	Current Sensing Range (A)	Sensitivity (mV/A)		Quiescent Voltage Output V_{QVO} (V)		Optimized Temperature Range T_A (°C)	Packing
		V_{DD} = 3.3 V	V_{DD} = 5 V	V_{DD} = 3.3 V	V_{DD} = 5 V		
CT4022 (SOIC-8 PACKAGE)							
-A VARIANT							
CT4022-A12BSN8 [1]	±12	110	166.7	1.65	2.5	–40 to 125	2000 pieces per 13-inch reel
CT4022-A24BSN8 [1]	±24	55	83.3				
CT4022-A40BSN8 [1]	±40	33	50				
CT4022-A50BSN8 [1]	±50	26.4	40				
CT4022-A65BSN8 [1]	±65	20.3	30.8				
-H VARIANT							
CT4022-H12BSN8	±12	110	166.7	1.65	2.5	–40 to 125	2000 pieces per 13-inch reel
CT4022-H24BSN8	±24	55	83.3				
CT4022-H40BSN8	±40	33	50				
CT4022-H50BSN8	±50	26.4	40				
CT4022-H65BSN8	±65	20.3	30.8				
CT4032 (SOICW-16 PACKAGE)							
-A VARIANT							
CT4032-A20BSWF [1]	±20	66	100	1.65	2.5	–40 to 125	1000 pieces per 13-inch reel
CT4032-A40BSWF [1]	±40	33	50				
CT4032-A50BSWF [1]	±50	26.4	40				
CT4032-A65BSWF [1]	±65	20.3	30.8				

[1] AEC-Q100 Grade 1, automotive grade (-A variants only).

PART NAMING SPECIFICATION



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ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Min.	Max.	Unit
Supply Voltage	V_{DD}		–0.3	6.0	V
Output Voltage	V_O	Applies to VOUT	–0.3	(V_{DD}+0.3)<6	V
Input Current	I_P	A current above this value can cause a permanent drift in sensitivity and quiescent output voltage beyond the limits of the datasheet.	–	150	A
Operating Ambient Temperature	T_A		–40	125	°C
Storage Temperature	T_{STG}		–65	155	°C
Maximum Junction Temperature	$T_{J(MAX)}$		–	165	°C

[1] Stresses that exceed those listed in the absolute maximum ratings might cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions that exceed those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods might affect device reliability.

PACKAGE CHARACTERISTICS

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Internal Conductor Resistance	R_{IC}	T_A = 25°C, CT4022	–	1	–	mΩ
		T_A = 25°C, CT4032	–	1	–	mΩ
Internal Conductor Inductance	L_{IC}	T_A = 25°C, CT4022	–	4.2	–	nH
		T_A = 25°C, CT4032	–	5	–	nH
Moisture Sensitivity Level	MSL	Per IPC/JEDEC J-STD-020	–	3	–	–

CT4022 (SOIC-8) ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Withstand Strength [1][2]	V_{ISO}	Agency rated for 60 seconds per UL 62368-1 (edition 3)	3500	V_{RMS}
Working Voltage for Basic Isolation [2]	V_{WVBI}	Maximum approved working voltage for basic (single) isolation according to UL 62368-1 (edition 3)	1280	$V_{PK\ or}\ V_{DC}$
			905	V_{RMS}
Working Voltage for Reinforced Isolation [2]	V_{WVRI}	Maximum approved working voltage for reinforced isolation according to UL 62368-1 (edition 3)	717	$V_{PK\ or}\ V_{DC}$
			507	V_{RMS}
Surge Voltage	V_{SURGE}	1.2 µs/50 µs waveform, tested in dielectric fluid to determine the intrinsic surge immunity of the isolation barrier	13000	V_{PK}
Impulse Voltage	$V_{IMPULSE}$	1.2 µs/50 µs waveform, tested in air	5000	V_{PK}
Clearance	D_{CL}	Minimum distance through air from IP leads to signal leads	4.1	mm
Creepage	D_{CR}	Minimum distance along package body from IP leads to signal leads	4.1	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	110	µm
Comparative Tracking Index	CTI	Material Group II	400 to 599	V

[1] Production tested for 1 second in accordance with UL 62368-1 (edition 3).
[2] Certification pending.

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CT4032 (SOICW-16) ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Withstand Strength [1][2]	V_{ISO}	Agency rated for 60 seconds per UL 62368-1 (edition 3)	5000	V_{RMS}
Working Voltage for Basic Isolation [2]	V_{WVBI}	Maximum approved working voltage for basic (single) isolation according to UL 62368-1 (edition 3)	1550	$V_{PK\ or}\ V_{DC}$
			1097	V_{RMS}
Working Voltage for Reinforced Isolation [2]	V_{WVRI}	Maximum approved working voltage for reinforced isolation according to UL 62368-1 (edition 3)	800	$V_{PK\ or}\ V_{DC}$
			565	V_{RMS}
Surge Voltage	V_{SURGE}	1.2 µs/50 µs waveform, tested in dielectric fluid to determine the intrinsic surge immunity of the isolation barrier	10000	V_{PK}
Impulse Voltage	$V_{IMPULSE}$	1.2 µs/50 µs waveform, tested in air	7071	V_{PK}
Clearance	D_{CL}	Minimum distance through air from IP leads to signal leads	8	mm
Creepage	D_{CR}	Minimum distance along package body from IP leads to signal leads	8	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	110	µm
Comparative Tracking Index	CTI	Material Group II	400 to 599	V

[1] Production tested for 1 second in accordance with UL 62368-1 (edition 3).
[2] Certification pending.

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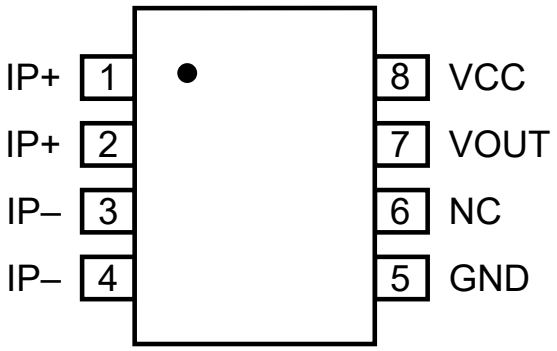
PINOUT DIAGRAM AND TERMINAL LIST TABLE

CT4022 (SOIC-8)

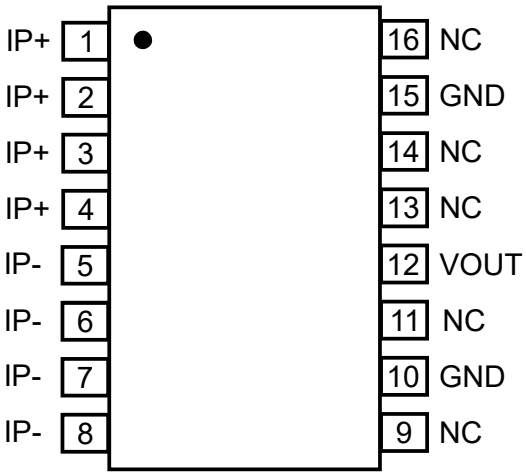
Terminal List for CT4022

Number	Name	Function
1, 2	IP+	Positive terminal for current being sensed
3, 4	IP–	Negative terminal for current being sensed
5	GND	Device ground terminal
6	NC	No connect; GND for optimal ESD performance
7	VOUT	Analog output voltage
8	VDD	Device power supply terminal



8-Pin SOIC Pinout Diagram (top-down view)

CT4032 (SOICW-16)



16-Pin SOICW Pinout Diagram (top-down view)

Terminal List for CT4032

Number	Name	Function
1, 2, 3, 4	IP+	Positive terminal for current being sensed
5, 6, 7, 8	IP–	Negative terminal for current being sensed
9	NC	No connect; GND for optimal ESD performance
10	VDD	Device power supply terminal
11	NC	No connect; GND for optimal ESD performance
12	VOUT	Analog output voltage
13, 14	NC	No connect; GND for optimal ESD performance
15	GND	Device ground terminal
16	NC	No connect; GND for optimal ESD performance

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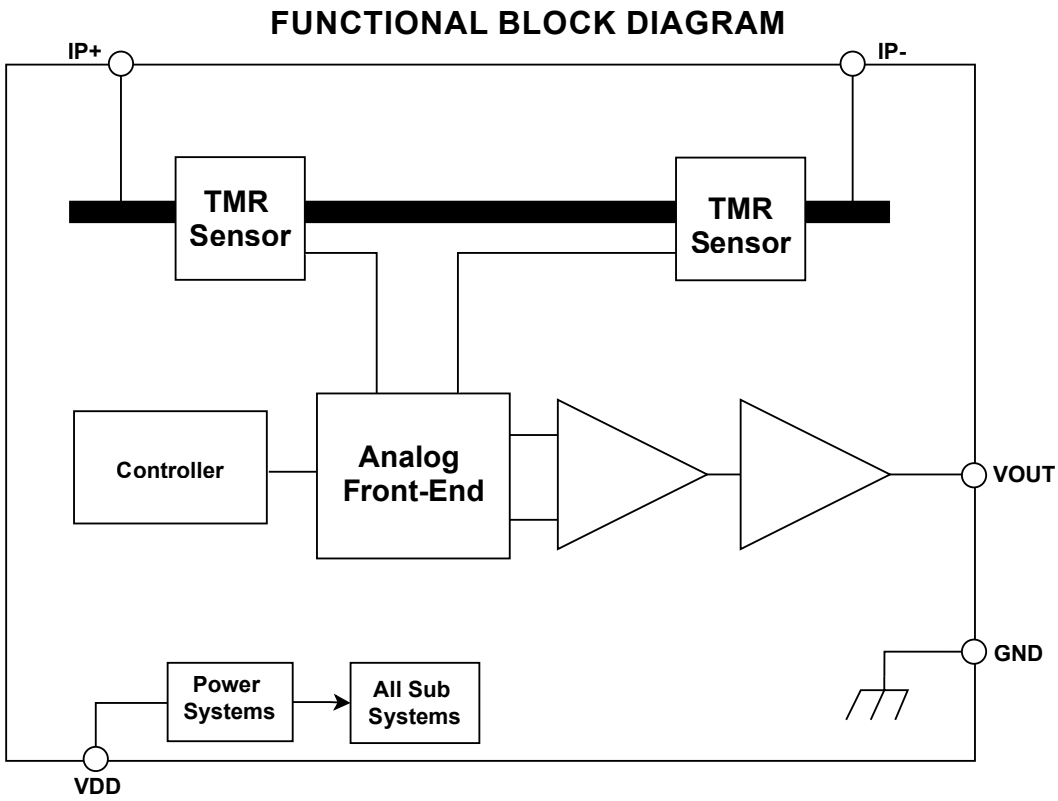

Figure 2: Functional Block Diagram

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NOTE: This is a short-form datasheet for preview purposes. Pages 7–21 have been removed. Contact Allegro MicroSystems to request a complete datasheet.

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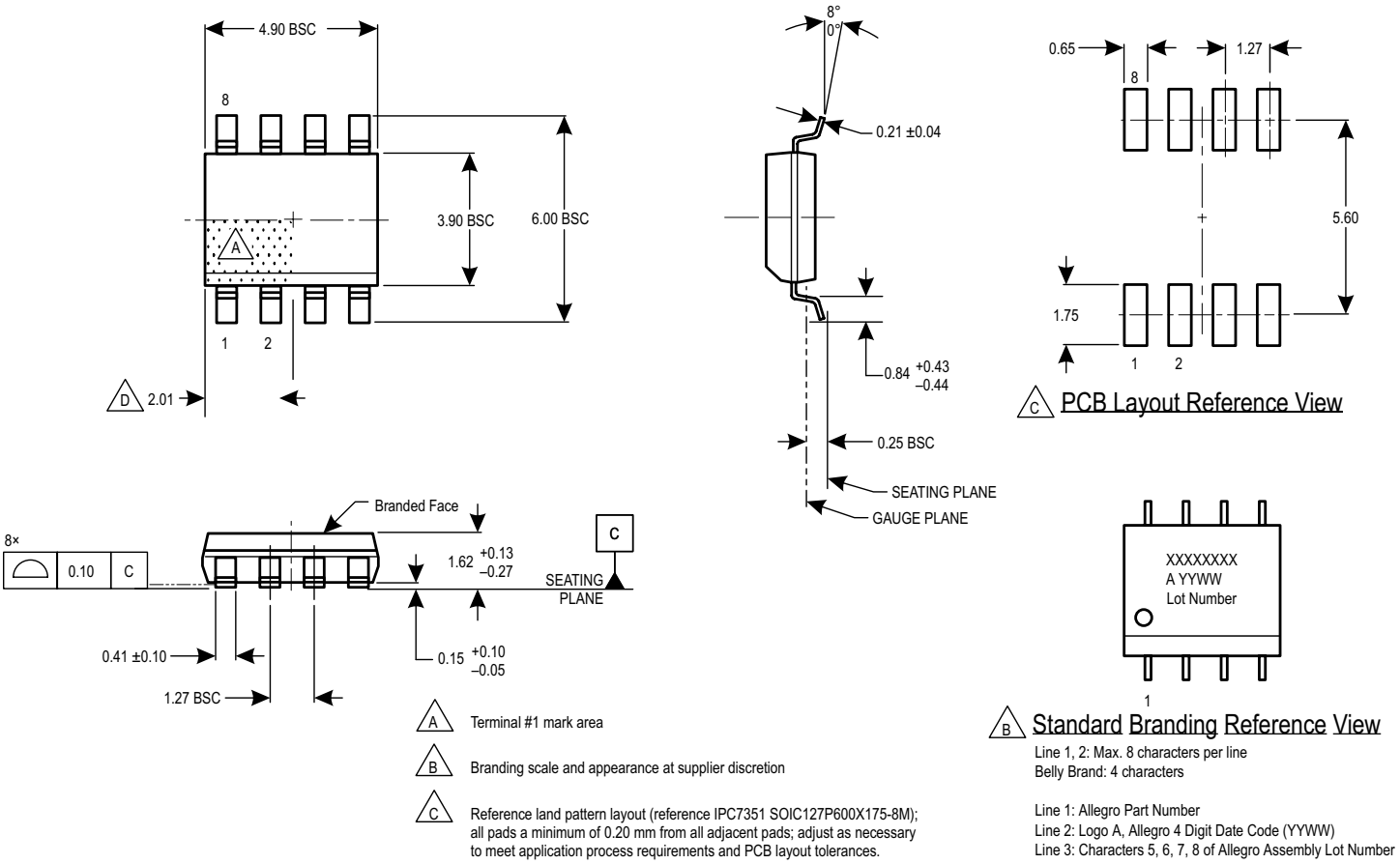
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(reference Allegro DWG-0000385, Rev. 2 or JEDEC MS-012AA)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Branding scale and appearance at supplier discretion

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances.

Line 1, 2: Max. 8 characters per line
Belly Brand: 4 characters

Line 1: Allegro Part Number
Line 2: Logo A, Allegro 4 Digit Date Code (YYWW)
Line 3: Characters 5, 6, 7, 8 of Allegro Assembly Lot Number

Figure 7: SOIC-8 Package Drawing and Dimensions

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For Reference Only – Not for Tooling Use
(Reference MS-013AA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

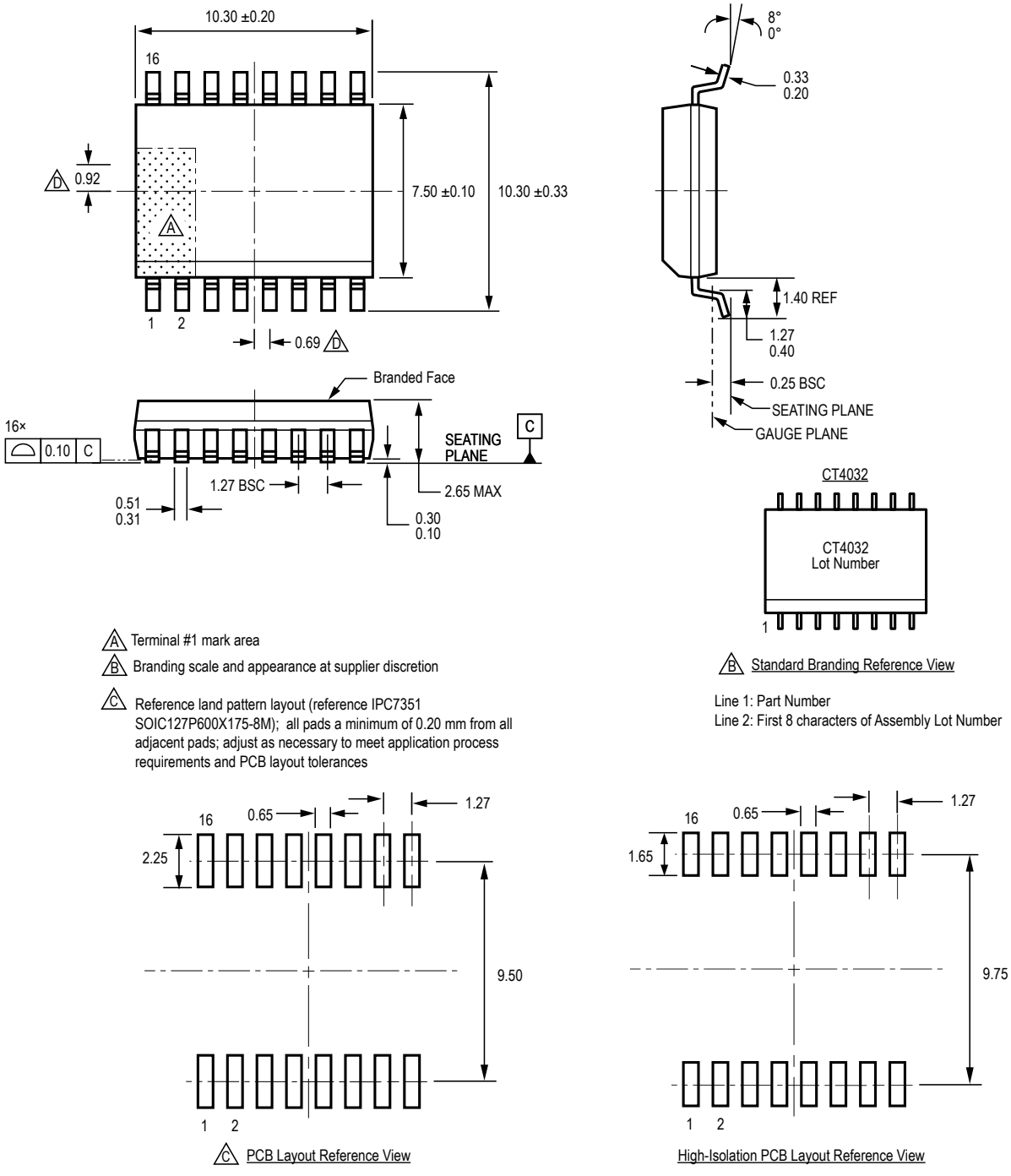

Figure 8: SOICW-16 Package Drawing and Dimensions

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Revision History

Number	Date	Description
–	March 18, 2025	Initial release

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