



Demo Note for the A8583 Evaluation Board

**4.7V_{IN} – 40V_{IN}, 3.3V_{OUT}, 3.5A, 2MHz
Asynchronous Buck Regulator**



GENERAL SPECIFICATIONS

Specification	Min	Nom	Max	Units
Absolute Maximum Input Voltage	-0.3	—	40	Volts
Operating Input Voltage Range	4.7	12	36	Volts
V _{IN} START Threshold, V _{IN} rising	—	4.2	4.6	Volts
V _{IN} STOP Threshold, V _{IN} falling	—	3.8	4.2	Volts
Output Voltage (FB: 5.23K/16.5K, ±1%)	3.20	3.32	3.44	Volts
Steady-State Output Current (12V _{IN})	—	3.5	4.0	A
Pulse-by-pulse Current Limit	4.75	—	6.25	A
Enable/Synchronization Input	-0.3	—	5.5	Volts

OPERATING INSTRUCTIONS

Input Power Connection:

Connect a 12V power supply from Vin to GND that is capable of at least 3A. **Once operational, V_{IN} can fall as low as 3.8V_{TYP} (4.2V_{MAX}) before the A8583 is reset.**

Enable Input Connection:

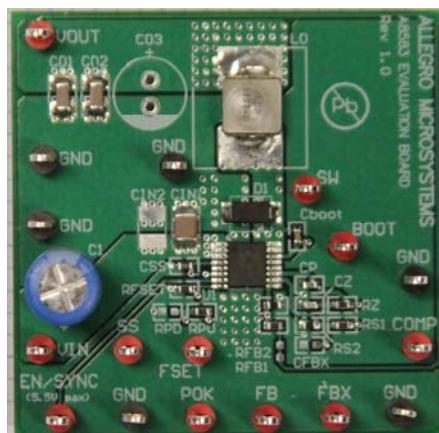
Connect an Enable signal from EN/SYNC to GND. If the EN/SYNC input voltage is higher than 1.8V the A8583 will be enabled. If the EN/SYNC input voltage is lower than 0.8V the A8583 will be disabled. Also, EN/SYNC may be used to simultaneously enable the A8583 and synchronize the PWM switching frequency by applying a square wave above 2.2MHz.

Note: Continuously applying more than 5.5V to the EN/SYNC pin may damage the A8583.

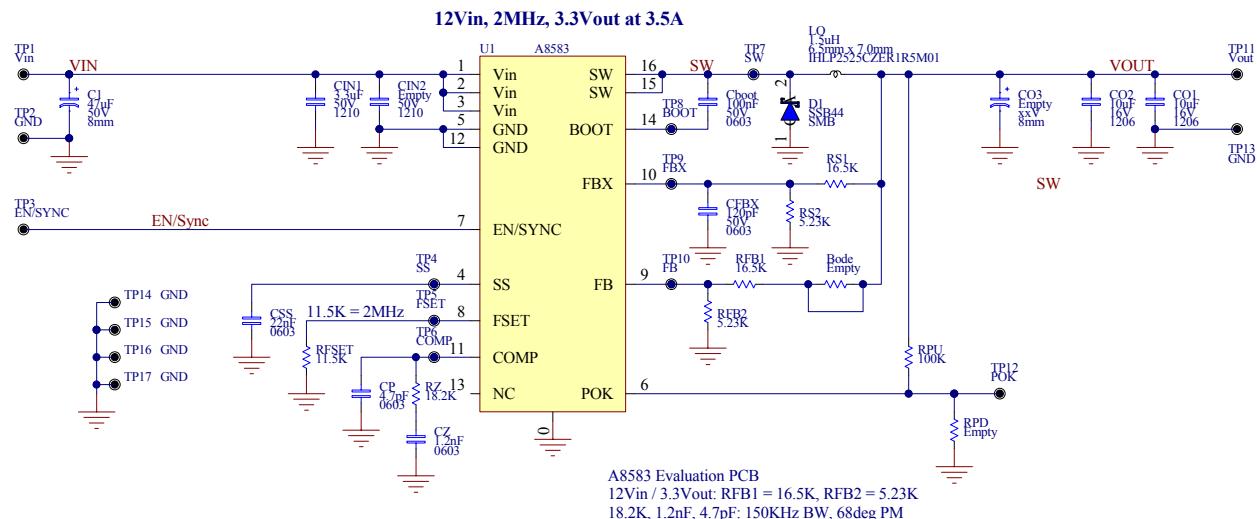
Output Load Connections:

Connect a load from V_{OUT} to GND. The steady-state load current can be as high as 3.5A. Pulse-by-pulse current limit and/or thermal shutdown will occur if the load is greater than 4.75A.

DEMO BOARD PICTURE



DEMO BOARD SCHEMATIC

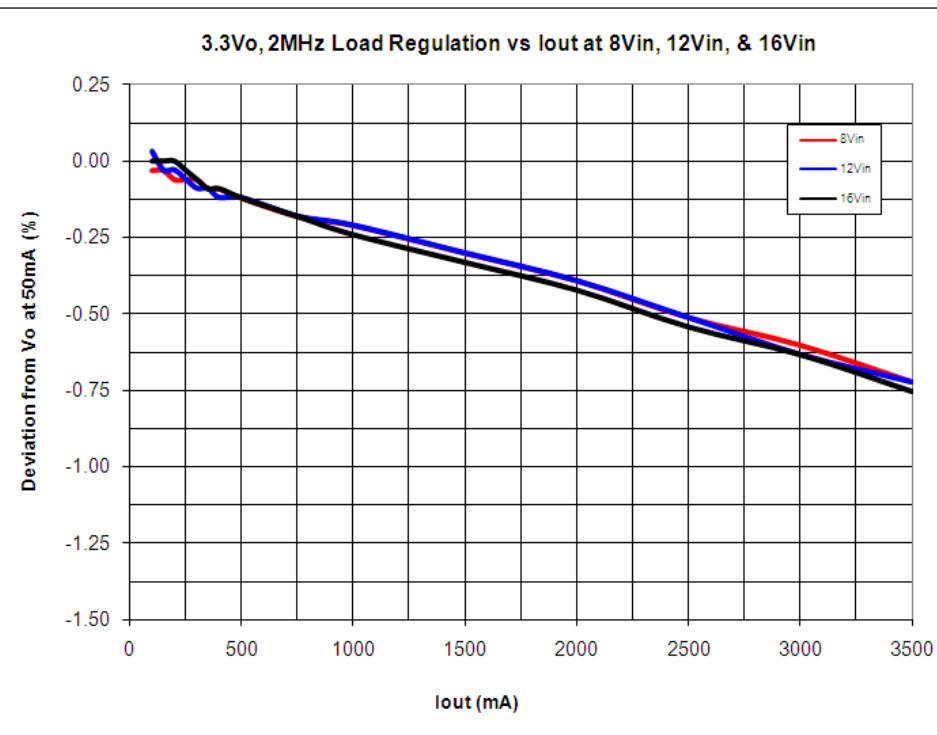
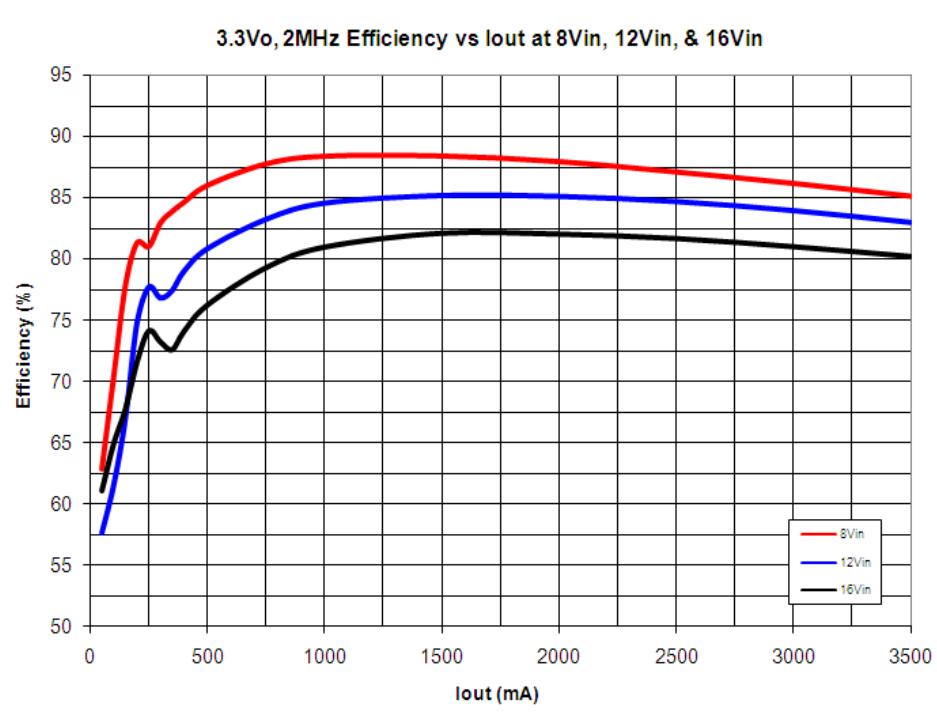


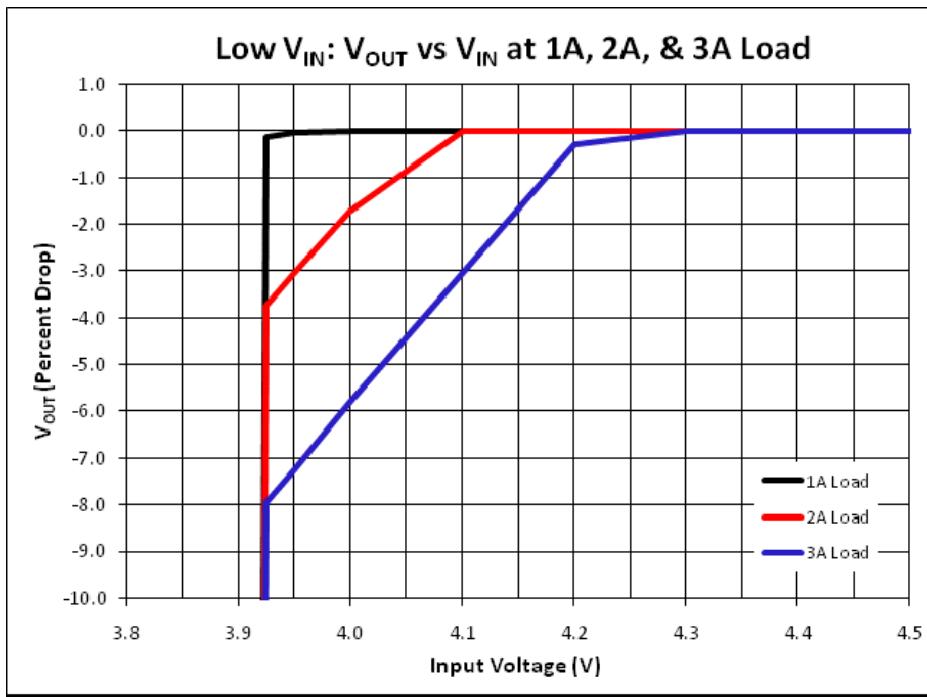
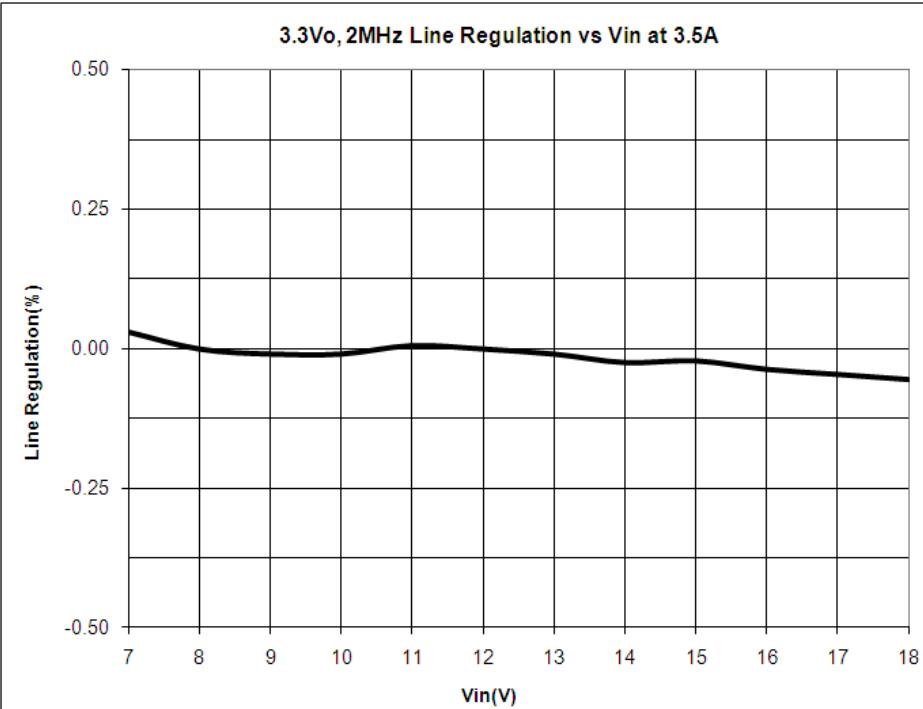
Note: C1 is an optional, bulk, electrolytic capacitor for general supply filtering

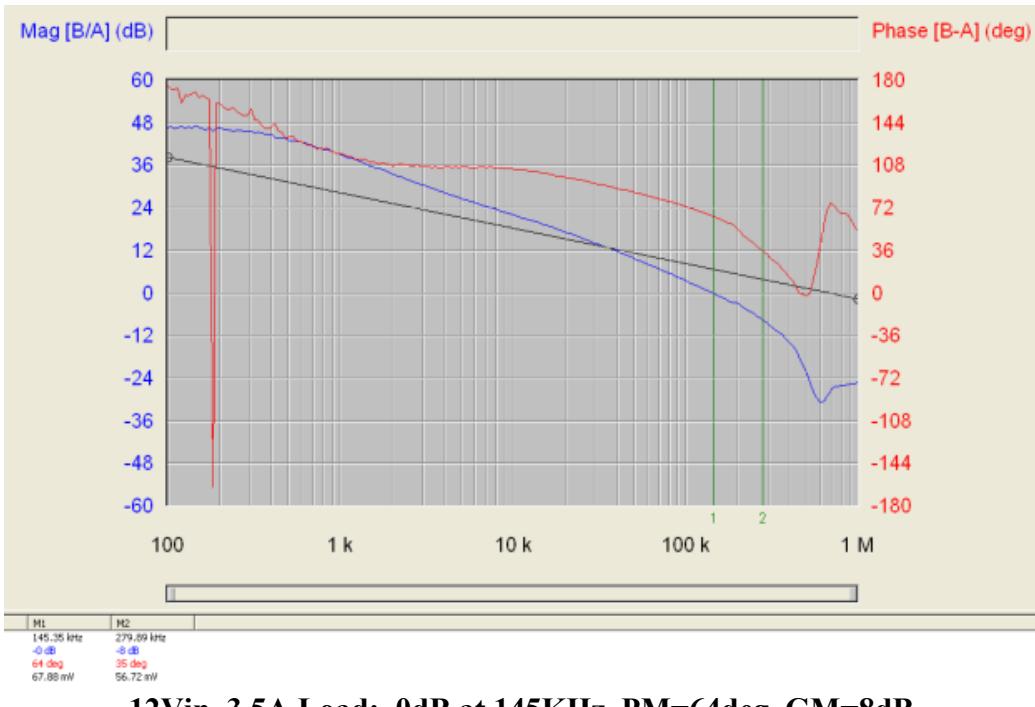
DEMO BOARD BILL-OF-MATERIALS

REFERENCE DESIGNATORS	DESCRIPTION	FOOTPRINT	QTY.	MANUFACTURER	MANUFACTURER P/N	SOURCE	PURCHASE P/N
PCB	A8583 EVAL PCB for eTSSOP16, Rev 1.0	N/A	1	Allegro MicroSystems		4pcb.com	
U1	A8583, 3.5A Buck Regulator	eTSSOP-16	1	Allegro MicroSystems	A8583		
RFB1, RS1	Resistor, 16.5Kohms, 1/10W, 1%	0603	2				
RFB2, RS2	Resistor, 5.23Kohms, 1/10W, 1%	0603	2				
RFSET	Resistor, 11.5Kohms, 1/10W, 1%	0603	1				
RZ	Resistor, 18.2Kohms, 1/10W, 1%	0603	1				
RPU	Resistor, 100Kohms, 1/10W, 1%	0603	1				
C1	Capacitor, Electrolytic, 47uF, 50V, 0.35ohms, 440mArms, -40degC to 125degC	Thru Hole 8mm x 11.5mm	1	Nichicon	UBT1H470MPD	Mouser	647-UBT1H470MPD
CIN1	Capacitor, Ceramic, 3.3uF, 50V, 10% or 20%, X5R or X7R, -55degC to 125degC	1210 part, 1210 pads	1	TDK	C3225X7R1H335M or C3225X7R1H335K	Digikey	445-1432-1-ND 445-3936-1-ND
CIN2	Empty	1210	0				
CO1, CO2	Capacitor, Ceramic, 10uF, 16V, 10%, X7R, -55degC to 125degC	1206 part, 1210 pads	2	TDK	C3216X7R1C106K	Digikey	445-4042-1-ND
CBOOT	Capacitor, Ceramic, 0.1uF, 50V, 10%, X7R	0603	1				
CSS	Capacitor, Ceramic, 22nF, 25V, 10%, X7R	0603	1				
CZ	Capacitor, Ceramic, 1.2nF, 50V, 10%, X7R	0603	1				
CP	Capacitor, Ceramic, 4.7pF, 50V, 10%, X7R	0603	1				
CFBX	Capacitor, Ceramic, 120pF, 50V, 10%, X7R	0603	1				
CO3, CO4, CO5, CIN3, CIN4, CSNUB, RSNUB, RPD, LX	Empty	Various	0				
D1	Diode, Schottky, 4A, 40V	SMB	1	Vishay	SSB44-E3/52T	Digikey Mouser	SSB44-E3/52TGICT-ND 625-SSB44-E3
LO	Inductor, SMT, 1.5uH, 15mohms max, 18Asat	6.5mm x 7mm 3mm thick	1	Vishay	IHLP2525CZER1R5M01	Digikey Mouser	541-1007-1-ND 70-IHLP2525CZER1R5M1
VIN, EN/SYNC, SS, FSET, COMP, SW, BOOT, FBX, FB, POK, VOUT	Test Points, Red, 0.063" diameter	0.063"	11	Keystone	5010	Digikey	5010K-ND
GND	Test Points, Black, 0.063" diameter	0.063"	6	Keystone	5011	Digikey	5011K-ND
Rubber Feet	Self stick rubber feet	Clear	4	3M	SJ-5303 (CLEAR)	Digikey	SJ5303-7-ND

DEMO BOARD PERFORMANCE





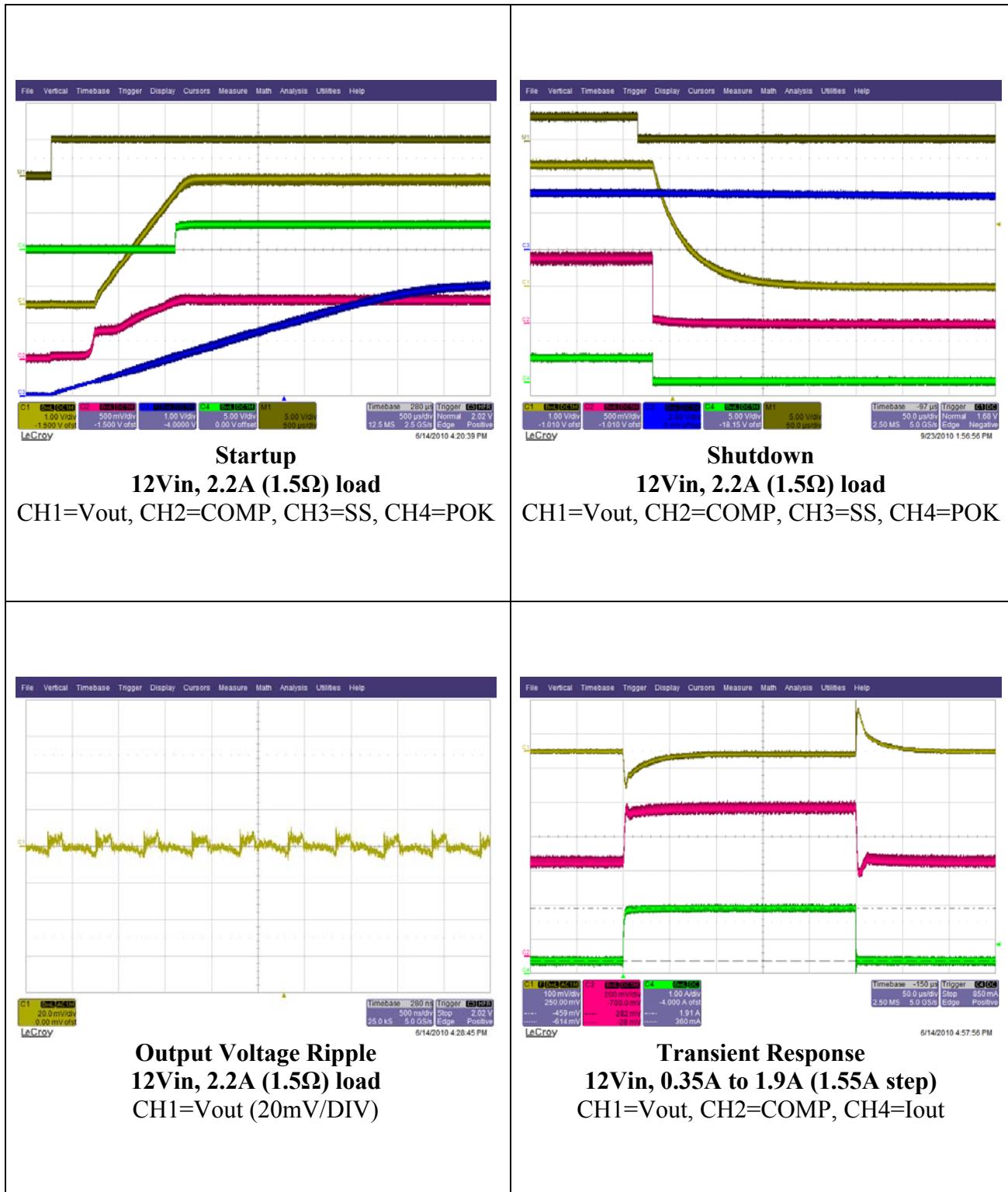


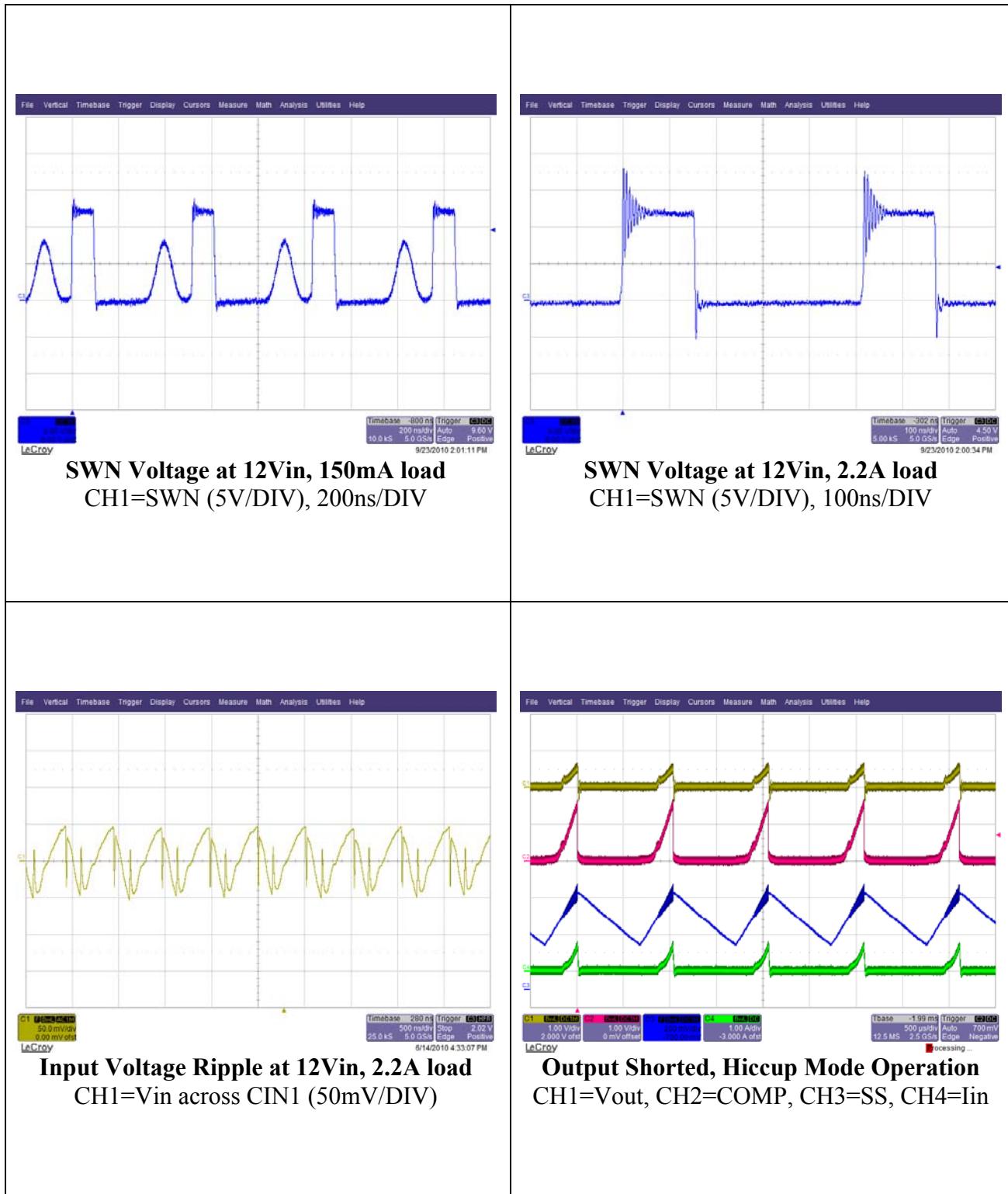
Iout (A)	A8583 (deg C)	D1 (deg C)	Lo (deg C)
0.5	32.3	32.9	30.4
1.0	36.2	39.5	34.2
1.5	40.6	46.5	38.6
2.0	47.2	55.3	44.5
2.5	54.4	66.3	51.4
3.5	73.5	91.1	67.3
Shorted Vout	30.8	34.7	29.5

Component Temperatures vs Load Current

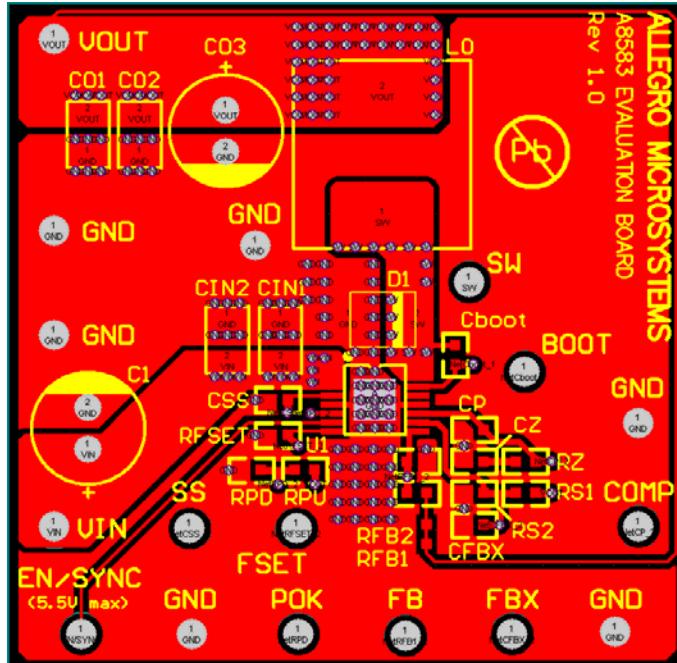
12Vin, 3.3Vout, 2MHz, T_{AMB}=25deg C

No Airflow (still air)

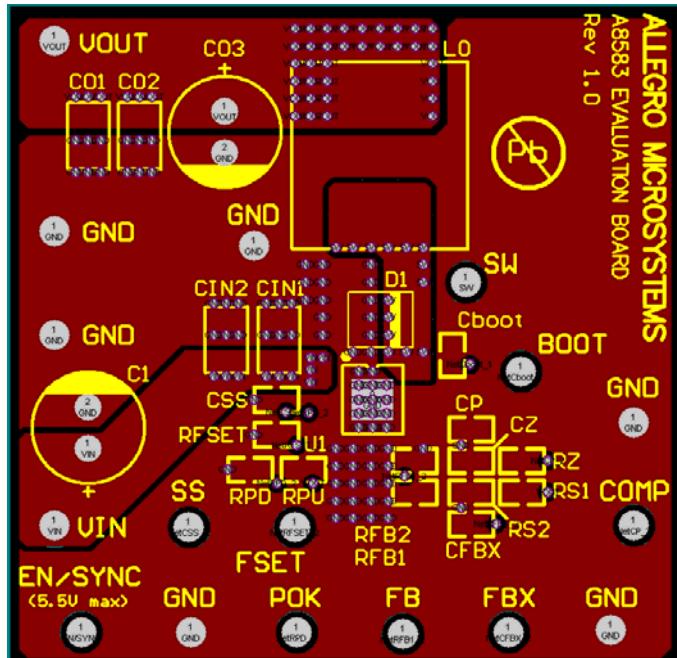




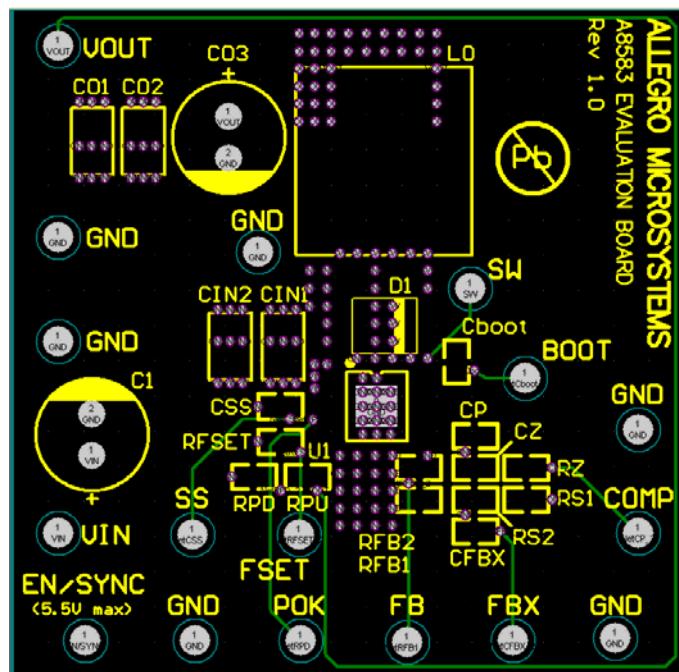
DEMO PCB LAYOUT:



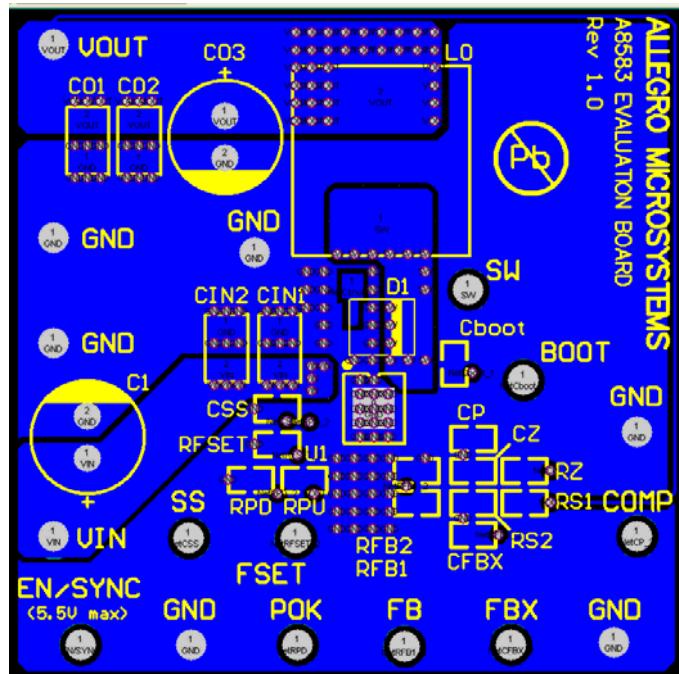
Top Layer and Top Silk



Layer 2 and Top Silk



Layer 3 and Top Silk



Bottom Layer and Top Silk