ASEK71240, Board, Demo, SOIC8, Bare Board

TED-0002524-FAB
Originator: S. Upton

FAB Drawing / FAB Notes and Requirements

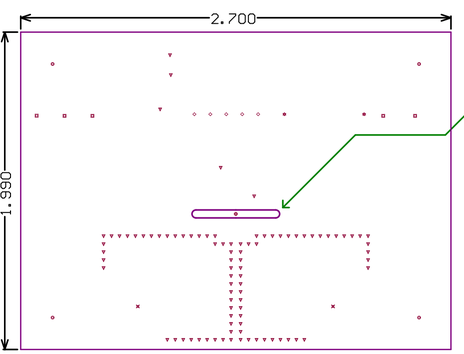
Rev 2
10/18/2018

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
	1	50.00mil (1.270mm)	NPTH	Slot
	2	56.00mil (1.422mm)	PTH	Round
	2	266.00mil (6.756mm)	PTH	Round
	4	125.00mil (3.175mm)	PTH	Round
	5	42.00mil (1.067mm)	PTH	Round
	5	62.00mil (1.575mm)	PTH	Round
	89	15.00mil (0.381mm)	PTH	Round
	108 Total			

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

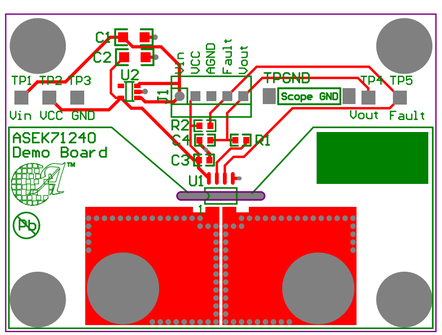
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	TopPaste				
2	TopOverlay				
3	TopSolder	Solder Resist	0.40mil	3.5	
4	TopLayer	Copper	5.60mil		
5	Dielectric1	FR-4	50.80mil	4	
6	BottomLayer	Copper	5.60mil		
7	BottomSolder	Solder Resist	0.40mil	3.5	
8	BottomOverlay				
9	BottomPaste				

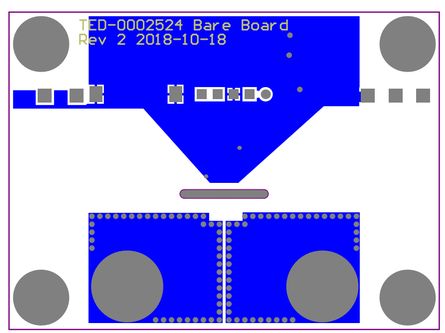
Mechanical Layer 1 *.gm1 is Board Outline, slots and circular cutouts
Mechanical Layer 2 *.gm2 is footprint notes (not for fab house)
Mechanical Layer 3 *.gm3 is hole location guide
Mechanical Layer 4 *.gm4 is board outline dimensions
Mechanical Layer 5 *.gm5 is topside labels (if no silk)
Mechanical Layer 6 *.gm6 is bottomside labels (if no silk)
Mechanical Layer 7 *.gm7 is FAB drawing notes
Mechanical Layer 8 *.gm8 is top selective hard gold
Mechanical Layer 9 *.gm9 is bottom selective hard gold
Mechanical Layer 10 and up are not for usage by PCB board house
*.gto and *.gbo are top and bottom layer silkscreen (aka overlay)
*.gts and *.gbs are top and bottom soldermask
*.drl is NC Drill
*.apr is aperature file
*.gpb and *.gpt are pad master layers, and are not used (ignore if in zip file)
Keepout layer *.gko is for internal usage only, and is not to be used by board house



50mil wide slot to be milled here
Feature is on mech1 layer
Slot shall not be plated. Plating not allowed

1. Finished PCB is RoHS
2. Dimensions are in inches, unless otherwise noted.
3. Applicable Standards:
   3a. Manufacture in accordance to IPC-6011, IPC-6012 for Class 2 applications.
   3b. PCB shall meet acceptance criteria as required for Class 2 PCB as defined in IPC-600
   3c. UL Approved to a minimum catagory of 94V0.
4. Laminate:
   4a. Thickness: 0.062inch +/- 10%
   4b. Type: high temp FR4
   4c. This line left blank
   4d. Core/prepreg thickness:
      4d.1. See chart to left.
      4d.2. Core/prepreg thicknesses to be roughly uniform thickness or +/-5mil from indicated
      4d.3. No impedance controlled stackup required
5. Copper:
   5a. Layer Count: 2
   5b. Finish copper layers to thickness shown in stackup table.
   5c. This line left intentionally blank.
   5d. Plated through holes: plate to 1mil min copper thickness
   5e. Trace separation: 10mil
   5f. Trace min width: 6mil
   5g. Line width reduction due to pinholes nicks or shrinking: 20% max.
   5h. No impedance controlled route used; no trace width adjustment required.
6. If PCB has regions where more than 1 square inch of soldermask is removed:
   6a. All PCB lands in this region (square and round) are to be 100% pristine.
   6b. Lands outside this region may remain at 80% pristine as defined by IPC-6012.
   6c. Board flatness in this region shall not exceed 0.001inch total
7. Total board flatness shall not exceed 0.002inch per inch.
8. Artwork layer registration shall be within 0.003inch total.
9. Surface Finish:
   9a. Immersion Gold
   9b. For all regions covered by mechanical layer 8 or mechanical layer 9 (*.gm8 or *.gm9):
      9b.1. 30microinches Hard gold over 100microinches min low stress nickel
      9b.2. Minimum hard gold hardness to be 130 - 200 knoop.
      9b.3. Mech Layer *.gm8 describes top layer selective gold regions
      9b.4. Mech Layer *.gm9 describes bottom layer selective gold regions
      9b.5. No hard gold required; no *.gm8 nor *.gm9 files provided
10. Soldermask:
   10a. Top/Bottom soldermask required
   10b. Soldermask color shall be green.
   10c. Soldermask finish may be matte or glossy.
11. Silkscreen
   11a. Top/bottom silkscreen required.
   11b. Silkscreen color shall be white.
   11c. Min silkscreen line width: 4mil
   11d. Epoxy or acrylic ink allowed
   11e. Photoimaging or inkject printing shall be used
   11f. Allegro Logo shall be printed as accurately as possible.
      11f1. Silkscreen imperfections in other regions allowed. Do not hold job for minor blemishes elsewhere.
12. Drill holes:
   12a. No blind or buried vias.
   12b. Hole sizes are specified after plating.
   12c. No via in pad used. No via filling required.
13. Mill separate according to mech1 (*.gm1) layer.
14. Electrical testing required.
15. Contact information:
   15a. Shawn Upton supton@allegromicro.com, 603.626.2429
   15b. If fast turn board, 24hr contact info: N/A


C1
C2
U2
J1
Vin
VCC
AGND
Fault
Vout
TP1 TP2 TP3
Vin VCC GND
TPGND
Scope GND
TP4 TP5
Vout Fault
R2
C4
R1
C3
U1
ASEK71240
Demo Board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