ACS37220 EZ Package Evaluation Board User Guide

DESCRIPTION

Evaluation boards offer a method for quickly evaluating Allegro current sensors in a lab environment without needing a custom circuit board. This document describes the use of the EZ current sensor evaluation board. This evaluation board (ACSEVB-EZ7, TED-0004114) is intended for use with the ACS37220 EZ packaged current sensor (custom 7-pin SOIC Allegro current sensor).

FEATURES

- Enhanced thermal performance
  - □ 6-layer PCB with 2 oz copper weight on all layers
  - □ Nonconductive-filled via-in-pad
  - □ High-performance FR4 material with 180°C glass transition temperature
- Flexible layout for user installed connection points
  - □ Standard Keystone test points
  - □ SMA/SMB connector
  - □ 2-pin headers
- Integrated current loop resistance can be measured directly on the evaluation board after test point installation; voltage drop can be measured for approximating power loss in the package.

EVALUATION BOARD CONTENTS

- Printed circuit board with populated components
  - □ Available ACS37220 board variants:
    - ♦ ACSEVB-EZ7-37220-100B3
    - ♦ ACSEVB-EZ7-37220-100B5
    - ♦ ACSEVB-EZ7-37220-150B3
    - ♦ ACSEVB-EZ7-37220-150B5
    - ♦ ACSEVB-EZ7-37220-200B5
- Recommended supporting circuitry for all compatible current sensor are listed in the Supporting Circuitry section below.

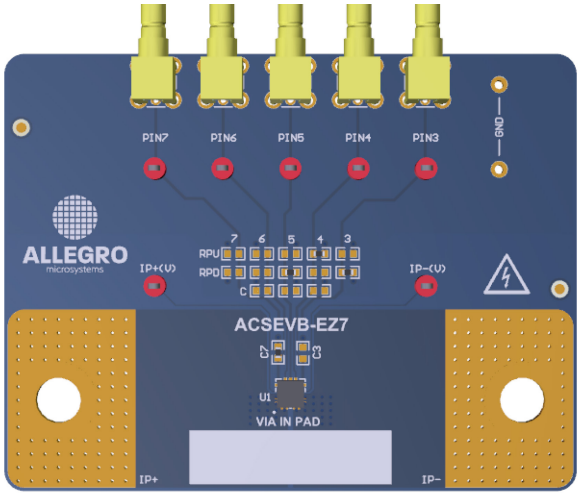


Figure 1: EZ Evaluation Board

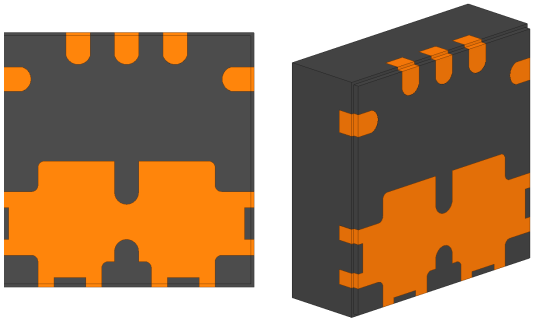


Figure 2: EZ Package

Table of Contents

USING THE EVALUATION BOARD

Evaluation Board Procedure

SETTING UP THE EVALUATION BOARD

Upon receiving the evaluation board, it is up to the user to populate the evaluation board with the desired test points, SMA/SMB connectors, header connectors, and supporting circuitry, as needed.

CONNECTING TO THE EVALUATION BOARD

The most reliable way to connect measurement instruments to the evaluation board is to use SMB/SMA or 2-pin headers connectors along with coaxial cables. This configuration will be most resilient to external coupling and is the most mechanically stable and it is the preferred way for measurement for high-speed signal.

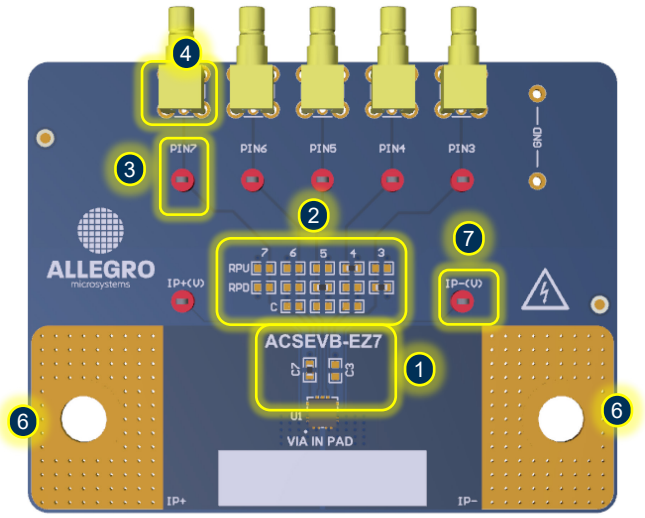
Keystone test points are a convenient way to connect any instrument, but is it recommended for DC setups only.

Evaluation Board Detailed Description

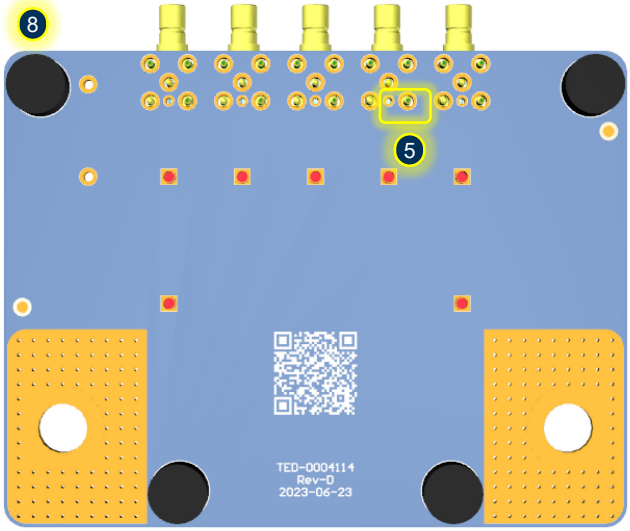
1. U1 is an EZ package footprint (pin 1 is on bottom left side of the package footprint, see the small white dot to the left of the package footprint).
2. U1 pins allow the option to connect:
   - ♦ RPU: pull-up resistor to VCC
   - ♦ RPD: pull-down resistor to GND
   - ♦ C: decoupling or load capacitor to GND

NOTE: All passive components are 0603 package size.

3. Optional through hole test points (Keystone 5005 test points, e.g., Digikey# 36-5005-ND)
4. Optional standard SMB or SMA connection points (e.g., Digikey# 1868-1429-ND)
5. Optional 2-pin 100 mil header connector (note: either SMB or header can be assembled)
6. Primary current cables mounting positions (positive current flow direction is left to right)
7. Optional 2-pin 100 mil header connector for voltage drop measurement across the integrated current loop of the current sensor
8. RB1, RB2, RB3, and RB4: rubber bumper mounting positions (e.g., Digikey# SJ61A6-ND)



Top view



Bottom view

Figure 3: EZ Generic Evaluation Board Reference Image

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

EZ PACKAGE LAYOUT GUIDELINES AND THERMAL PERFORMANCE DATA

Introduction

Self-heating due to the flow of current in the package IP conductor should be considered during the design of any current sensing system. The sensor, printed circuit board (PCB), and contacts to the PCB will generate heat and act as a heat sink as current moves through the system.

Thermal management is important for PCBs that generate a lot of heat, such as current sensors used in high current applications. Heat sinking and other active cooling techniques can be used to dissipate heat away from components, allowing better performance over temperature.

The thermal response is highly dependent on PCB layout, copper thickness, cooling techniques, and the profile of the injected current. The current profile includes peak current value, current on-time, and duty cycle.

Vias-in-Pad and Thermal Management

The thermal performance of the EZ package should be verified by the end user in the specific conditions of the application. The maximum junction temperature, $T_{J(max)}$ (165°C), should not be exceeded. Measuring the temperature of the top of the package is a close approximation of the die temperature.

Placing vias under the copper pads of the Allegro current sensor evaluation board minimizes the current path resistance and improves heatsinking to the PCB, while vias outside of the pads limit the current path to the top of the PCB trace and have worse heatsinking under the part (see Figure 4 and Figure 5 below). The EZ Current Sensor Evaluation Board does include vias in pad and is recommended to improve thermal performance. See Figure 6 showing the top layer of the EZ evaluation board. This evaluation board is 6 layers with 2-ounce copper (Cu).

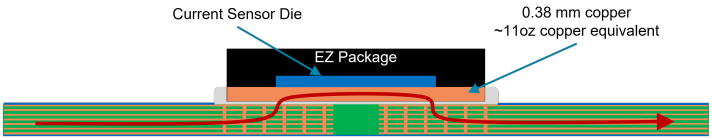


Figure 4: Vias Under Copper Pads

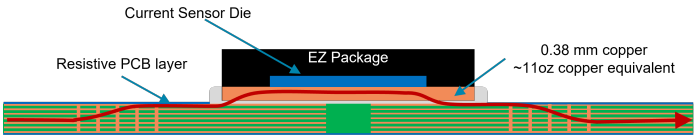


Figure 5: No Vias Under Copper Pads

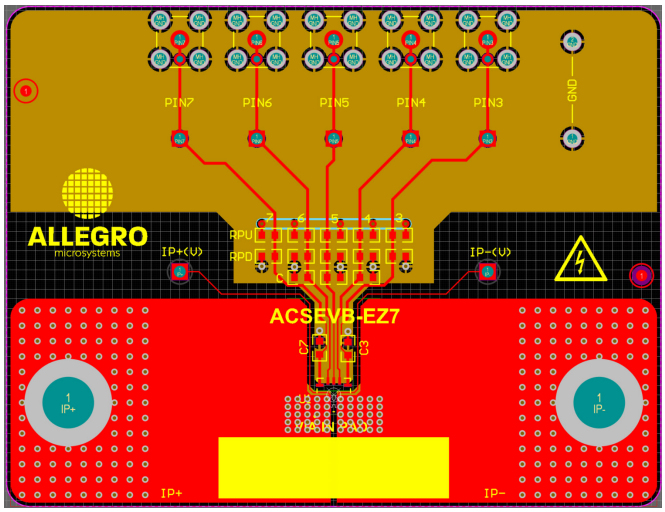


Figure 6: Top Layer of EZ Evaluation Board

Current should be distributed over all available copper layers as close to the package as possible, ideally under the package. Using vias-in-pad avoids the applied current being primarily conducted through the top layer of the PCB, which results in lower power dissipation. An 8-layer board with several layers being utilized for carrying the primary current is ideal, but a 4-layer stack-up with 2 oz copper is acceptable.

The plot in Figure 7 shows the measured rise in steady-state die temperature of the EZ package versus DC continuous current at an ambient temperature, T_A, of 25°C for two board designs: filled vias under copper pads and no vias under copper pads. This plot was generated using the evaluation board shown in Figure 6.

Note: Using in-pad vias has better thermal performance than no in-pad vias, and this is the design the EZ Current Sensor Evaluation Board uses.

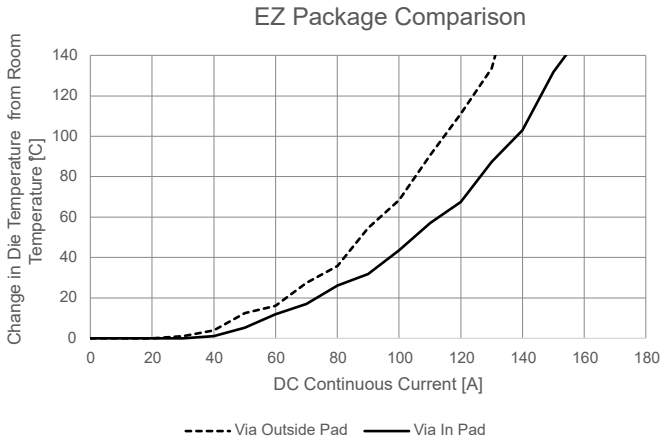


Figure 7: EZ Package Comparison with and without In-Pad Vias

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I/O leads, especially GND and VDD, should have a narrow trace of 4 milometers distance, and should not be a direct via to ground or the power plane (VDD) in order to minimize heat-sinking on that side in order to keep the die temperature uniform. This ensures heat dissipates more evenly to prevent die thermal gradient. Heat moves across the thermal gradient from a high-temperature to a low-temperature, moving from the current sensor package to other lower temperature portions of the board. When the heat generated by the component can be more efficiently dissipated through the board, this can help to prevent overheating of the die and improve the overall reliability of the board. It can also prevent minor changes in QVO or sensitivity temperature drifts due to a thermal gradient.

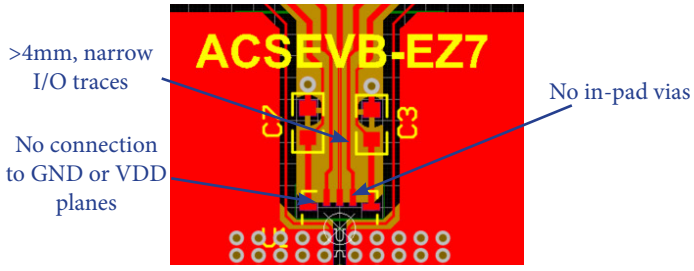


Figure 8: Top Layer of EZ Evaluation Board

Flow of Current Through the EZ Package

To achieve the datasheet specified sensitivity accuracy, the direction of the current path is through the sides of the package, from pin 1 to pin 2 (IP+ to IP-) and should follow a straight path through the IC leadframe (see Figure 9 below). The current sensor is calibrated with current flowing straight through the package. If current flows through the points labeled NC (No Connect) in a curved path around the Hall sensor elements, the sensitivity accuracy could be off by ±1% or more. The NC pins are to be soldered to the PCB to maximize the heat sinking to the PCB; current should not flow through these pins (see Figure 10 below demonstrating how the current should not flow).

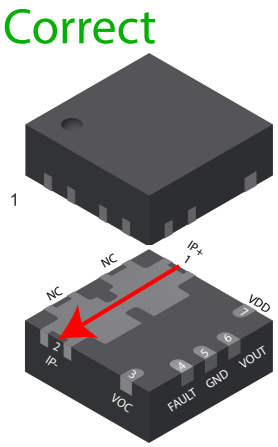


Figure 9: EZ Package Correct Flow of Current

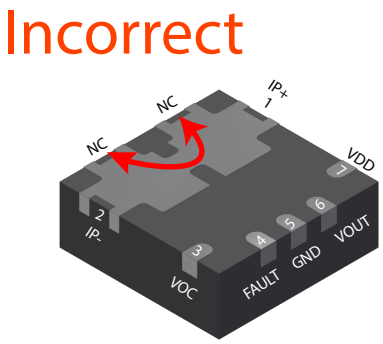


Figure 10: EZ Package Incorrect Flow of Current

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SCHEMATIC

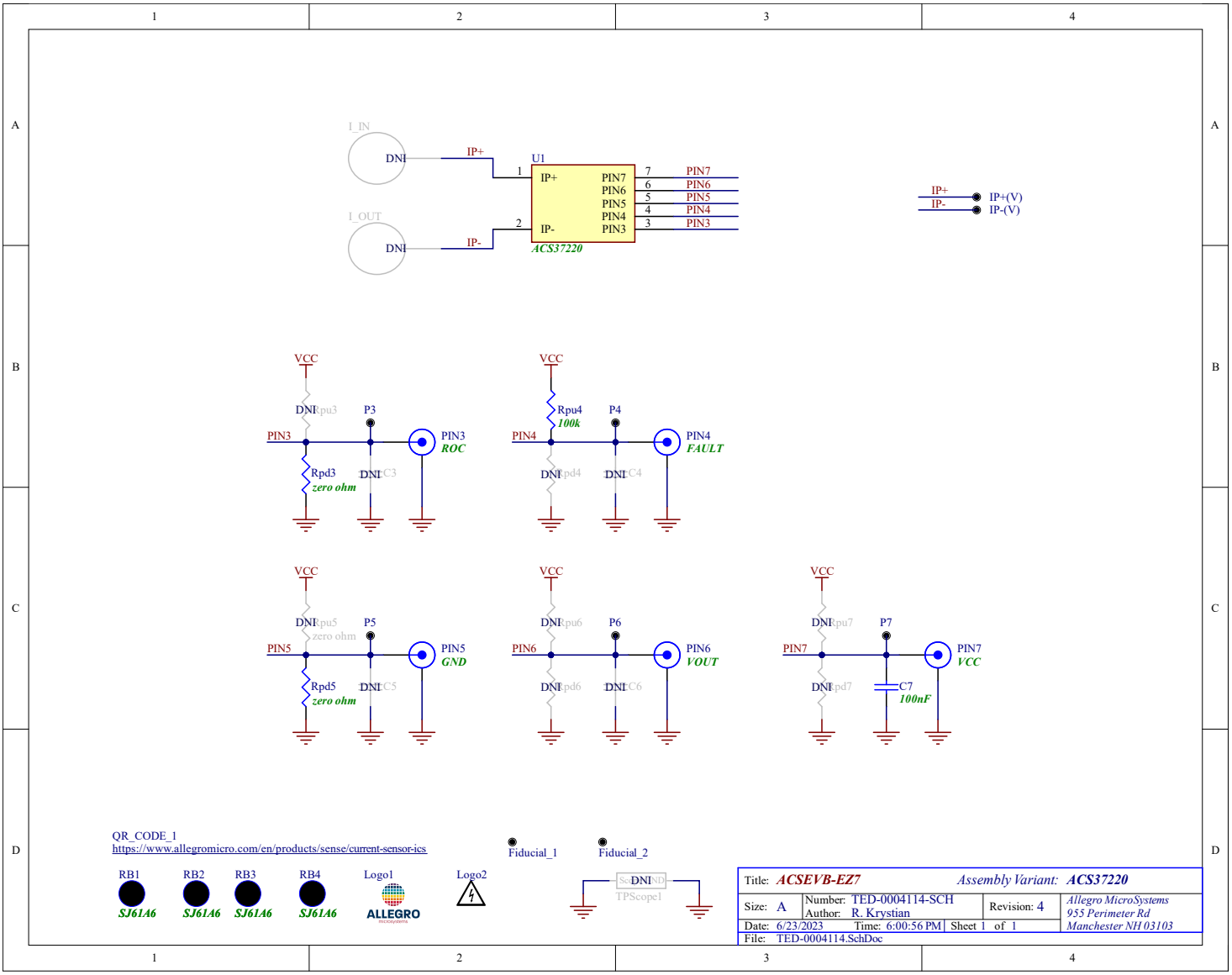


Figure 11: EZ Evaluation Board Schematic

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

LAYOUT

The EZ current sensor evaluation board has the option for a 2-pin 100 mil header connector, which allows the integrated current loop resistance to be measured directly from the evaluation board. The voltage drop sensing is routed in the first internal layer (as to not reduce isolation specification of the package). As a consequence, the voltage drop will include the parasitic resistance of the vias between the top layer and the first interior layer.

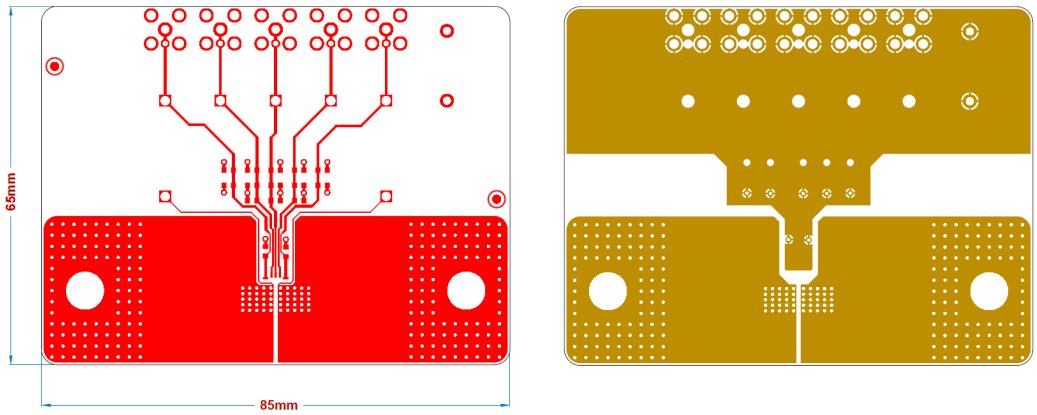


Figure 12: EZ Evaluation Board Top Layer (left) and Interior Layer 1

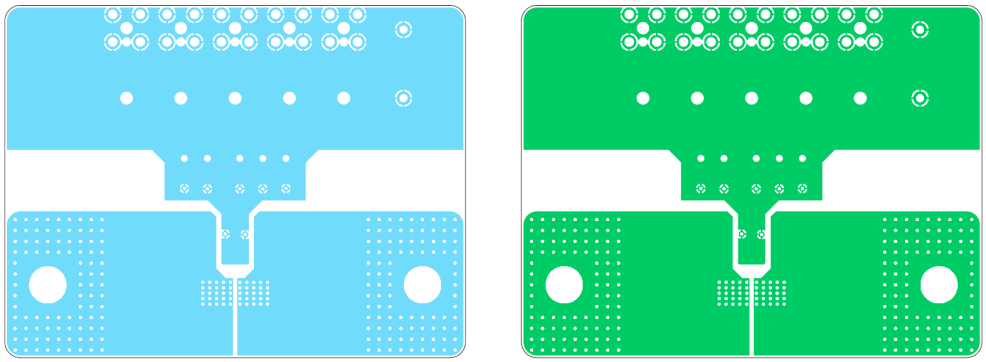


Figure 13: EZ Evaluation Board Interior Layer 2 (left) and Interior Layer 3

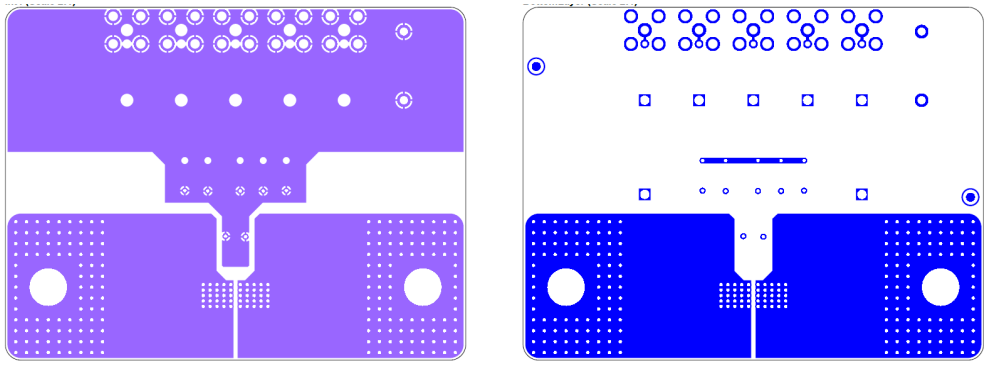


Figure 14: EZ Evaluation Board Interior Layer 4 (left) and Bottom Layer

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SUPPORTING CIRCUITRY

Components listed are based on the typical application circuit given in the respective device datasheet. In the event of a conflict between this document and the main datasheet, the datasheet takes precedence.

Table 1: Evaluation Board Bill of Materials

ACS37220 ASSEMBLY VARIANT

Pin	Terminal	Components
1	IP+	Positive and negative terminals for current being sensed
2	IP-	
3	VOC	Resistor from VOC to GND sets FAULT trip level; capacitor from VOC to GND helps with noise performance
4	FAULT	Pull-up Resistor from FAULT to VDD needed for overcurrent FAULT operation
5	GND	Connect to GND; required for implement of the current sensor
6	VOUT	Capacitor from VOUT to GND helps with noise performance and stability (not required)
7	VDD	Decoupling capacitor from VDD to GND suggested

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

RELATED LINKS AND APPLICATION SUPPORT

Table 2: Related Documentation and Application Support

Documentation	Summary	Location
Allegro Current Sensors Webpage	Product datasheet defining common electrical characteristics and performance characteristics	https://www.allegromicro.com/en/products/sense/current-sensor-ics
Allegro Current Sensor Package Documentation	Schematic files, step files, package images	https://www.allegromicro.com/en/design-support/packaging
An Effective Method for Characterizing System Bandwidth in Complex Current Sensor Applications	Application note describing methods used by Allegro to measure and quantify system bandwidth	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an-effective-method-for-characterizing-system-bandwidth-an296169
DC and Transient Current Capability/Fuse Characteristics of Surface Mount Current Sensor ICs	DC and Transient Current Capability/Fuse Characteristics of Surface Mount Current Sensor ICs	https://www.allegromicro.com/en/Insights-and-Innovations/Technical-Documents/Hall-Effect-Sensor-IC-Publications/DC-and-Transient-Current-Capability-Fuse-Characteristics.aspx
High-Current Measurement with Allegro Current Sensor IC and Ferromagnetic Core: Impact of Eddy Currents	Application note focusing on the effects of alternating current on current measurement	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an296162_a1367_current-sensor-eddy-current-core
Secrets of Measuring Currents Above 50 Amps	Application note regarding current measurement greater than 50 A	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an296141-secrets-of-measuring-currents-above-50-amps
Allegro Hall-Effect Sensor ICs	Application note describing Hall-effect principles	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/allegro-hall-effect-sensor-ics
Hall-Effect Current Sensing in Electric and Hybrid Vehicles	Application note providing a greater understanding of hybrid electric vehicles and the contribution of Hall-effect sensing technology	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/hall-effect-current-sensing-in-electric-and-hybrid-vehicles
Hall-Effect Current Sensing in Hybrid Electric Vehicle (HEV) Applications	Application note providing a greater understanding of hybrid electric vehicles and the contribution of Hall-effect sensing technology	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/hall-effect-current-sensing-in-hybrid-electric-vehicle-hev-applications
Achieving Closed-Loop Accuracy in Open-Loop Current Sensors	Application note regarding current sensor IC solutions that achieve near closed-loop accuracy using open-loop topology	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/achieving-closed-loop-accuracy-in-open-loop-current-sensors
Allegro Current Sensor ICs Can Take the Heat! Unique Packaging Options for Every Thermal Budget	Application note regarding current sensors and package selection based on thermal capabilities	https://www.allegromicro.com/-/media/files/application-notes/an296190-current-sensor-thermals.pdf
Explanation Of Error Specifications For Allegro Linear Hall-Effect-Based Current Sensor Ics And Techniques For Calculating Total System Error	Application note describing error sources and their effect on the current sensor output	https://www.allegromicro.com/-/media/files/application-notes/an296181-acs72981-error-calculation.pdf

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	August 25, 2023	Initial release
1	January 4, 2024	Corrected part numbers (page 1), minor editorial and clarification updates

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com