

APM80905 Evaluation Board User Guide

DESCRIPTION

The APM80905 Evaluation Board is designed to help system designers evaluate the operation and performance of the APM80905 synchronous buck LED driver ClearPower module. The APM80905 Evaluation Board can support various length strings of LEDs, including IR LEDs, and the output current can be configured by changing the value of a sense resistor.

FEATURES

- APM80905 Synchronous buck LED driver module.
- Test points for applying enable, PWM and analog dimming inputs.
- PWM Monitor with user-selectable TMAX and DMAX configuration for safety when powering IR LEDs.
- Active low fault flag output.
- Banana jacks for input and output power connections.

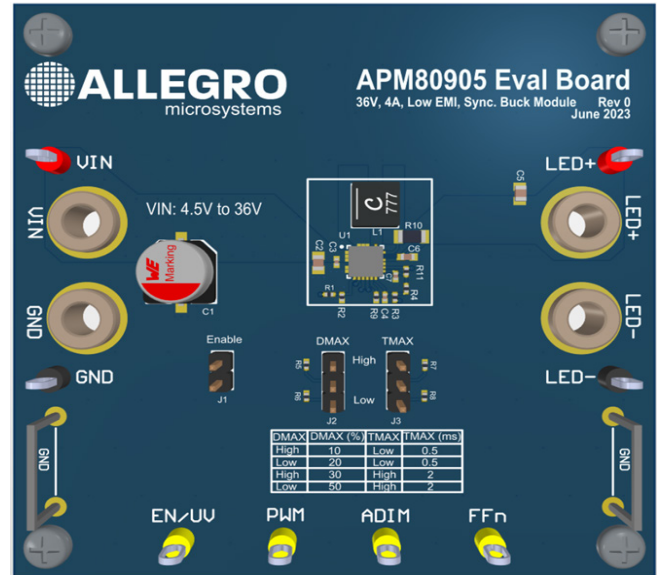


Figure 1: APM80905 Evaluation Board

Table of Contents

Description	1
Features	1
Using the Evaluation Board	2
Evaluation Board Performance Data	5
Schematic	9
Bill of Materials	10
PCB Layout	11
Related Links	12
Application Support	12
Revision History	13



Table 1: APM80905 Evaluation Board Configurations

Configuration Name	Part Number	Output Current (A)
APM80905 Evaluation Board	APEK80905KNB-01	1

Table 2: General Specifications

Specification	Min	Nom	Max	Units
Input Operating Voltage	4.5	–	36	V
Output Current [1]	–	1	–	A
Switching Frequency	–	2.1	–	MHz
PWM Input Logic High Threshold	–	–	1.2	V
PWM Input Logic LowThreshold	0.6	–	–	V
En Input Logic High	–	1.2	–	V
EN Input Logic Low	–	–	1.0	V
ADIM Input Range	0.62	–	1.75	V

[1] Output current can be adjusted to desired level up to 4 A by changing the current sense resistor R10.

USING THE EVALUATION BOARD

This section provides an overview of the connections and configuration options of the APM80905 Evaluation Board. Each group of connections highlighted in Figure 2 has a detail section below. The default jumper positions are highlighted in green. The APM80905 datasheet contains detailed information on the use and functionality of each pin. The datasheet should be consulted for more detailed information than is contained in this user guide.

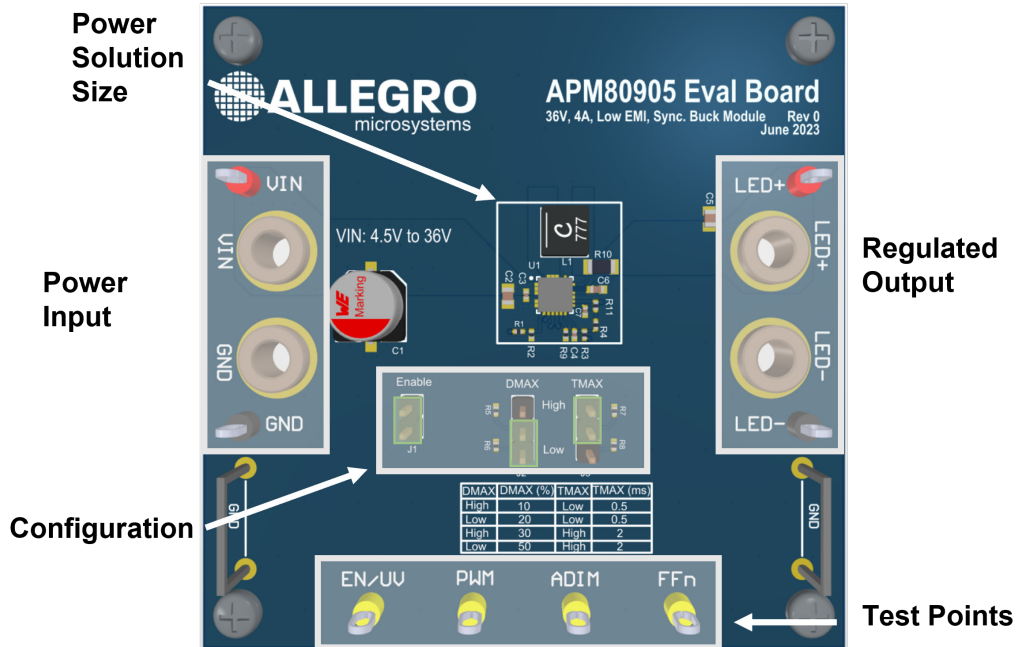


Figure 2: APM80905 Evaluation Board I/O Connections and Default Jumper Positions

Power Input

Connect a power supply using banana plugs or clip leads to the left side of the Evaluation Board using the VIN and GND connections.

Power Output

Connect one or more high power LEDs using banana plugs or clip leads to the right side of the Evaluation Board using the LED+ and LED– connections. The number of LEDs that can be powered is limited by the input voltage. The APM80905 is a buck converter, so the input voltage must exceed the output voltage for proper operation.

Output Current

The APM80905 Evaluation Board is configured for a 1 A output but can achieve up to a 4 A output current by changing the value of the sense resistor, R10. If an output current other than 1 A is desired, see the datasheet for details on selecting the appropriate sense resistor.

Accurate Enable

The APM80905 Evaluation Board is set up with a 10 kΩ resistor from Vin to the Enable pin, EN, when the Enable jumper is installed. Optionally, R2 may be installed to complete a voltage divider on the EN pin which will allow the APM80905 to start up and shut down at a set input voltage. If this behavior is desired, consult the APM80905 datasheet for more details.

Analog Dimming

Analog dimming to reduce the regulated output current level is achievable by applying a voltage between 0.62 V and 1.3 V to the ADIM test point. If analog dimming is desired, consult the APM80905 datasheet for more details on the setup and limitations of this function.

Device Configuration

The APM80905 Evaluation Board has three configuration jumpers. The DMAX and TMAX jumpers must be configured prior to power-on.

Table 3: APM80905 Jumper Descriptions

Jumper	Name	Description
J1	Enable	Install jumper to tie EN pin to VIN and enable the APM80905. Uninstall to control enable using an external signal connected at the EN/UV test point.
J2	DMAX	Install this jumper in the desired location for the maximum duty cycle limit. Install in the high position for 10% or 20% or install in the low position for 30% or 50% duty cycle. See Table 4 for more details on setting DMAX and TMAX.
J3	TMAX	Install this jumper in the desired location for maximum PWM on-time limit. Install in the high position for a 0.5 millisecond limit or install in the low position for a 2 millisecond maximum PWM on-time limit. See Table 4 for more details on setting DMAX and TMAX.

Startup Procedure

To begin using the APM80905 Evaluation Board, follow the instructions below and refer to the diagram in Figure 2 or the test point connections outlined in Table 5.

1. Ensure the two jumpers for DMAX/TMAX are in the Low/High positions respectively for initial testing.
2. Connect an LED load to the regulated output connections of the APM80905 Evaluation Board. The load should be a string of one or more LEDs capable of handling 1 A of current.
3. Ensure the Enable jumper J1 is installed or leave open and apply an external enable signal to the EN/UV test point.
4. If using ADIM, apply a DC voltage to the ADIM test point between 0.62 V and 1.3 V.
5. Apply an external PWM signal to the PWM test point. The initial settings of the PWM signal should be a pulse wave with a frequency of 400 Hz, a duty cycle of 10%, and amplitude levels of 0 V and 2.5 V.
6. Apply an input voltage across the Power Input terminals that is 3 V higher than the expected forward voltage drop of the LED string on the output. Do not exceed 36 V on the Power Input connections. To ensure desirable startup behavior the input power source should be able to supply twice the regulated output current level (1 A on the standard APM80905 Evaluation Board).

NOTE: The DMAX and TMAX jumper positions were selected for quick start up and evaluation. Once initial board operation has been achieved try different jumper configurations according to those in Table 4, combined with different PWM duty cycle limits. To obtain specific DMAX and TMAX limits, the resistor values associated with each pin can be changed. See the datasheet for detailed instructions on setting the DMAX.

Table 4: APM80905 DMAX/TMAX Settings

DMAX	DMAX (%)	TMAX	TMAX (ms)
High	10	Low	0.5
Low	20	Low	0.5
High	30	High	2.0
Low	40	High	2.0

Table 5: APM80905 Test Point Description

Test Point	Description
VIN	Positive terminal for input voltage connection or sensing.
GND	Negative terminal for input voltage connection or sensing.
LED+	Positive terminal for the output current to the LED load.
LED-	Negative terminal for the output current to the LED load.
EN/UV	Enable pin voltage input. Leave Enable Jumper, J1, open if applying an external signal on the EN/UV test point.
PWM	PWM control input. Connect an appropriate pulsed signal to this test point to switch output current on/off. Avoid violating the DMAX and TMAX limitations to prevent faults.
ADIM	Analog dimming control input. Apply an external voltage between 0.62 V and 1.3 V to achieve between 20% and 90% LED dimming. The ADIM pin is pulled high through a 100 k Ω resistor, R4, and can be left open if ADIM is not used.
FFn	The fault pin is asserted low when a fault is detected. Monitor this test point for faults.

EVALUATION BOARD PERFORMANCE DATA

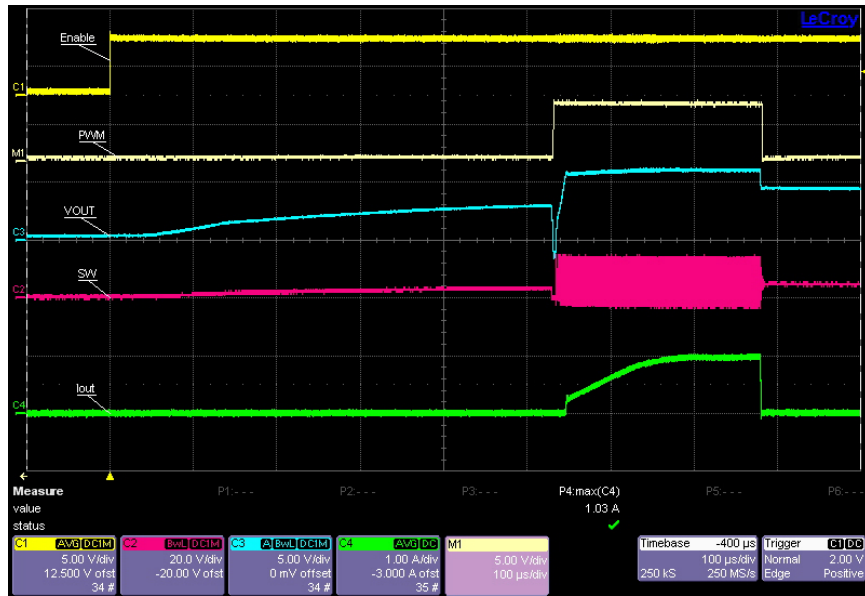


Figure 3: Startup, 2 LEDs, Externally applied Enable Pulse, VIN = 12.5 V

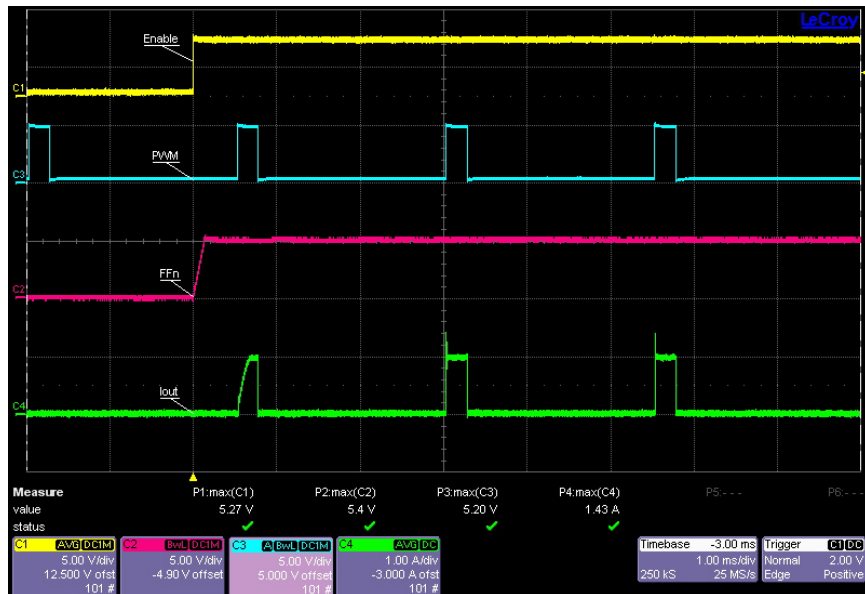


Figure 4: Normal Operation, Fault Pin Remains High

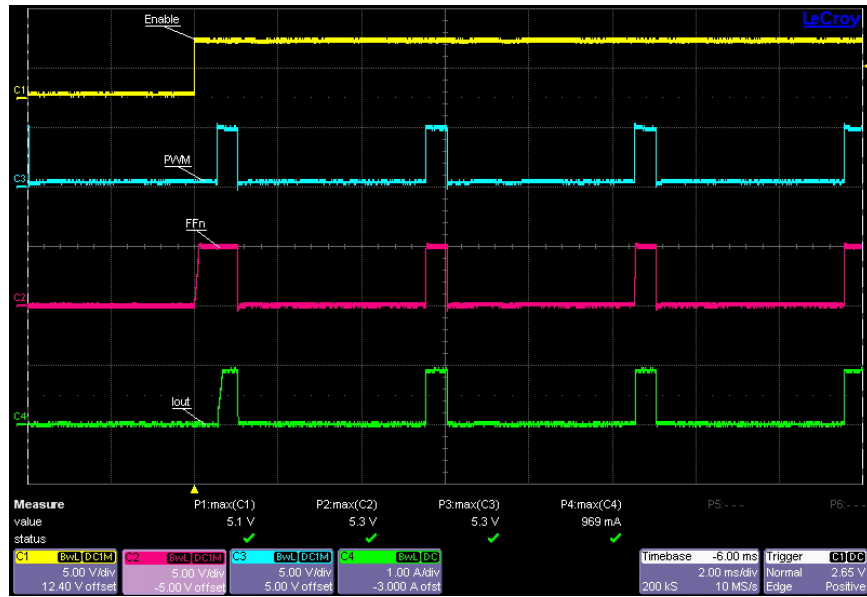


Figure 5: Repeated t_{MAX} fault, PWM pulse exceeds t_{MAX} .

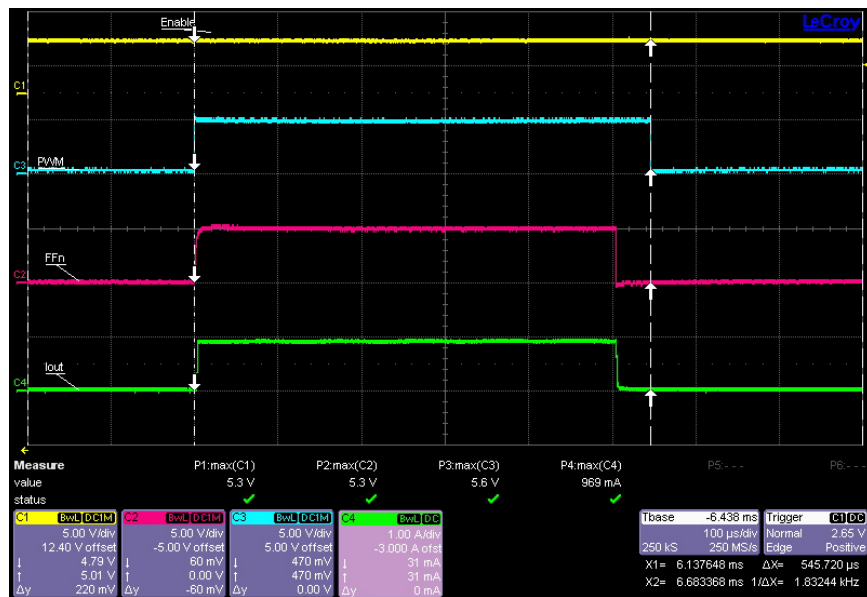


Figure 6: Single t_{MAX} fault, PWM pulse exceeds t_{MAX} .

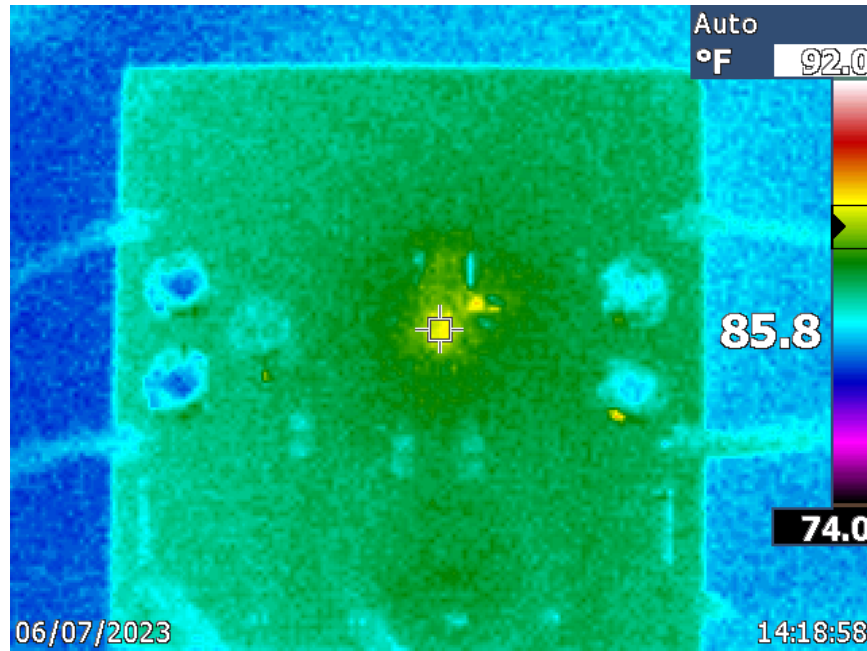


Figure 9: Thermal Performance, 2 White LEDs, $V_{in} = 12\text{ V}$, $I_{LOAD} = 1\text{ A}$, $D_{MAX} = 50\%$, $T_{MAX} = 2\text{ ms}$, $PWM = 400\text{ Hz}$, 48% duty cycle

SCHEMATIC

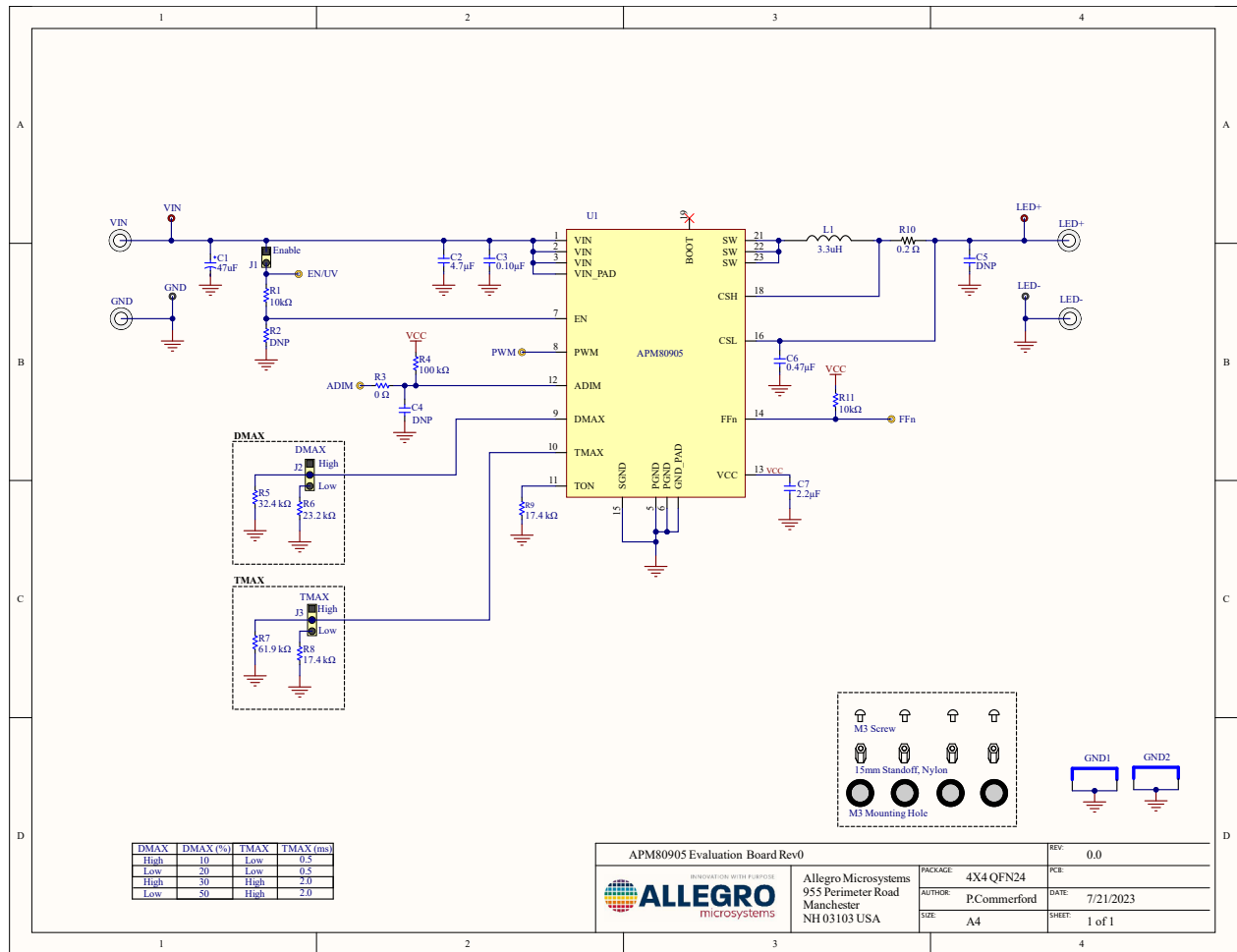


Figure 10: APM80905 Evaluation Board schematic

BILL OF MATERIALS

Table 6: APEK80905KNB-01 Version Evaluation Board Bill of Materials

ELECTRICAL COMPONENTS				
Designator	Quantity	Description	Manufacturer	Manufacturer Part Number
C1	1	Capacitor, Electrolytic, 47 uF, 50 V, 8 mm	Nichicon	UUX1H470MNL6GS
C2	1	CAP CER 4.7 µF 50 V X5R 0805	Murata	GRM21BR61H475KE51L
C3	1	CAP CER 0.1 µF 50 V X5R 0402	Murata	GRM155R61H104KE19D
C7	1	CAP CER 2.2 µF 16V X5R 0402	Murata	GRM155R61C225KE11D
C6	1	CAP CER 0.47 µF 50V X5R 0603	Murata	GRM188R61H474KA12D
L1	1	Inductor, 3.3 uH	CoilCraft	XAL5030-332ME
R1, R11	2	Resistor, 10.0 kΩ, 1/16 W, 1%, 0402	Yaego	AC0402FR-0710KL
R3	1	Resistor, 0 Ω, 1/16 W, Jumper, 0402	Yaego	RC0402FR-070RL
R4	1	Resistor, 100 kΩ, 1/16 W, 1%, 0402	Yaego	RC0402FR-13100KL
R5	1	Resistor, 32.4 kΩ, 1/16 W, 1%, 0402	Yaego	RC0402FR-0732K4L
R6	1	Resistor, 23.2 kΩ, 1/16 W, 1%, 0402	Yaego	RC0402FR-0723K2L
R7	1	Resistor, 61.9 kΩ, 1/16 W, 1%, 0402	Yaego	RC0402FR-0761K9L
R8, R9	2	Resistor, 17.4 kΩ, 1/16 W, 1%, 0402	Yaego	RC0402FR-0717K4L
R10	1	Resistor, 0.2 Ω, 1/2 W, 1%, 1206	Panasonic	ERJ-8BSFR20V
U1	1	APM80905 in MIS package	Allegro MicroSystems	APM80905KNBATR
OTHER COMPONENTS				
Designator	Quantity	Description	Manufacturer	Manufacturer Part Number
VIN	1	Banana Jack- Non-Insulated .218" Length	Keystone Electronics	575-4
LED+	1	Banana Jack- Non-Insulated .218" Length	Keystone Electronics	575-4
LED-	1	Banana Jack- Non-Insulated .218" Length	Keystone Electronics	575-4
GND	1	Banana Jack- Non-Insulated .218" Length	Keystone Electronics	575-4
GND1, GND2	2	Ground Bar, 18 AWG Bus Bar, 12 mm Body	N/A	N/A
J1	1	CONN HEADER VERT 2POS 2.54MM	Würth Electronics	61300211121
J2, J3	2	CONN HEADER VERT 3POS 2.54MM	Würth Electronics	61300311121
MH1, MH2, MH3, MH4	4	M3 sized mounting hole	N/A	N/A
MS1, MS2, MS3, MS4	4	PAN HEAD SCREW_M3 X 8MM CROSS SL	Würth Electronics	97790803111
SO1, SO2, SO3, SO4	4	Standoffs & Spacers 5.0 HEX 15.0 mm NYLON	Keystone Electronics	25512
VIN, LED+	2	Test Point, Red, Through Hole Mount, 1.6 mm	Keystone Electronics	5010
GND, LED-	2	Test Point, Black, Through Hole Mount, 1.6 mm	Keystone Electronics	5011
EN/UV, PWM, ADIM, FFn	4	Test Point, Yellow, Through Hole Mount, 1.6 mm	Keystone Electronics	5014
PCB	1	APM80905 Customer Evaluation Board	Allegro MicroSystems	
NOT FITTED				
C4	0	Optional Multi-Layer Ceramic Capacitor	Murata	GRM155R61C225KE11D
C5	0	Optional Multi-Layer Ceramic Capacitor	Murata	GCM21BR71H474KA55L
R2	0	Optional Resistor, 0402	Yaego	AC0402FR-0710KL

PCB LAYOUT

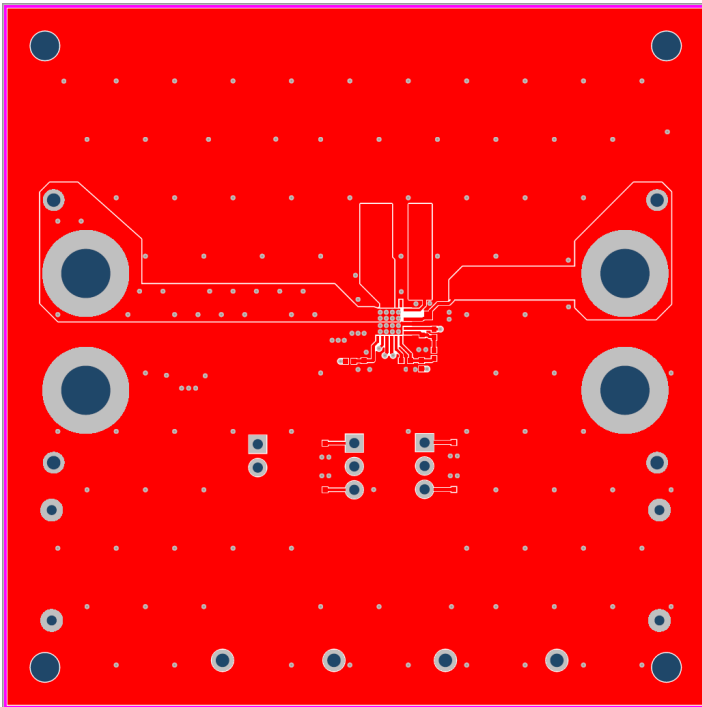


Figure 11: Top Layer

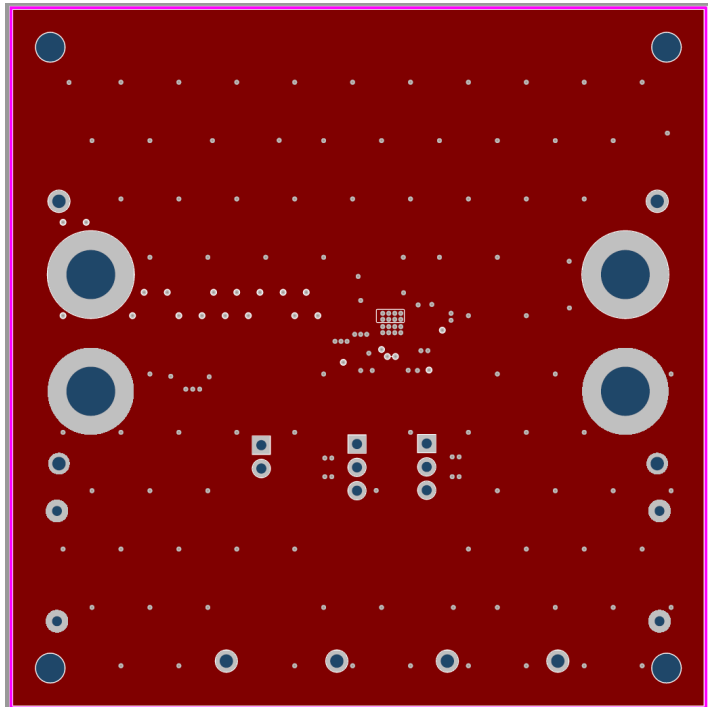


Figure 12: Inner Layer 2 (PGND Plane)

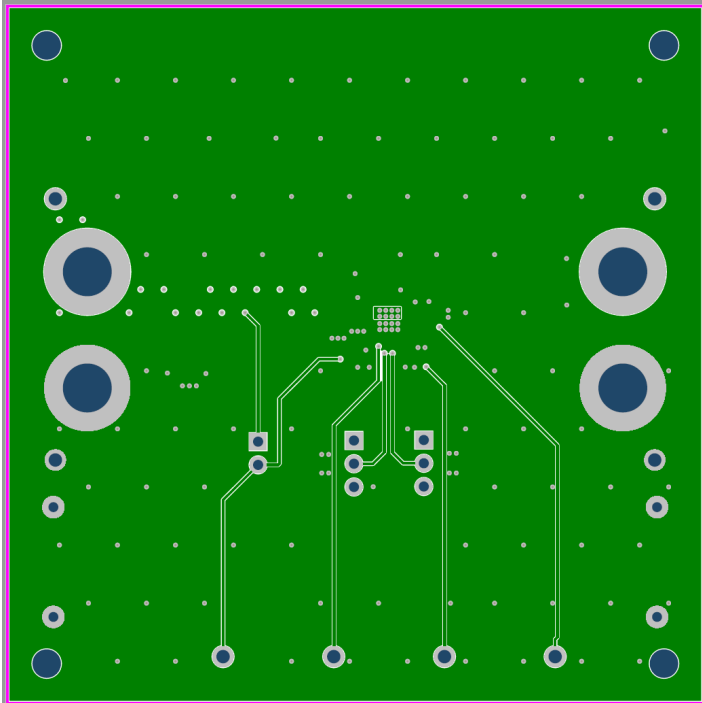


Figure 13: Inner Layer 3 (PGND Plane)

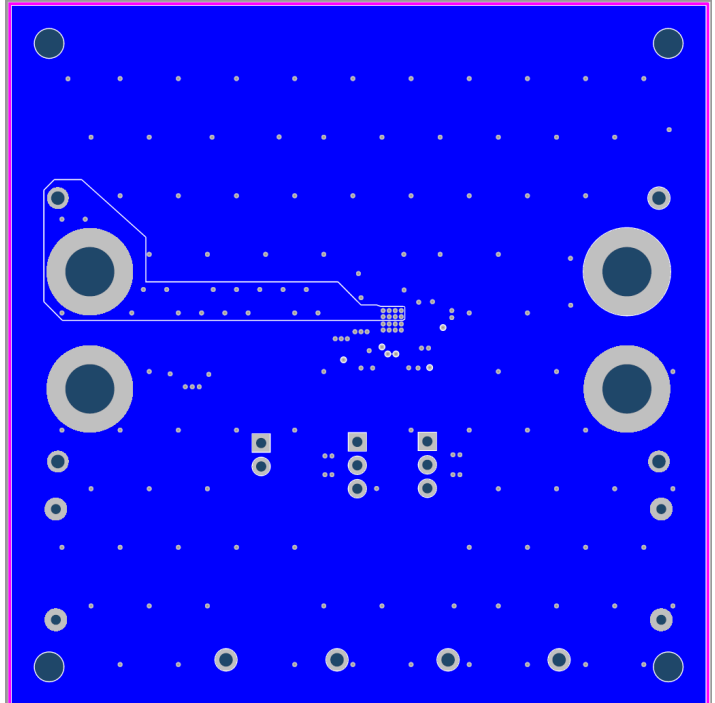


Figure 14: Bottom Layer 4

RELATED LINKS

<https://www.allegromicro.com>

APPLICATION SUPPORT

<https://www.allegromicro.com>

Revision History

Number	Date	Description
-	July 26, 2023	Initial release

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