ACSEVB-MA16-LA16

MA/LA/SW Package Bare Evaluation Board User Guide

DESCRIPTION

Bare evaluation boards offer a method for evaluating Allegro current sensors in a lab environment. This document describes the use of the MA/LA/SW current sensor evaluation board.This evaluation board (ACSEVB-MA16-LA16, TED-0004111) is intended for use with any MA, LA or SW package (16-pin SOIC-W) Allegro Hall-based or TMR-based current sensors.

FEATURES OF THE BARE BOARD

- Enhanced thermal performance:
  - □ 6-layer PCB with 2 oz copper weight on all layers
  - □ Nonconductive filled Via-In-Pad used
  - □ High performance FR4 material with 180°C glass transition temperature
- Flexible layout for user installed connection points
  - □ Standard Keystone test points
  - □ SMA/SMB connector
  - □ 2-pin headers
- Integrated current loop resistance can be measured directly on the evaluation board after test point installation; voltage drop can be measured for approximating power loss in the package.

EVALUATION BOARD CONTENTS

- **NOTE:** It is up to the user to assemble the board with the desired current sensor and supporting circuitry. This board does not come populated with an Allegro current sensor or other components.
- Recommended supporting circuitry for all compatible current sensor are listed in the Supporting Circuitry section below.

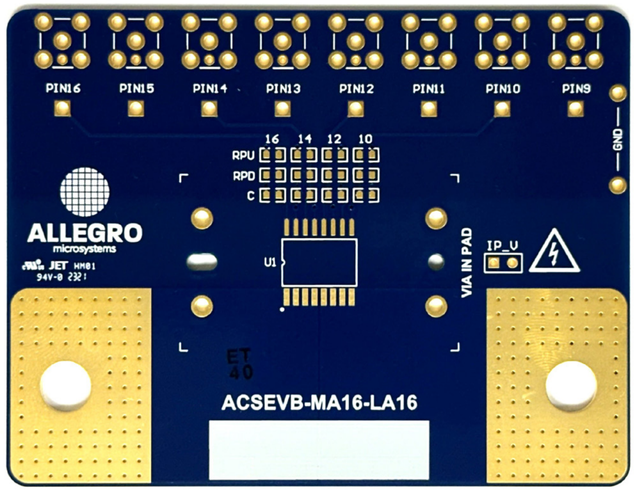
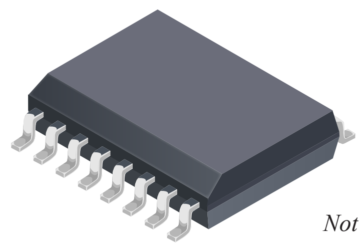


Figure 1: MA/LA/SW Bare Evaluation Board



Not to scale

Figure 2: SOIC-W Package (MA/LA/SW Package)

Table of Contents

USING THE EVALUATION BOARD

Evaluation Board Components

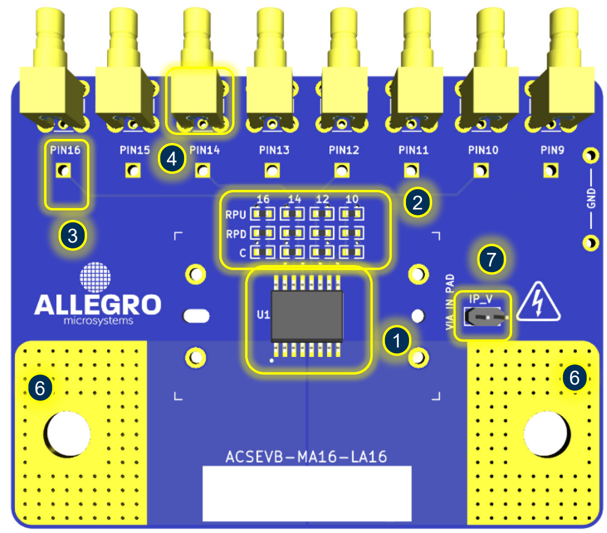
1. U1 is an MA/LA/SW package footprint (Pin 1 is on bottom left side, see the small white dot)
2. U1 pins allow the option to connect:
   - □ RPU: Pull-up resistor to VCC
   - □ RPD: Pull-down resistor to GND
   - □ C: decoupling or load capacitor to GND
   - □ All passive components are 0603 package size
3. Keystone 5005 test points (e.g., Digikey #36-5005-ND)
4. Standard SMB/SMA connector (e.g., Digikey #1868-1429-ND)
5. 2-pin 100 mil header connector option (note: either SMB or header can be assembled)
6. Primary current cables mounting positions (positive current flow direction is left to right)
7. 2-pin 100 mil header connector for voltage drop measurement across the integrated current loop of the current sensor
8. RB1, RB2, RB3, and RB4: rubber bumper mounting positions (e.g., Digikey #SJ61A6-ND)

Evaluation Board Procedure

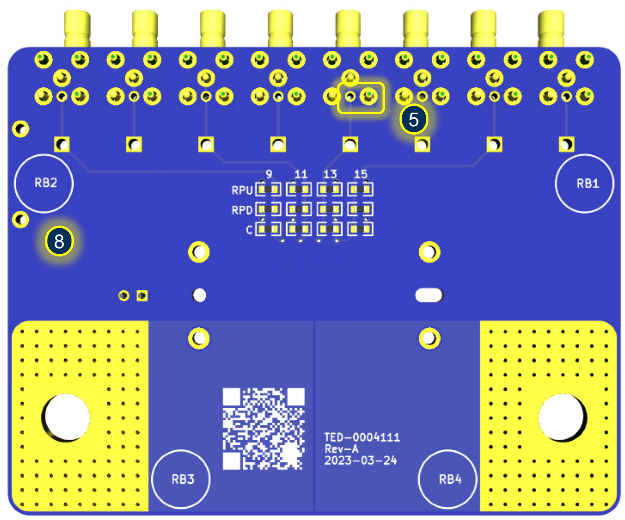
CONNECTING TO THE EVALUATION BOARD

The best way to connect measurement instruments to the evaluation board is to use SMB/SMA or 2-pin headers connectors along with coaxial cables. This configuration will be most resilient to external coupling, and it is preferred way for measurement, e.g., high speed dI/dt transients.

Keystone test point are a convenient way to connect any instrument, but is it recommended for DC setups only.



Top view



Bottom view

Figure 3: MA/LA/SW Current Sensor Evaluation Board Reference Image

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EVALUATION BOARD PERFORMANCE DATA

Thermal Rise vs. Primary Current

Self-heating due to the flow of current in the package IP conductor should be considered during the design of any current sensing system. The sensor, printed circuit board (PCB), and contacts to the PCB will generate heat and act as a heat sink as current moves through the system.

The thermal response is highly dependent on PCB layout, copper thickness, cooling techniques, and the profile of the injected current. The current profile includes peak current value, current on-time, and duty cycle.

Placing vias under the copper pads of the Allegro current sensor evaluation board minimize the current path resistance and improves heatsinking to the PCB, while vias outside of the pads limit the current path to the top of the PCB trace and have worse heatsinking under the part (see Figure 4 and Figure 5 below). The ACSEVB-MA16-LA16 does include vias in pad and is recommended to improve thermal performance.

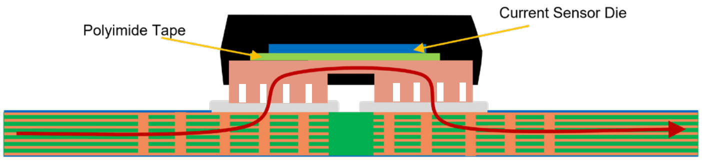

Figure 4: Vias Under Copper Pads (not to scale)

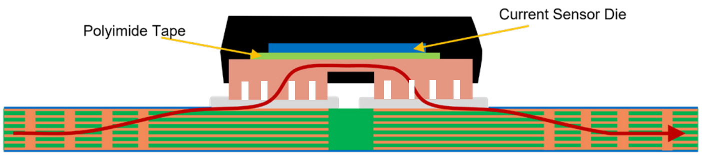

Figure 5: No Vias Under Copper Pads (not to scale)

The plot in Figure 6 shows the measured rise in steady-state die temperature of the MA package versus DC continuous current at an ambient temperature, T_A, of 25 °C for two board designs: filled vias under copper pads and no vias under copper pads.

The plot in Figure 7 shows the measured rise in steady-state die temperature of the LA package versus DC continuous current at an ambient temperature, T_A, of 25 °C for two board designs: filled vias under copper pads and no vias under copper pads.

Note: Using in-pad vias has better thermal performance that no in-pad vias, and this is the design the ACSEVB-MA16-LA16 uses.

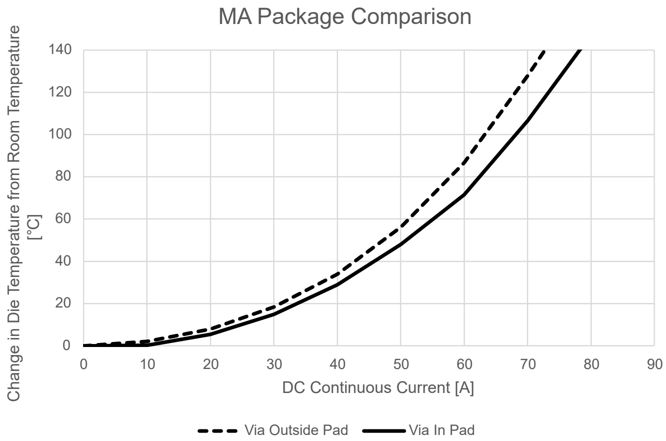

Figure 6: MA Package Comparison with and without In-Pad Vias

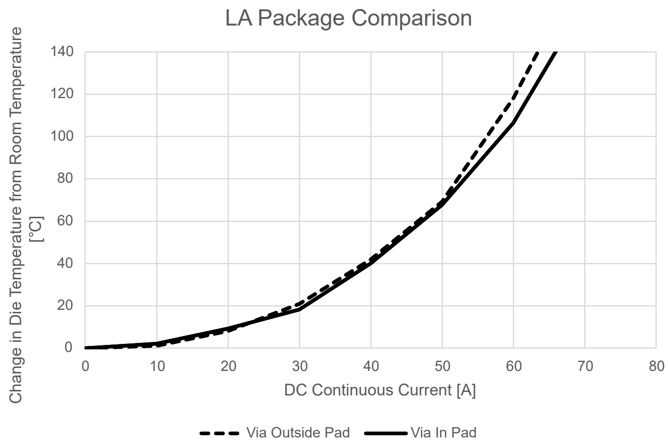

Figure 7: LA Package Comparison with and without In-Pad Vias

The thermal capacity of the MA and LA package should be verified by the end user in the application's specific conditions. The maximum junction temperature, $T_{J(max)}$ (165°C), should not be exceeded. Measuring the temperature of the top of the package is a close approximation of the die temperature.

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SCHEMATIC

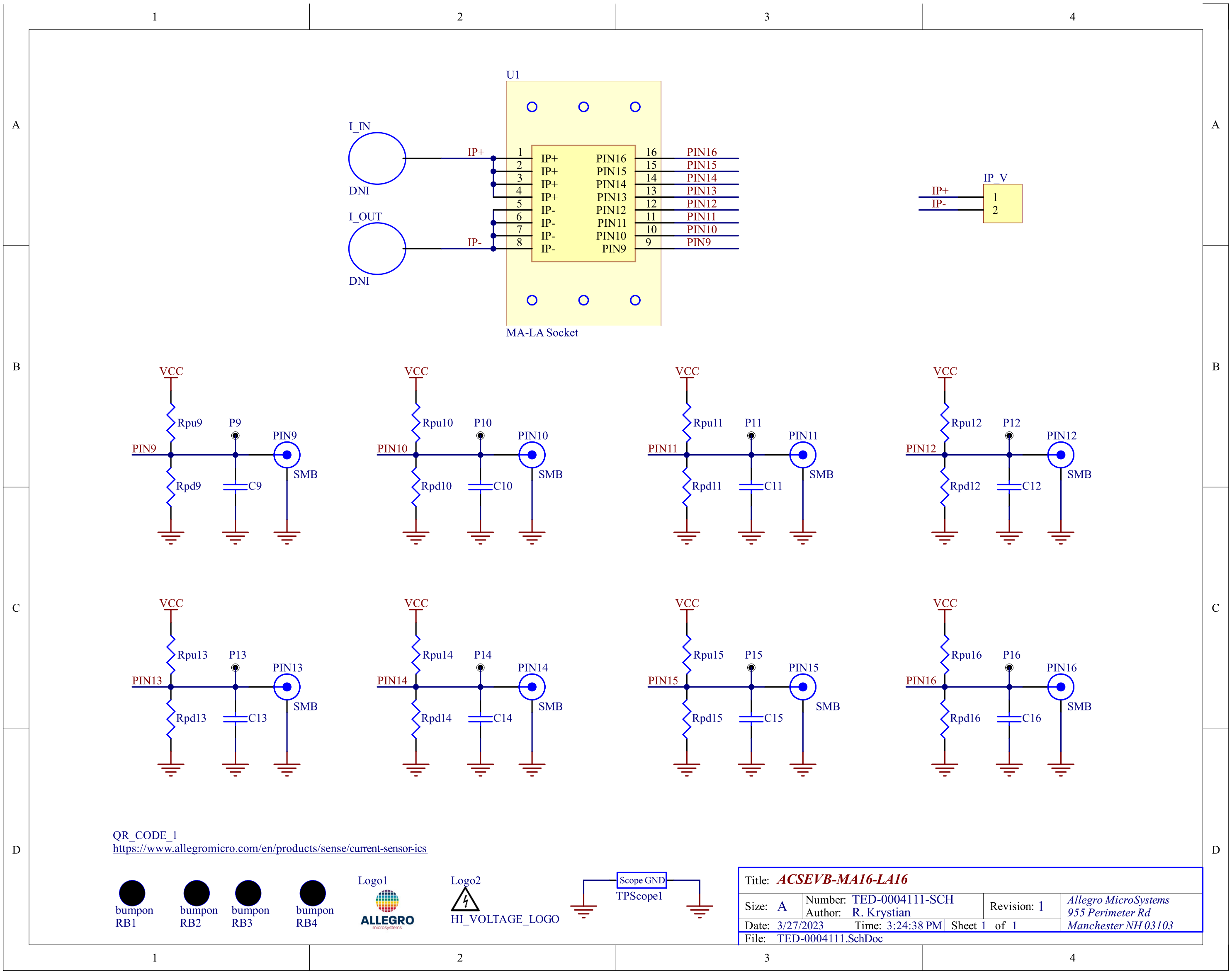

Figure 8: MA/LA/SW Generic Evaluation Board Schematic

LAYOUT

The MA/LA Current Sensor Evaluation board has the option for a 2-pin 100 mil header connector, which allows the integrated current loop resistance to be measured directly from the evaluation board. The voltage drop sensing is routed in the first internal layer (as to not reduce isolation spec of the package). As a consequence, the voltage drop will include the parasitic resistance of the vias between the top layer and the first interior layer.

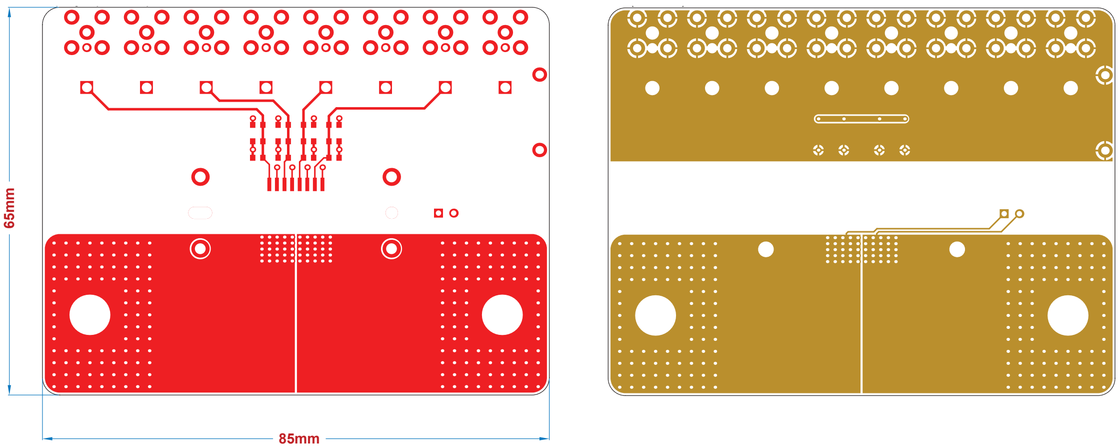

Figure 9: MA/LA/SW Bare Evaluation Board Top Layer (left) and Interior Layer 1

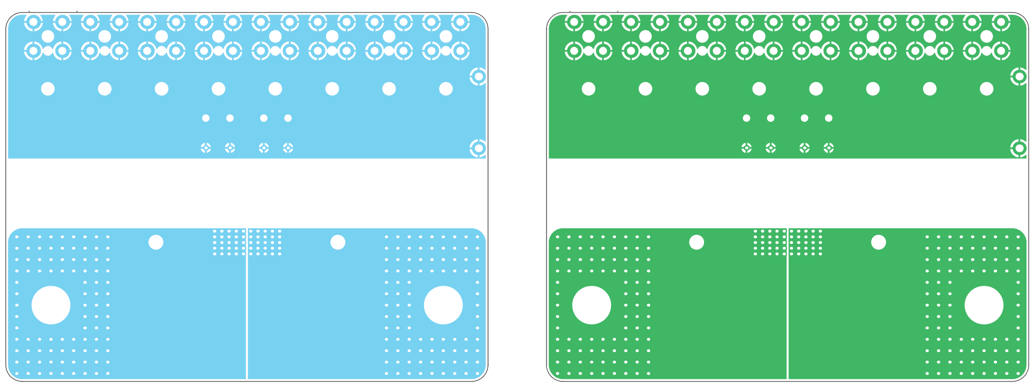

Figure 10: MA/LA/SW Bare Evaluation Board Interior Layer 2 (left) and Interior Layer 3

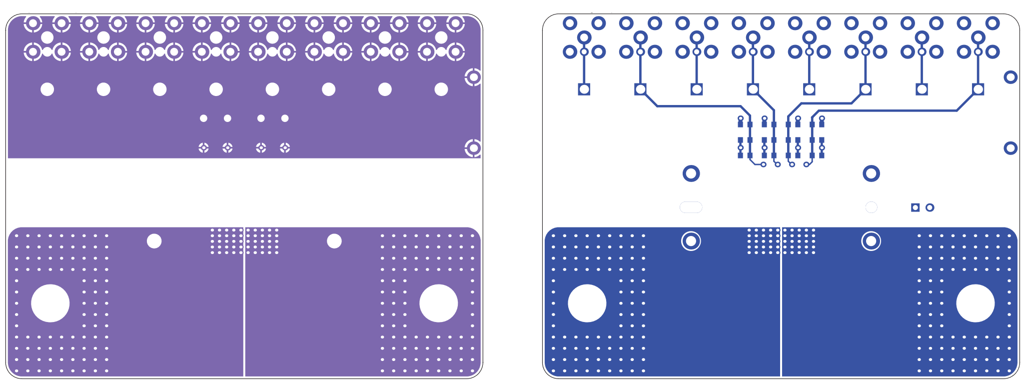

Figure 11: MA/LA/SW Bare Evaluation Board Interior Layer 4 (left) and Bottom Layer

SUPPORTING CIRCUITRY

Components listed are based on the typical application circuit given in the respective device datasheet. In the event of a conflict between this document and the main datasheet, the datasheet takes precedence.

Table 1: Evaluation Board Circuitry

ACS37002 ASSEMBLY VARIANT (MA AND LA)

Pin	Terminal	Components
1, 2, 3, 4	IP+	Terminals for current being sensed; fused internally
5, 6, 7, 8	IP-	
9	OCF	Overcurrent fault, open-drain, requires pull-up resistor
10	VCC	Device power supply terminal, connected to supply voltage
11	VOC	Overcurrent fault operation point input, connected to resistor divider or external power source
12	VOUT	Analog output representing the current flowing through IP, optional load capacitance or load resistance
13	VREF	Zero current voltage reference
14	GAIN_SEL_1	Gain selection bit 1, connected to high or GND
15	GND	Device ground terminal, connected to GND
16	GAIN_SEL_0	Gain selection bit 0, connected to high or GND

ACS724/25 ASSEMBLY VARIANT (MA)

Pin	Terminal	Components
1, 2, 3, 4	IP+	Terminals for current being sensed; fused internally
5, 6, 7, 8	IP-	
9, 11, 14, 16	NC	No internal connection; recommended to be left unconnected in order to maintain high creepage
10	VCC	Device power supply terminal, connected to supply voltage
12	VOUT	Analog output representing the current flowing through IP, optional load capacitance or load resistance
13	FILTER	Terminal for external capacitor that sets bandwidth
14	GAIN_SEL_1	Gain selection bit 1, connected to high or GND
15	GND	Device ground terminal, connected to GND

ACS732/733 ASSEMBLY VARIANT (MA AND LA)

Pin	Terminal	Components
1, 2, 3, 4	IP+	Terminals for current being sensed; fused internally
5, 6, 7, 8	IP-	
9, 10	GND	Device ground terminal, connected to GND
11	PROGRAM	Programming input pin for factory calibration. Connect to GND for best ESD performance
12	VOUT	Analog output representing the current flowing through IP, optional load capacitance or load resistance
13	FAULT	Overcurrent fault, open-drain, requires pull-up resistor
14	VOC	Overcurrent fault operation point input, connected to resistor divider or external power source
15, 16	VCC	Device power supply terminal, connected to supply voltage

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RELATED LINKS AND APPLICATION SUPPORT

Table 2: Related Documentation and Application Support

Documentation	Summary	Location
Allegro Current Sensors Webpage	Product datasheet defining common electrical characteristics and performance characteristics	https://www.allegromicro.com/en/products/sense/current-sensor-ics
Allegro Current Sensor Package Documentation	Schematic files,step files, package images	https://www.allegromicro.com/en/design-support/packaging
An Effective Method for Characterizing System Bandwidth in Complex Current Sensor Applications	Application note describing methods used by Allegro to measure and quantify system bandwidth	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an-effective-method-for-characterizing-system-bandwidth-an296169
DC and Transient Current Capability/Fuse Characteristics of Surface Mount Current Sensor ICs	DC and Transient Current Capability/Fuse Characteristics of Surface Mount Current Sensor ICs	https://www.allegromicro.com/en/Insights-and-Innovations/Technical-Documents/Hall-Effect-Sensor-IC-Publications/DC-and-Transient-Current-Capability-Fuse-Characteristics.aspx
High-Current Measurement with Allegro Current Sensor IC and Ferromagnetic Core: Impact of Eddy Currents	Application note focusing on the effects of alternating current on current measurement	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an296162_a1367_current-sensor-eddy-current-core
Secrets of Measuring Currents Above 50 Amps	Application note regarding current measurement greater than 50 A	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an296141-secrets-of-measuring-currents-above-50-amps
Allegro Hall-Effect Sensor ICs	Application note describing Hall-effect principles	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/allegro-hall-effect-sensor-ics
Hall-Effect Current Sensing in Electric and Hybrid Vehicles	Application note providing a greater understanding of hybrid electric vehicles and the contribution of Hall-effect sensing technology	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/hall-effect-current-sensing-in-electric-and-hybrid-vehicles
Hall-Effect Current Sensing in Hybrid Electric Vehicle (HEV) Applications	Application note providing a greater understanding of hybrid electric vehicles and the contribution of Hall-effect sensing technology	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/hall-effect-current-sensing-in-hybrid-electric-vehicle-hev-applications
Achieving Closed-Loop Accuracy in Open-Loop Current Sensors	Application note regarding current sensor IC solutions that achieve near closed-loop accuracy using open-loop topology	https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/achieving-closed-loop-accuracy-in-open-loop-current-sensors
Allegro Current Sensor ICs Can Take the Heat! Unique Packaging Options for Every Thermal Budget	Application note regarding current sensors and package selection based on thermal capabilities	https://www.allegromicro.com/-/media/files/application-notes/an296190-current-sensor-thermals.pdf
Explanation Of Error Specifications For Allegro Linear Hall-Effect-Based Current Sensor Ics And Techniques For Calculating Total System Error	Application note describing error sources and their effect on the current sensor output	https://www.allegromicro.com/-/media/files/application-notes/an296181-acs72981-error-calculation.pdf

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Revision History

Number	Date	Description
–	August 17, 2023	Initial release
1	August 28, 2024	Editorial updates throughout; updated title, figure 1 caption, and description (page 1)