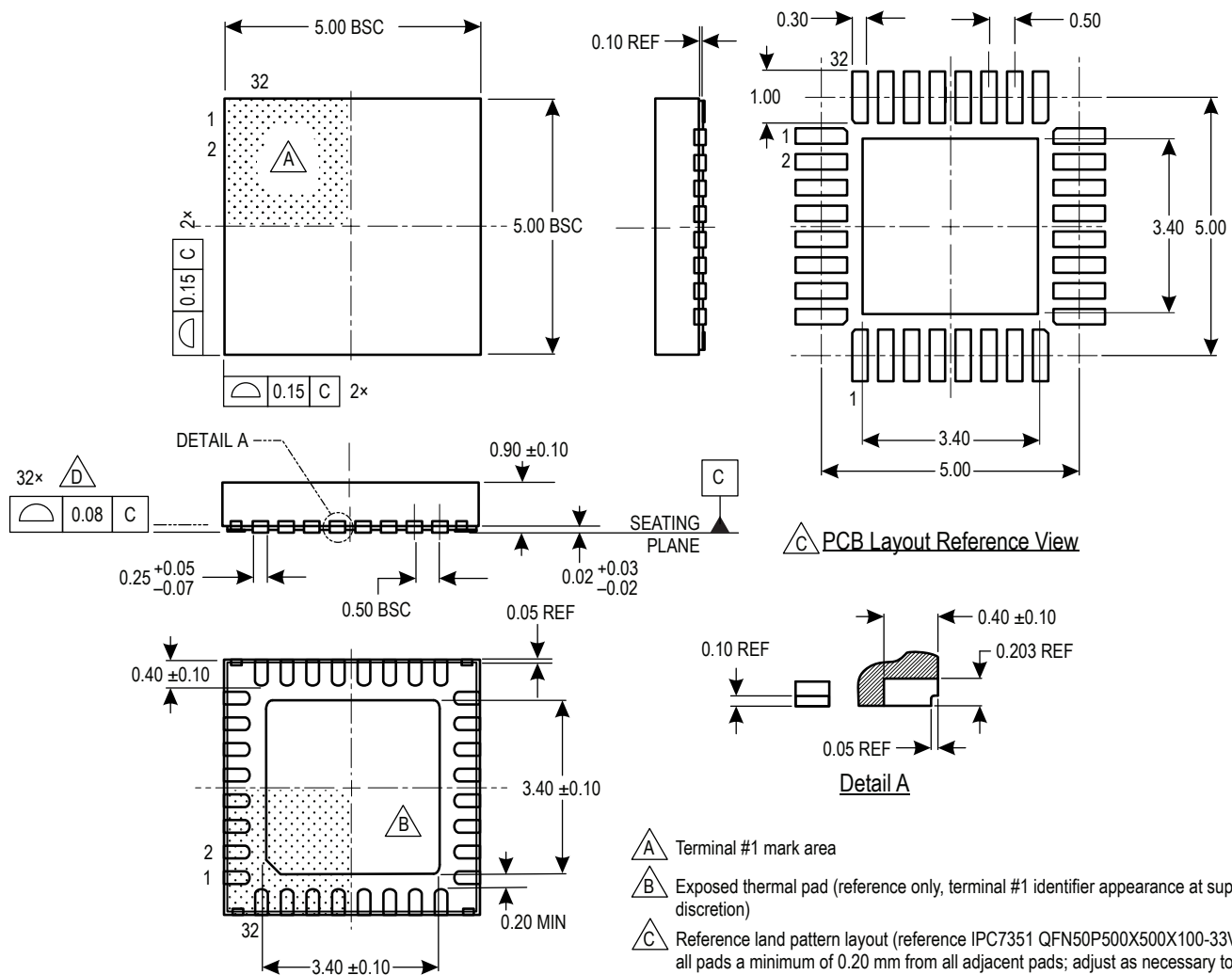


For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000378, Rev. 3 and JEDEC MO-220VHHD-5)

Dimensions in millimeters – NOT TO SCALE

Exact case and lead configuration at supplier discretion within limits shown



- A** Terminal #1 mark area
- B** Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)
- C** Reference land pattern layout (reference IPC7351 QFN50P500X500X100-33V6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)
- D** Coplanarity includes exposed thermal pad and terminals