Three-Phase Motor Controller IC Drives External FETs for PWM Current Control, Synchronous Rectification, and 100% Duty-Cycle Capability

By Peter Morris
Allegro MicroSystems, LLC

ABSTRACT

The increasing use of high-current brushless dc (BLDC) three-phase motors puts stringent requirements on the drive electronics for function and safety. A new three-phase motor controller has integrated all the circuitry to control the six power NMOS FETs for fractional horse-power motors up to 50 V. The basic techniques of fixed off-time PWM current control and bootstrapped high-side gate drives are enhanced by adding synchronous rectification control, cross-conduction protection and on-chip charge pumps to allow 100% PWM duty cycles. Safety features and diagnostic output prevent inappropriate switching of the power FETs and allow programmable motor spin-down on power loss.

This paper presents the system concepts and describes the circuit implementation of several key features.

FUNCTIONAL DESCRIPTION

Architecture overview

The block diagram of the A3932 chip (figure 1) shows all the main functions. Being a three-phase driver, there are three half-bridge drive circuits (one only shown in the diagram). Each phase has a high and low side drive circuit providing the push-pull control to charge and discharge the external FET gates. The low side gate driver simply runs off the regulated voltage VREG (13 V with respect to ground), while the high side driver circuit supply is bootstrapped up above the motor supply Vbb (Cx is about 12 V with respect to the Sx terminal, see below).

It is common practice to add resistors in series with the gates when driving high current FETs in motor drive circuits, to reduce slew rates and hence noise, coupling and emission problems. Since this technique increases turn-on and off times there is a danger that both FETs in a phase could be partially on at the same time during state changes. To prevent the resulting high shoot-through currents the design provides a turn-on delay circuit, which stops either driver turning on until the other has been turned off for a fixed time (the deadtime), set by an external resistor on the DEAD terminal. It is up to the user to ensure that this time is sufficient. Directly sensing the gate voltages would allow an automatic cross-over protection scheme to be implemented, but this would add 6 terminals to the chip. It is also not generally preferred by designers, the deadtime scheme giving more flexibility for system design.

PWM current control is achieved by chopping the high-side FET (which also guarantees frequent refresh of the bootstrap capacitor during normal operation). A fixed off-time control scheme is implemented – the user setting the scale (external sense resistor in the bridge's ground return) and the timing (parallel resistor/capacitor on the RC terminal). This fixed off-time function can be used as the main current-control loop or as an upper current limit with the PWM terminal duty cycle providing the main control. To prevent false tripping by reverse recovery spikes, user adjustable leading edge blanking is integral with this scheme.

Correct commutation of the three half-bridges requires accurate rotor position information. A standard way of doing this is via three hall-effect sensors placed at 120 electrical degree intervals, their logic outputs being fed to the Hx inputs. Any scheme that provides a clear logic-level signal (such as angular position sensors or back-emf (bemf) detection) can also be used.

The control logic block takes the commutation information and the fixed off-time signal, together with other user controlled input (PWM, DIR, MODE, SR, BRAKE & RESET), so as to provide the appropriate logic states to all six outputs – as shown in the state tables in figure 2.

Standard control functions of direction (DIR), pulse-width-modulation of the active high-side driver (PWM), RESET and BRAKE, are complemented by more advanced features – MODE and SR.

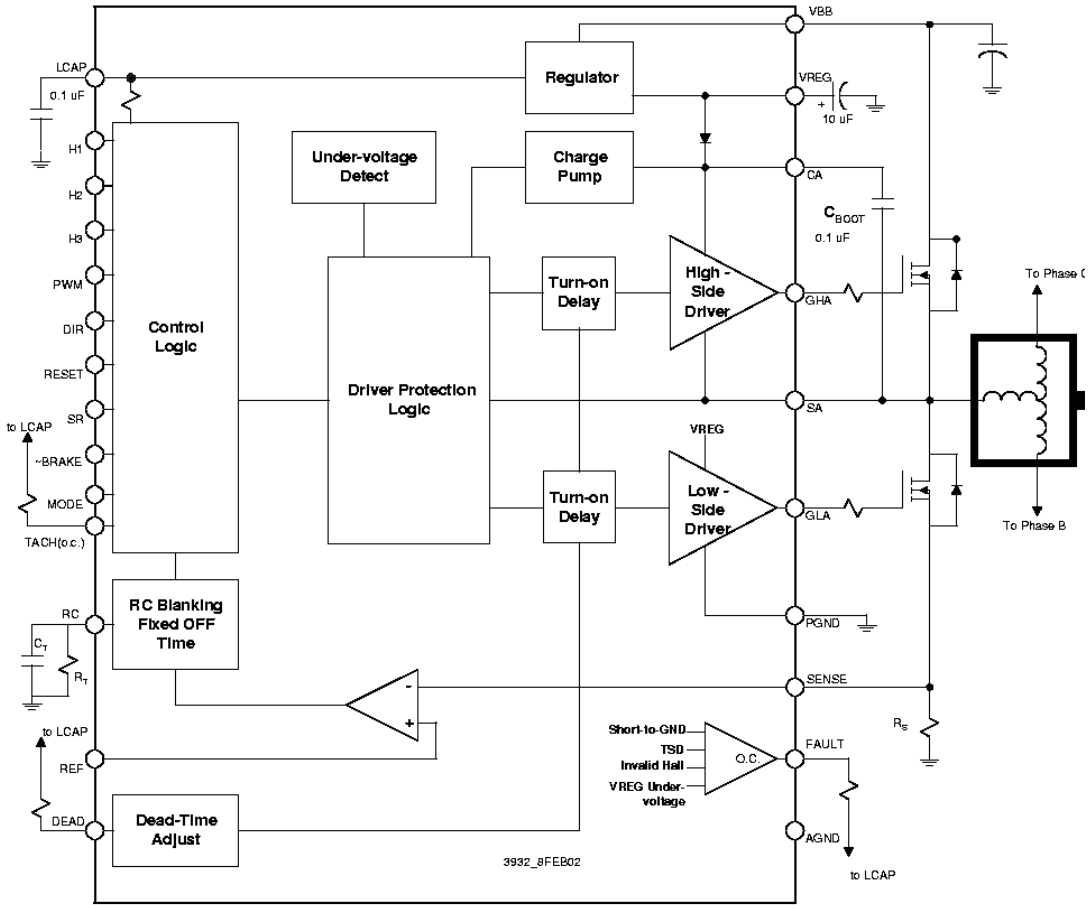


Figure 1 – A3932 block diagram (only one phase of three shown)

Figure 2a – Commutation truth table

H1	H2	H3	DIR	GLA	GLB	GLC	GHA	GHB	GHC	SA	SB	SC
1	0	1	1	0	0	1	1	0	0	HI	Z	LO
1	0	0	1	0	0	1	0	1	0	Z	HI	LO
1	1	0	1	1	0	0	0	1	0	LO	HI	Z
0	1	0	1	1	0	0	0	0	1	LO	Z	HI
0	1	1	1	0	1	0	0	0	1	Z	LO	HI
0	0	1	1	0	1	0	1	0	0	HI	LO	Z
1	0	1	0	1	0	0	0	0	1	LO	Z	HI
1	0	0	0	0	1	0	0	0	1	Z	LO	HI
1	1	0	0	0	1	0	1	0	0	HI	LO	Z
0	1	0	0	0	0	1	1	0	0	HI	Z	LO
0	1	1	0	0	0	1	0	1	0	Z	HI	LO
0	0	1	0	1	0	0	0	1	0	LO	HI	Z

Figure 2b – Current control state logic

BRAKE	MODE	PWM	SR	RESET	Quadrant	Mode of operation
0	0	0	0	0	Fast decay	PWM chop – current decay, all drivers OFF
0	0	1	0	0	Fast decay	Peak current limit, selected drivers ON
0	1	0	0	0	Slow decay	PWM chop – current decay, selected low-side drivers ON
0	1	1	0	0	Slow decay	Peak current limit, selected drivers ON
0	0	0	1	0	Fast decay	PWM chop – current decay with opposite drivers ON
0	0	1	1	0	Fast decay	Peak current limit, selected drivers ON
0	1	0	1	0	Slow decay	PWM chop – current decay with both low-side drivers ON
0	1	1	1	0	Slow decay	Peak current limit, selected drivers ON
X	X	X	X	1	N/A	All gate outputs to 0 V – clear fault logic
1	X	X	X	0	N/A	Brake – all low-side drivers ON, all high-side drivers OFF

The MODE terminal allows the selection of slow or fast decay modes, which defines the load current recirculation path during the off-time (see figure 3) allowing the user flexibility to profile the load current waveform. During slow decay the high-side driver only is turned off and the current recirculates through the same phase's low side. During fast decay the same thing happens but in addition the low-side driver is turned off so the current also recirculates through it's partner high-side FET.

The SR input allows selection of synchronous rectification, which turns on the appropriate low- or high-side driver during recirculation shorting out the reversed body diode and hence reducing dissipation in the power FETs. The body diodes will still be conducting for the duration of the deadtime.

It is crucial for these types of high-current applications to have protection circuits to prevent inappropriate FET drive signals, as well as general circuit protection. These are covered in a later section.

The process chosen for this device is Allegro™ ABCD3 process (Allegro, Bipolar, CMOS, DMOS, 3rd generation). Merging analogue bipolar/CMOS, low-voltage CMOS logic and power DMOS transistors, ABCD3 features 65 V vertical power DMOS as well as 12, 35, and 65 V lateral DMOS transistors. In addition, it provides several features that allow an efficient die size to be achieved for this design, such as the twin buried layers (see next section). One complication is that the maximum on-chip gate-source voltage is restricted to 10 V, so the design of several circuit blocks requires care to ensure no gates are overstressed – ABCD3 again helps, as there are suitable Zener-diode structures available for gate clamping.

The device is assembled into a standard low-cost 32-lead PLCC package.

Gate drivers

The requirements of the gate drive circuitry (especially the high-side driver) are very demanding:

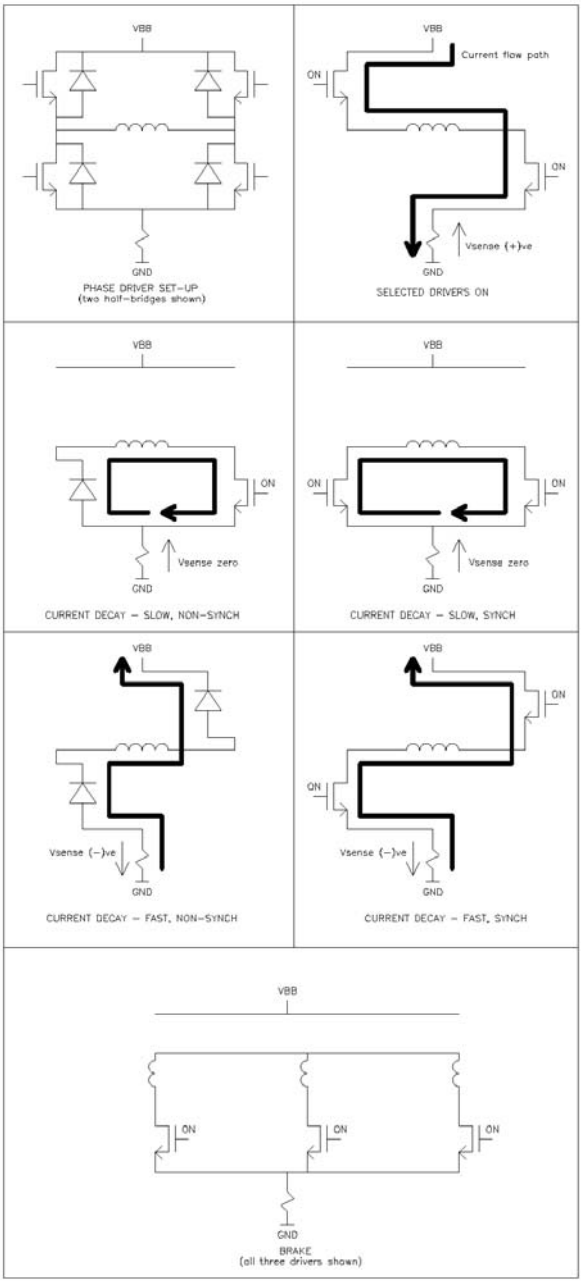
- Provide an absolute minimum gate drive of 10 V – for efficient power FET selection.
- Minimal static current consumption from the bootstrapped supply – this governs the size of the top-up charge pump (see next section).
- Operate from a 50 V motor supply (VBB), which means up to 65 V maximum on the bootstrapped supply nodes.
- Keep propagation delays low – target 100-200 ns
- Capable of driving 100 nC and higher FET gate charge.

Of course all of these requirements plus the other necessary circuit functions, must be integrated for as low a cost as possible – hence silicon area is at a premium.

The circuit technique for the high-side driver circuit is shown simplified in figure 4. The bootstrapped supply Vcs is created by Cboot being charged from the 13 V Vreg supply through diode d1 while the low-side power FET is on. Normally, during PWM operation (synchronous rectification ON and in slow decay mode) Cboot will charge up to:

$$Vcs = Vreg - Vfwd(d1) + Vds(low\text{-}side)$$

Vds should be low, to keep power FET losses to a minimum. Operating with synchronous rectification OFF will change the Vds term to the drain-bulk diode forward drop, while changing the mode to fast decay will add in Vsense (voltage drop across the sense resistor) – figure 3 may help to explain this. Care should also be taken in the board layout to ensure that the SENSE node (sources of the low-side driver) does not show excessive negative transients due to stray inductance, as this could potentially lead to Vcs getting too high. As will become apparent, the



design approach adopted does allow for correct and safe operation even with several volts negative on this node.

The above explanation applies once the phase drive has settled into PWM cycling – initial turn on of a particular phase's high-side may see Cboot charged to a lower level, due to the current being in the opposite direction in the low-side driver :

$$Vcs = Vreg - Vfwd(d1) - Vds - Vsense$$

As this will only occur for one or two cycles the slight loss of efficient drive is negligible. It is also likely that Cboot still retains its charge level from the previous phase activation.

The gate of the external high-side FET is push-pull driven through terminal GH by transistors m1 and m2, which are sized for adequate drive levels (rdson of 14 Ω for the pmos and 4 Ω for the nmos). To turn the high-side power FET on, m2 is driven on by current sink Ih2 fed through cascode transistor m7. Similarly, the high-side power FET is turned off by current sink Il2 fed through cascode m9, mirrored and fed into m1 gate, turning it on. As m1 and m2 are high gm devices and we must keep parasitic charge depletion of Cboot to a minimum, m1 and m2 must be prevented from being on at the same time during transitions. To do this, the extra current sinks Ih1 and Il2 are switched in. For example, to turn on the high side (m2 on), Ih1 starts to discharge m1's gate, but until this falls to a Vt m3 and m4 remain on holding off the gate of m2 – once m3 turns off, m4 turns off and m2 can start to turn on, driven by Ih2. Similarly for turn-off, m5 prevents Il2 from turning on m1 until m2 has virtually gone off. Ih1 and Il2 could have been derived from mirrors up at the bootstrap supply, but this would have added some extra consumption from Vcp and would have slowed down the transition time as the turn-off signal would have taken longer to propagate to the output.

This technique was chosen over the pulsed high-side latch method (ref 2) for two reasons:

- To ensure a steady-state drive in case of noise transients that might cause loss of correct state.
- Maximum Vgs limitation makes gate clamping mandatory, so some current limiting (and hence current consumption) is required – leading naturally to a current-driven approach.

To keep current consumption from the bootstrapped supply to a minimum when the high-side driver is on, the current sinks are pulsed at 0.5 mA for 1 µs to allow

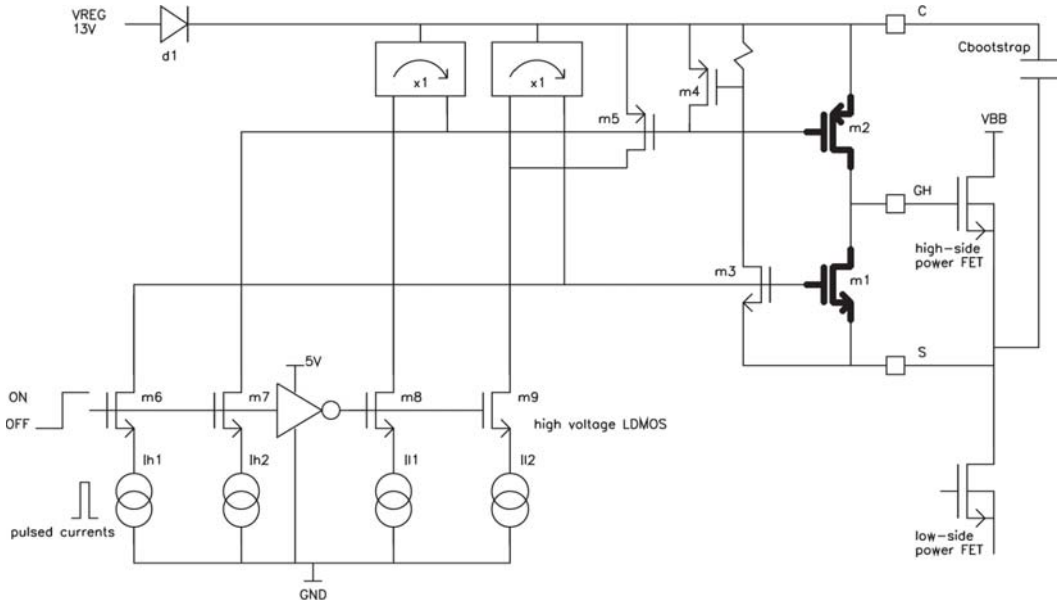


Figure 4 – High-side gate driver circuit

sufficient time for all nodes to settle before falling back to a 2 µA retention level. This gives a total static current consumption of about 10 µA from the Cboot. The actual pulse time is made proportional to the user selected dead time, so can vary from around 0.3 to 4 µs – this provides slightly better matched drive duration.

The last, but by no means trivial, advantage of the bootstrap technique is in silicon area. Because most of the circuitry is 'floating' across Vcs (<15 V) and the ABCD3 process has an n- and p-type buried layer, low-voltage devices and layout can be used within an isolated epitaxial island that is tied to the C node – the spacings of the outer edge of the island must be high voltage, but this is only the periphery, so wastes little silicon area – figure 5 shows a simplified cross-section. The current sources and switching circuits are all ground referenced low voltage also – only the four cascode devices need to be 65 V lateral dmos devices and as they are low current, signal devices can be kept to minimum size. This gives a tremendous area advantage over non-bootstrapped techniques – i.e., those that create one fixed supply above Vbb, whether by charge pump or boost converter.

Top-up charge pump

Under certain circumstances the chip is required to maintain one phase state and keep the high-side drive on for long periods of time (100% duty cycle). Maintaining gate drive to the high-side FET is critical for these conditions. As there are no recharge cycles for the boot capacitor, the charge decay (and hence loss of gate drive) must be prevented in some way. The high-side gate-drive circuitry does require a small current draw from the boot-capacitor, but even if this was not the case there would be no way to guarantee that leakage on the Cx node (chip, board, and capacitor) would not eventually create inadequate gate drive. Thus some type of auxiliary top-up circuitry is required.

Previous techniques (ref 1) have used a high-side gate monitor circuit to force a boot-capacitor recharge cycle (i.e., turn the high-side FET off and the low-side FET on until the boot-capacitor is recharged) whenever the gate voltage falls below a threshold. This system works well, but the intermittent loss of gate drive (effectively going into a brake mode) is undesirable in some applications.

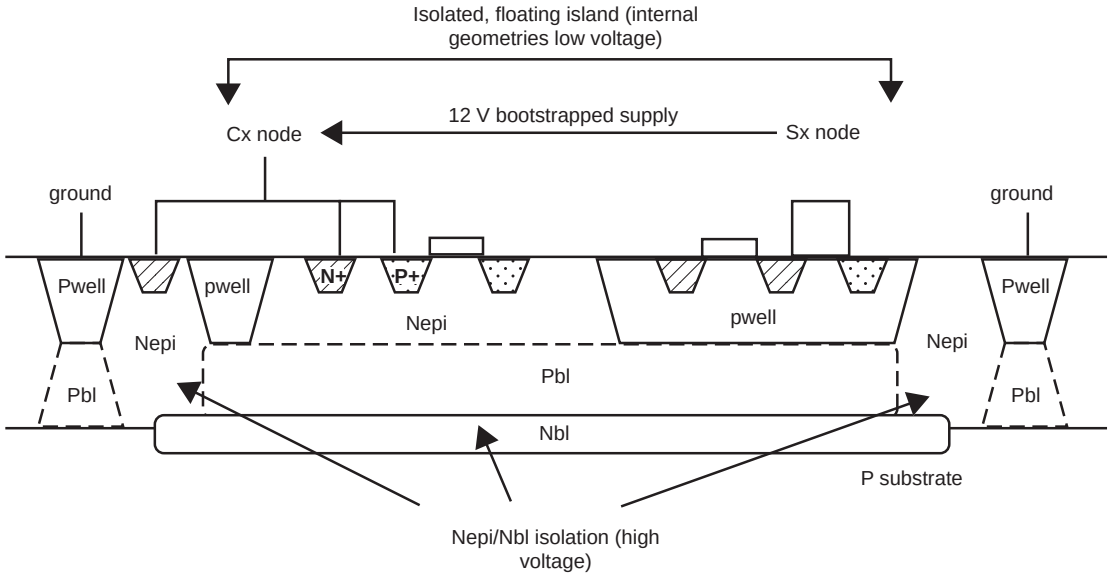


Figure 5 – High-side drive circuitry, isolated island structure

The method chosen for this chip is an internal low-current top-up charge pump that is active when the high-side FET is turned on (figure 6). In clock cycle Cb the pump capacitor C1 is charged to –12 V with respect to Vbb, set by the switched current sink I1 into R2 and clamped by Q1. In clock cycle C switches S1 and S2 are opened and S3 closed – this pulls the bottom end of the capacitor to Vbb, reverse biases D1 and forward biases D2 passing charge to GH through M2. Regulating in the charge cycle has the advantage of avoiding having to sense the voltage on the charge pump output (which can be as high as 62 V nominal) and level shift a control signal back down; while pumping relative to Vbb avoids large and variable voltage swings on m1's drain and hence loss of charge due to parasitic capacitances on this node.

The presence of M2, 3, 4, and DZ1 is to allow the output to go below ground – as happens during output flyback. Due to the high-voltage operation of the charge pump, the pump diode D2 has a parasitic diode to substrate on its cathode, so this node cannot be allowed to go below ground. Once the output and D2 cathode have dropped below Vbb, then M2 is switched off as its Vgs is negative. DZ1 clamps D2's cathode two diodes below Vdd and also prevents negative transients to M2's gate. M3 and M4 ensure that during a normal pumping cycle there is no appreciable current leakage through DZ1 to Vbb – would not turn on until Vz + 2Vthp (app. 12.5 V).

The charge-pump circuit is driven by a 1.8 MHz on-chip clock.

Protection

A feature of this chip design is to implement a fairly rigorous set of protection features to ensure that under virtually any circumstance the FET drivers can be protected from fault conditions, poor set-up (e.g., deadtime too short) and situations that might limit the gate drive in some way, leading to excessive system power dissipation. Outputs are disabled in the event of:

- VREGuvlo (undervoltage lockout) – if the 13 V regulated output falls below 9.1 V.
- Invalid Hall state – only six of the possible eight Hall states are valid positions – all 0s or all 1s are faults.

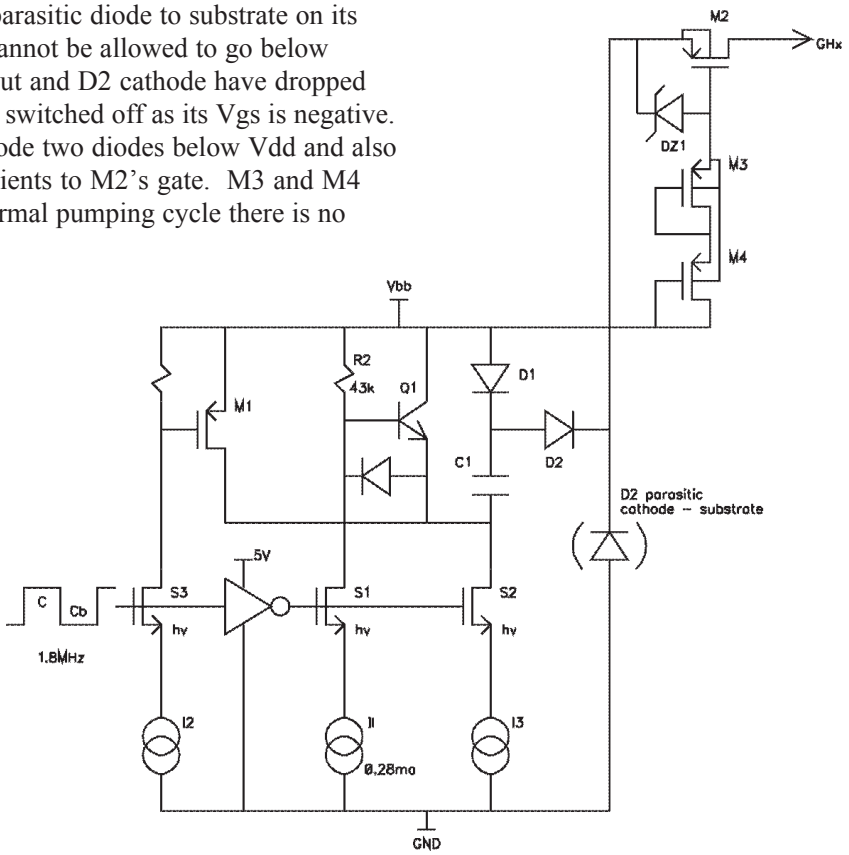


Figure 6 – Top-up charge pump

- Die temperature > 165°C – outputs disabled until die temperature cools 15°C then re-enable.
- A 'short-to-ground' on any phase node – detected if the S node does not get within 2 V of Vbb when the high-side driver is turned on. This comparator is disabled until the high-side driver goes into its low current drive state, to prevent false tripping as the drive settles. This fault is cleared at each phase commutation to allow limited operation even with one phase dead – however, if the fault causes the motor to stop before a commutation change then a system reset will be required to clear the fault.
- Note that 'short to supply' faults are effectively dealt with by the main current-control loop.
- Inadequate charging of Cboot – see below.

Ensuring that the bootstrap procedure is carried out correctly is one of the trickier protection features implemented. Monitoring the voltage across Cboot during charging and during use might be seen as ideal (ref 1), however a circuit implementation compatible with all the other operating requirements is non-trivial – especially the very low current consumption required while the high side is on. So a three-way approach was adopted:

i. During Cboot charging the charge current is monitored – as the bootstrap charge path is about 9 Ω, Cboot is not considered to be charged until this current has dropped to around 9 mA. This means it will be guaranteed to be charged to about 100 mV from the maximum.

ii. The bottom end of Cboot (i.e., the S node) is monitored to ensure it is less than 1 V from ground.

iii. Time-out – if conditions i and ii above are not met within 60 µs then there must be a fault preventing Cboot from charging, so to prevent excessive power dissipation and/or VREG failure, the Cboot charging path is disconnected. Reset or commutation is required to clear this.

The combination of the above conditions (plus the VREGuvlo) ensures that the high side is only turned on if Cboot is fully charged – if not the phase is disabled and made safe. The only lack of direct protection in this scheme is the lack of monitor of the high-side gate drive voltage – however, this is covered indirectly by the 'short-to-ground' detector. If the FET starts to lose gate drive its Vds will increase and be detected by the high-side 'short-to-ground' monitor (in this case maybe it should have been called a 'not-shorted-to-Vbb' monitor!).

Of course it would be easy to dream up fault scenarios that would damage any IC, but the target with this design was to cover the likely faults that could occur in real applications. For example, there are no direct current limits on the gate-driver outputs (GLx and GHx), but in a real application these nodes would have some series gate resistance and would not go 'off-board', so a direct short is unlikely. In the event of a power FET becoming damaged and causing a gate short then one of the other protection functions may well come into play. In addition there are other more standard protection features not mentioned so far – such as current limits on both VREG and the 5 V logic output LCAP.

Power loss brake/coast

There are two versions of this chip – so far the above descriptions have been applicable to both, but the A3938 version has an extra function added to allow controlled motor operation during a power-loss event. In some motor applications (such as reel to reel tape drives) it is important to control the operation of the motor as power is being removed. For example, in a tape drive application one reel should brake and the other coast, to ensure the tape does not run off the reel or snap.

The default system operation during power loss (detected by the VREGuvlo) is to coast the motor – i.e., turn off all drivers. The alternative is dynamic braking where all three phase windings are 'shorted' (to ground in this case) by turning on all three low-side drivers. The extra circuit block provides a means to remember the required power-down state and drive the low-side power FETs appropriately, even when the Vbb and VREG supplies have disappeared.

Figure 7 shows the concept. A user-selected capacitor on BRKCAP is charged through an internal diode D1 to VREG during normal operation. The required power-down state is applied to the BRKSEL terminal – this can be dynamically changed during normal operation but the state is latched on the VREGuvlo falling edge (i.e., on power loss being detected). Output from this block is inhibited during normal operation by the same signal.

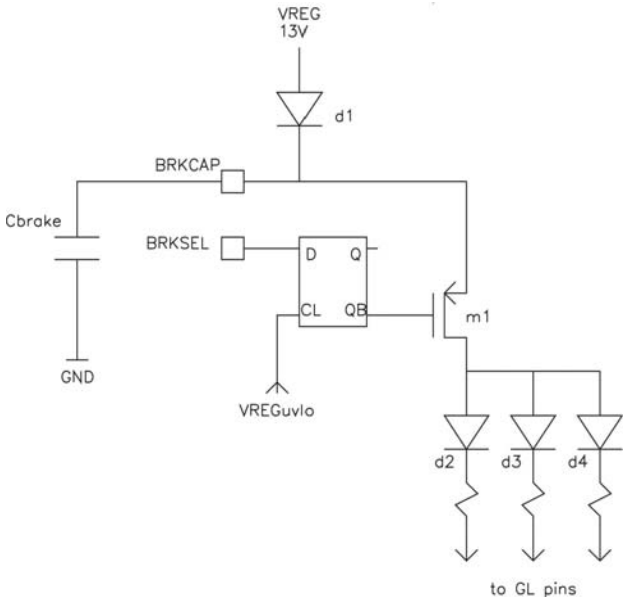


Figure 7 – Power-loss brake

Once power is lost, the falling VREG voltage will reverse bias the diode leaving the BRKCAP capacitor to provide power. If a brake mode was selected (BRKSEL = 1) then the D flip-flop clocks a 1 to its output, turning on Q1 and driving directly the three GLx to turn on the external FETs. D2-4 are required to block interactions between outputs in normal operation. Also, each output-stage driver circuit has a blocking diode added to its pmos pull-up drive, to prevent the parasitic drain-bulk diode from forward biasing and shunting the brake drive current into the VREG capacitor and VBB. Once the gates have been charged up there will be effectively zero output current, so the only current discharging the BRKCAP capacitor will be this blocks' static consumption, which is kept low (a 4.7 µF capacitor will provide > 6.5 V gate drive for 300 ms).

If a coast mode was selected then obviously the D flip-flop latches a 0 on its output, holding off the gate drives, allowing the normal power-down circuitry to operate.

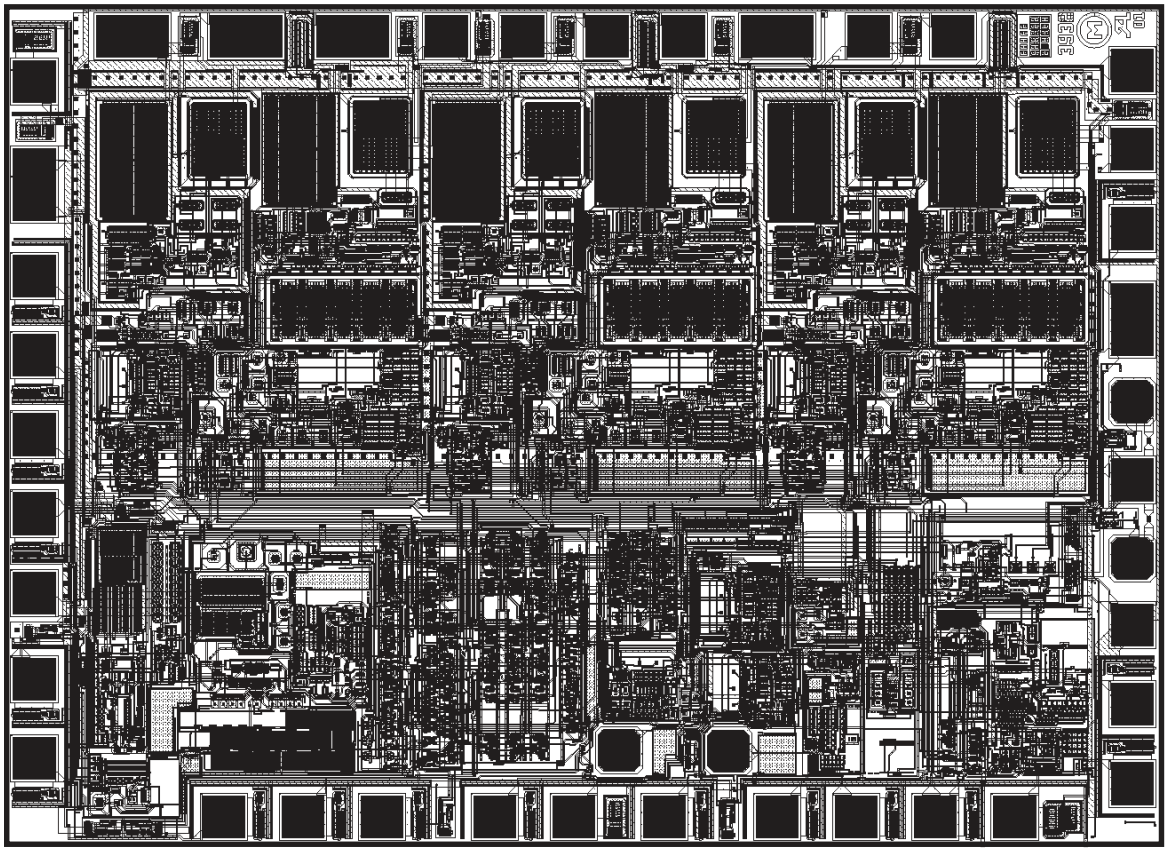


Figure 8 – A3932 die layout

CONCLUSION

A new three-phase motor controller design, the A3932 has been described (die layout shown in figure 8), with key circuit features highlighted. Some of the trade-offs often made in IC design to balance function, die size/package and process design constraints/opportunities have been discussed also.

The market for high-power 3-phase BLDC motors continues to expand, pushing the further development of the presented techniques. Higher operating voltages and gate-drive capabilities, as well as better diagnostic capabilities for safety-critical applications, will fuel the push to smaller geometries and 'smarter' processes and design techniques.

REFERENCES

1. Allegro™ MicroSystems LLC A3933 datasheet.
2. High-voltage integrated circuits for off-line power applications by C. Diazzi (chapter 8 of Smart Power Applications – B. Murari, F. Bertotti & G. A Vignola (Eds) – Springer 1996.