Low-Noise, High-Precision, Programmable Linear Hall-Effect Sensor IC

with Regulated Supply, Advanced Temperature Compensation, and High-Bandwidth (240 kHz) Analog Output

FEATURES AND BENEFITS

- 240 kHz nominal bandwidth achieved via proprietary packaging and chopper stabilization techniques
- On-board supply regulator with reverse-battery protection
- Proprietary segmented linear temperature compensation (TC) technology provides a typical accuracy of 1% over the full operating temperature range
- Customer-programmable, high-resolution offset and sensitivity trim
- Factory-programmed sensitivity and quiescent output voltage TC with extremely stable temperature performance
- High-sensitivity Hall element for maximum accuracy
- Extremely low noise and high resolution achieved via proprietary Hall element and low-noise amplifier circuits

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PACKAGE: 4-pin SIP (suffix KT)

TN Leadform

Not to scale

TH Leadform

Contact Allegro about legacy leadform options

DESCRIPTION

The Allegro™ A1367 programmable linear Hall-effect current sensor IC has been designed to achieve high accuracy and resolution without compromising bandwidth. This goal is achieved through new proprietary linearly interpolated temperature compensation technology that is programmed at the Allegro factory and provides sensitivity and offset that are virtually flat across the full operating temperature range. Temperature compensation is performed in the digital domain with integrated EEPROM technology while maintaining a 240 kHz bandwidth analog signal path, making this device ideal for HEV inverter, DC-to-DC converter, and electric power steering (EPS) applications.

This ratiometric Hall-effect sensor IC provides a voltage output that is proportional to the applied magnetic field. The customer can configure the sensitivity and quiescent (zero field) output voltage through programming on the VCC and output pins, to optimize performance in the end application. The quiescent output voltage is user-adjustable, around 50% (bidirectional configuration) or 10% (unidirectional configuration) of the supply voltage, V_{CC}, and the output sensitivity is adjustable within the range of 0.6 to 6.4 mV/G.

The sensor IC incorporates a highly sensitive Hall element with a BiCMOS interface integrated circuit that employs a low-

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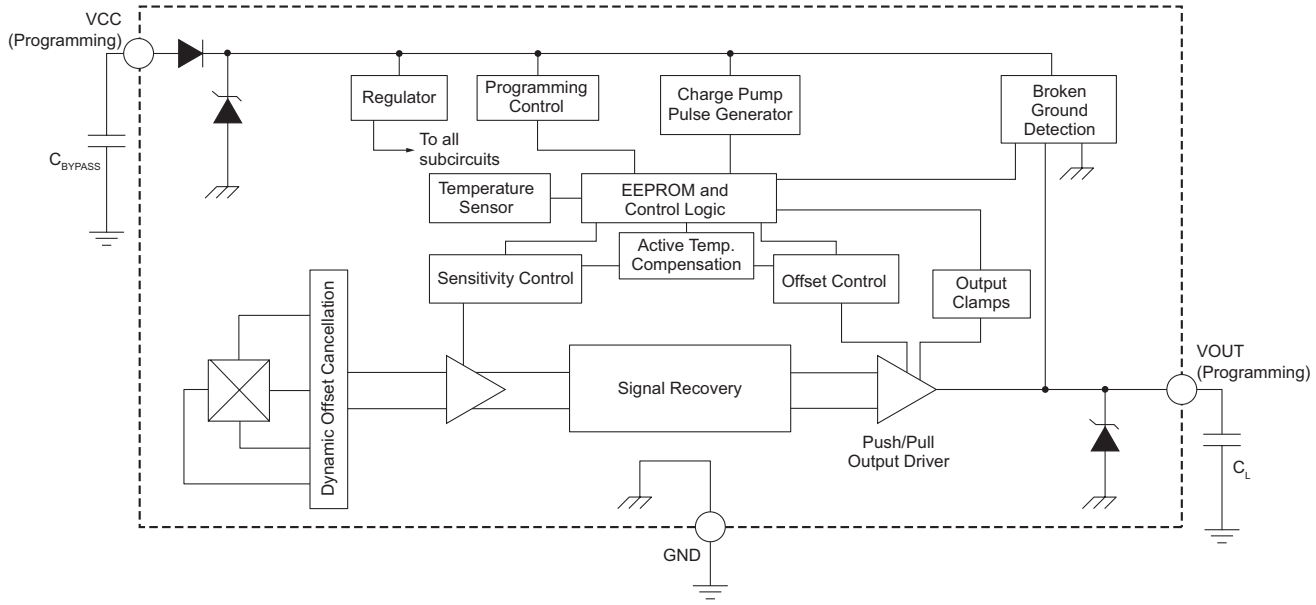

Functional Block Diagram

FEATURES AND BENEFITS (continued)

- Patented circuits suppress IC output spiking during fast current step inputs
- Open circuit detection on ground pin (broken wire)
- Selectable sensitivity range between 0.6 and 6.4 mV/G through use of coarse sensitivity program bits
- User-selectable ratiometric behavior of sensitivity, quiescent voltage, and clamps (ratiometry can be disabled), for simple interface with application A-to-D converter (ADC)
- Precise recoverability after temperature cycling
- Output voltage clamps provide short-circuit diagnostic capabilities
- Wide ambient temperature range: –40°C to 150°C
- Immune to mechanical stress
- Extremely thin package: 1 mm case thickness
- AEC-Q100 automotive qualified

DESCRIPTION (continued)

noise small-signal high-gain amplifier, a clamped low-impedance output stage, and a proprietary, high-bandwidth dynamic offset cancellation technique. These advances in Hall-effect technology work together to provide an industry-leading sensing resolution at the full 240 kHz bandwidth. Broken ground wire detection as well as user-selectable output voltage clamps also are built into this device for high reliability in automotive applications.

Device parameters are specified across an extended ambient temperature range: –40°C to 150°C. The A1367 sensor IC is provided in an extremely thin case (1 mm thick), 4-pin SIP (single in-line package, suffix KT) that is lead (Pb) free, with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number [1]	Leadform	Package	Packing [2]	Sensitivity Range [3] (mV/G)
A1367LKTTN-1B-T	TN (Straight)	4-pin SIP	4000 pieces per 13-inch reel	SENS_COARSE 00: 0.6 to 1.3
A1367LKTTN-2B-T [4]	TN (Straight)	4-pin SIP	4000 pieces per 13-inch reel	SENS_COARSE 01: 1.3 to 2.9
A1367LKTTN-2U-T [4]	TN (Straight)	4-pin SIP	4000 pieces per 13-inch reel	SENS_COARSE 01: 1.3 to 2.9
A1367LKTTN-5B-T [4]	TN (Straight)	4-pin SIP	4000 pieces per 13-inch reel	SENS_COARSE 10: 2.9 to 6.4

[1] TH package leadform options available.
[2] Contact Allegro for additional packing options.
[3] Allegro recommends against changing Coarse Sensitivity settings when programming devices that will be used in production. Each A1367 has been factory temperature compensated at a specific sensitivity range, and changing the coarse bits setting could cause sensitivity drift through temperature range ($\Delta Sens_{TC}$) to exceed specified limits.
[4] Part variants A1367LKTTN-2B-T, A1367LKTTN-2U-T, and A1367LKTTN-5B-T are in production but have been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status change date: April 1, 2024. Last-time buy date: July 31, 2024.

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ALLEGRO microsystems
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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		15	V
Reverse Supply Voltage	V_{RCC}	T_J(max) should not be exceeded	–15	V
Forward Output Voltage	V_{OUT}	$V_{OUT} < V_{CC} + 2$ V	16	V
Reverse Output Voltage	V_{ROUT}	Difference between V_{CC} and output should not exceed 20 V	–6	V
Output Source Current	$I_{OUT(source)}$	VOUT to GND	2.8	mA
Output Sink Current	$I_{OUT(sink)}$	VCC to VOUT	10	mA
Maximum Number of EEPROM Write Cycles	$EEPROM_{w(max)}$		100	cycle
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C

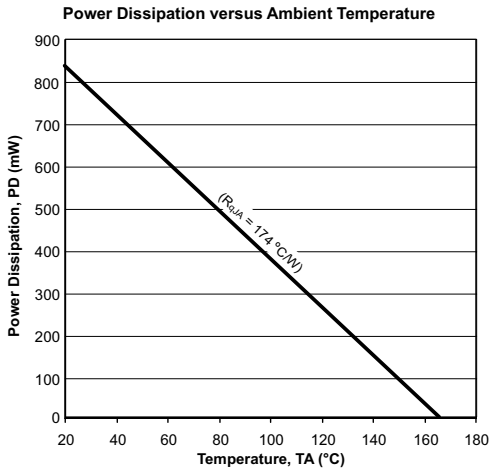
ESD RATINGS

Characteristic	Symbol	Test Conditions	Value	Unit
Human Body Model	V_{HBM}	Per AEC-Q100	±4.5	kV
Charged Device Model	V_{CDM}	Per AEC-Q100	±1	kV

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 1-layer PCB with exposed copper limited to solder pads	174	°C/W

*Additional thermal information available on the Allegro website



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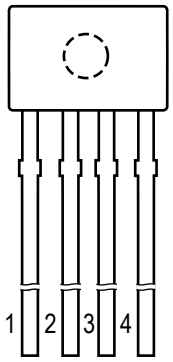
PINOUT DIAGRAM AND TERMINAL LIST



KT Package Pinout Diagram

(Ejector pin mark on opposite side)

Terminal List Table

Number	Name	Function
1	VCC	Input Power Supply, use bypass capacitor to connect to ground; also used for programming
2	VOUT	Output Signal, also used for programming
3	NC	No connection; connect to GND for optimal ESD performance
4	GND	Ground

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OPERATING CHARACTERISTICS: Valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{CC}	No load on VOUT	–	11	16.25	mA
Power-On Time [2]	t_{PO}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF, Sens = 2 mV/G, constant magnetic field of 400 G	–	80	–	µs
Temperature Compensation Power-On Time [2]	t_{TC}	T_A = 150°C, C_{BYPASS} = open, C_L = 1 nF, Sens = 2 mV/G, constant magnetic field of 400 G	–	146	–	µs
Power-On Reset Voltage [2]	V_{PORH}	T_A = 25°C, V_{CC} rising	3.75	4	4.2	V
	V_{PORL}	T_A = 25°C, V_{CC} falling	–	3.5	–	V
Power-On Reset Hysteresis	V_{PORHYS}	T_A = 25°C	–	500	–	mV
Power-On Reset Release Time [2]	t_{PORR}	T_A = 25°C, V_{CC} rising	–	32	–	µs
Power-On Reset Analog Delay	t_{PORA}	T_A = 25°C, V_{CC} rising	–	46	–	µs
Supply Zener Clamp Voltage	V_z	T_A = 25°C, I_{CC} = 30 mA	18	21	–	V
Internal Bandwidth	BW_i	Small signal –3 dB, C_L = 1 nF, T_A = 25°C	–	240	–	kHz
Chopping Frequency [3]	f_C	T_A = 25°C	–	1	–	MHz
OUTPUT CHARACTERISTICS						
Propagation Delay Time [2]	t_{pd}	T_A = 25°C, magnetic field step of 400 G, C_L = 1 nF, Sens = 2 mV/G	–	1.1	–	µs
Rise Time [2]	t_r	T_A = 25°C, magnetic field step of 400 G, C_L = 1 nF, Sens = 2 mV/G	–	2.4	–	µs
Response Time [2]	$t_{RESPONSE}$	T_A = 25°C, magnetic field step of 400 G, C_L = 1 nF, Sens = 2 mV/G, measurement of 80% input to 80% output	–	1.8	–	µs
		T_A = 25°C, magnetic field step of 400 G, C_L = 1 nF, Sens = 2 mV/G, measurement of 90% input to 90% output	–	2.2	–	µs
Delay to Clamp [2]	t_{CLP}	T_A = 25°C, magnetic field step from 800 to 1200 G, C_L = 1 nF, Sens = 2 mV/G	–	10	–	µs
Output Voltage Clamp [4]	$V_{CLP(HIGH)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	4.55	–	4.85	V
	$V_{CLP(LOW)}$	T_A = 25°C, $R_{L(PULLUP)}$ = 10 kΩ to VCC	0.15	–	0.45	V
Output Saturation Voltage [2]	$V_{SAT(HIGH)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	4.7	–	–	V
	$V_{SAT(LOW)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to VCC	–	–	400	mV
Broken Wire Voltage [2]	$V_{BRK(HIGH)}$	T_A = 25°C, $R_{L(PULLUP)}$ = 10 kΩ to VCC	–	V_{CC}	–	V
	$V_{BRK(LOW)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	–	100	–	mV
Noise [5]	V_N	T_A = 25°C, CL = 1 nF, BW_f = BW_i	–	1.4	_	mG/√(Hz)
		T_A = 25°C, CL = 1 nF, Sens = 2 mV/G, BW_f = BW_i	–	12.6	_	mV_{p-p}
		T_A = 25°C, CL = 1 nF, Sens = 2 mV/G, BW_f = BW_i	–	2.1	_	mV_{RMS}

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OPERATING CHARACTERISTICS (continued): Valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
OUTPUT CHARACTERISTICS (continued)						
DC Output Resistance	R_{OUT}		–	3	–	Ω
Output Load Resistance	$R_{L(PULLUP)}$	VOUT to VCC	4.7	–	–	kΩ
	$R_{L(PULLDWN)}$	VOUT to GND	4.7	–	–	kΩ
Output Load Capacitance [6]	C_L	VOUT to GND	–	1	10	nF
Output Slew Rate [7]	SR	Sens = 2 mV/G, C_L = 1 nF	–	480	–	V/ms
QUIESCENT VOLTAGE OUTPUT ($V_{OUT(Q)}$) [2]						
Initial Unprogrammed Quiescent Voltage Output [2][8]	$V_{OUT(QBI)init}$	T_A = 25°C	2.4	2.5	2.6	V
	$V_{OUT(QU)init}$	T_A = 25°C	0.45	0.5	0.55	V
Quiescent Voltage Output Programming Range [2][4][9]	$V_{OUT(QBI)PR}$	T_A = 25°C	2.35	–	2.65	V
	$V_{OUT(QU)PR}$	T_A = 25°C	0.4	–	0.6	V
Quiescent Voltage Output Programming Bits [10]	QVO		–	9	–	bit
Average Quiescent Voltage Output Programming Step Size [2][11][12]	$Step_{VOUT(Q)}$	T_A = 25°C	0.95	1.15	1.4	mV
Quiescent Voltage Output Programming Resolution [2][13]	$Err_{PGVOUT(Q)}$	T_A = 25°C	–	±0.5 × $Step_{VOUT(Q)}$	–	mV
SENSITIVITY (Sens) [2]						
Initial Unprogrammed Sensitivity [8]	$Sens_{init}$	SENS_COARSE = 00, T_A = 25°C	–	1	–	mV/G
		SENS_COARSE = 01, T_A = 25°C	–	2.2	–	mV/G
		SENS_COARSE = 10, T_A = 25°C	–	4.7	–	mV/G
Sensitivity Programming Range [4][9]	$Sens_{PR}$	SENS_COARSE = 00, T_A = 25°C	0.6	–	1.3	mV/G
		SENS_COARSE = 01, T_A = 25°C	1.3	–	2.9	mV/G
		SENS_COARSE = 10, T_A = 25°C	2.9	–	6.4	mV/G
Coarse Sensitivity Programming Bits [14]	SENS_COARSE		–	2	–	bit
Fine Sensitivity Programming Bits [10]	SENS_FINE		–	9	–	bit
Average Fine Sensitivity and Temperature Compensation Programming Step Size [2][14][15]	$Step_{SENS}$	SENS_COARSE = 00, T_A = 25°C	2.4	3.2	4.1	µV/G
		SENS_COARSE = 01, T_A = 25°C	5	6.6	8.5	µV/G
		SENS_COARSE = 10, T_A = 25°C	11	14.2	18	µV/G
Sensitivity Programming Resolution [2][13]	Err_{PGSENS}	T_A = 25°C	–	±0.5 × $Step_{SENS}$	–	µV/G
FACTORY-PROGRAMMED SENSITIVITY TEMPERATURE COEFFICIENT						
Sensitivity Temperature Coefficient [2]	TC_{SENS}	T_A = 150°C, T_A = –40°C, calculated relative to 25°C	–	0	–	%/°C
Sensitivity Drift Through Temperature Range [2][9][15]	$\Delta Sens_{TC}$	T_A = 25°C to 150°C	–2	–	2	%
		T_A = –40°C to 25°C	–3.5	–	3.5	%
Average Sensitivity Temperature Compensation Step Size	$Step_{SENSTC}$	T_A = –40°C to 150°C	2 × $Step_{SENS}$			µV/G

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
FACTORY-PROGRAMMED QUIESCENT VOLTAGE OUTPUT TEMPERATURE COEFFICIENT						
Quiescent Voltage Output Temperature Coefficient [2]	TC_{QVO}	T_A = 150°C, T_A = –40°C, calculated relative to 25°C	–	0	–	mV/°C
Quiescent Voltage Output Drift Through Temperature Range [2][9][15]	$\Delta V_{OUT(Q)TC}$	T_A = 25°C to 150°C; SENS_COARSE = 00 or 01	–10	–	10	mV
		T_A = 25°C to 150°C; SENS_COARSE = 10	–15	–	15	mV
		T_A = –40°C to 25°C	–30	–	30	mV
Average Quiescent Voltage Output Temperature Compensation Step Size	$Step_{QVOTC}$		–	2.3	–	mV
LOCK BIT PROGRAMMING						
EEPROM Lock Bit	EELOCK		–	1	–	bit
ERROR COMPONENTS						
Linearity Sensitivity Error [2][16]	Lin_{ERR}		–1	< ±0.25	1	%
Symmetry Sensitivity Error [2]	Sym_{ERR}		–1	< ±0.25	1	%
Ratiometry Quiescent Voltage Output Error [2][17]	$Rat_{ERRVOUT(Q)}$	Through supply voltage range (relative to V_{CC} = 5 V ±5%); SENS_COARSE = 00	–0.8	±0.15	0.8	%
		Through supply voltage range (relative to V_{CC} = 5 V ±5%); SENS_COARSE = 01	–0.9	±0.15	0.9	%
		Through supply voltage range (relative to V_{CC} = 5 V ±5%); SENS_COARSE = 10	–1.2	±0.25	1.2	%
Ratiometry Sensitivity Error [2][17]	$Rat_{ERRSens}$	Through supply voltage range (relative to V_{CC} = 5 V ±5%)	–1	< ±0.5	1	%
Ratiometry Clamp Error [2][18]	Rat_{ERRCLP}	Through supply voltage range (relative to V_{CC} = 5 V ±5%), T_A = 25°C	–	< ±1	–	%
Sensitivity Drift Due to Package Hysteresis [2]	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling, 25°C to 150°C and back to 25°C	–	±0.6	–	%
Sensitivity Drift Over Lifetime [19]	$\Delta Sens_{LIFE}$	T_A = 25°C, shift after AEC Q100 grade 0 qualification testing	–	±1	–	%

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] See Characteristic Definitions section.
[3] f_C varies up to approximately ±20% over the full operating ambient temperature range, T_A, and process.
[4] Sens, $V_{OUT(Q)}$, $V_{CLP(LOW)}$, and $V_{CLP(HIGH)}$ scale with V_{CC} due to ratiometry.
[5] Noise, measured in mV_{PP} and in mV_{RMS}, is dependent on the sensitivity of the device.
[6] Output stability is maintained for capacitive loads as large as 10 nF.
[7] High-to-low transition of output voltage is a function of external load components.
[8] Raw device characteristic values before any programming.
[9] Exceeding the specified ranges will cause sensitivity and Quiescent Voltage Output drift through the temperature range to deteriorate beyond the specified values.
[10] Refer to Functional Description section.
[11] Step size is larger than required, in order to provide for manufacturing spread. See Characteristic Definitions section.
[12] Non-ideal behavior in the programming DAC can cause the step size at each significant bit rollover code to be greater than twice the maximum specified value of $Step_{VOUT(Q)}$ or $Step_{SENS}$.
[13] Overall programming value accuracy. See Characteristic Definitions section.
[14] Each A1367 part number is factory programmed and temperature compensated at a different coarse sensitivity setting. Changing coarse bits setting could cause sensitivity drift through temperature range, $\Delta Sens_{TC}$, to exceed specified limits.
[15] Allegro will be testing and temperature compensating each device at 150°C. Allegro will not be testing devices at –40°C. Temperature compensation codes will be applied based on characterization data.
[16] Linearity applies to output voltage ranges of ±2 V from the quiescent output for bidirectional devices.
[17] Percent change from actual value at V_{CC} = 5 V, for a given temperature, through the supply voltage operating range.
[18] Percent change from actual value at V_{CC} = 5 V, T_A = 25°C, through the supply voltage operating range.
[19] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits. Cannot be guaranteed. Drift is a function of customer application conditions. Please contact Allegro MicroSystems for further information.

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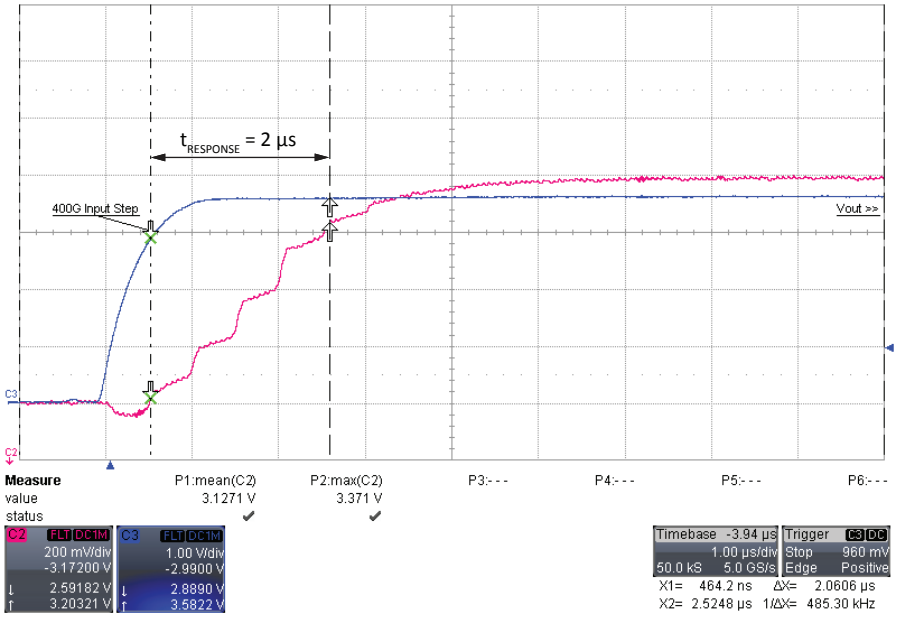
CHARACTERISTIC PERFORMANCE DATA

Response Time ($t_{RESPONSE}$)

400 G Excitation Signal with 10%-90% rise time = 1 µs

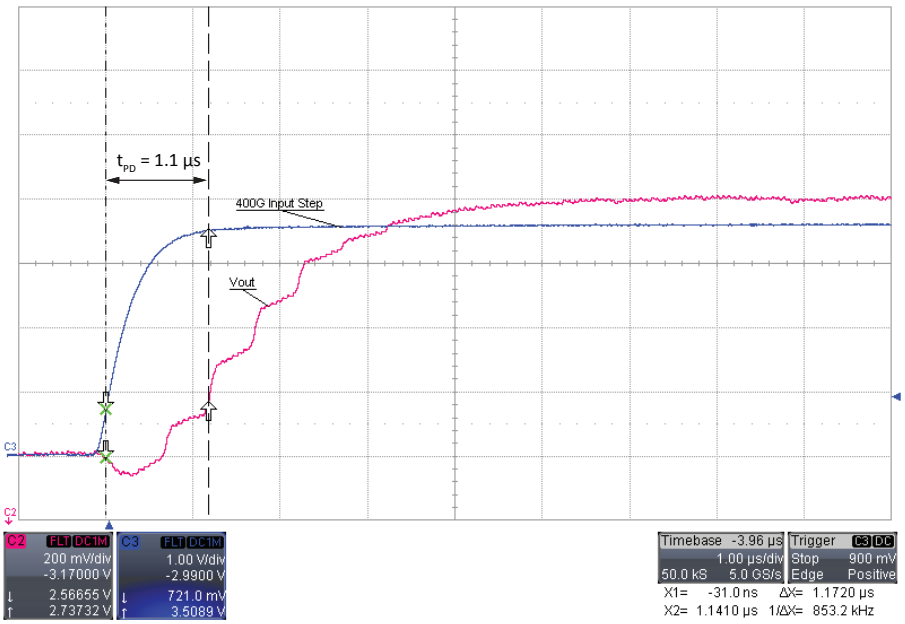
Response time (80% input to 80% output) = 2.06 µs, Sensitivity = 2 mV/G, C_{BYPASS} = 0.1 µF, C_L = 1 nF



Propagation Delay (t_{PD})

400 G Excitation Signal with 10%-90% rise time = 1 µs

Sensitivity = 2 mV/G, C_{BYPASS} = 0.1 µF, C_L = 1 nF



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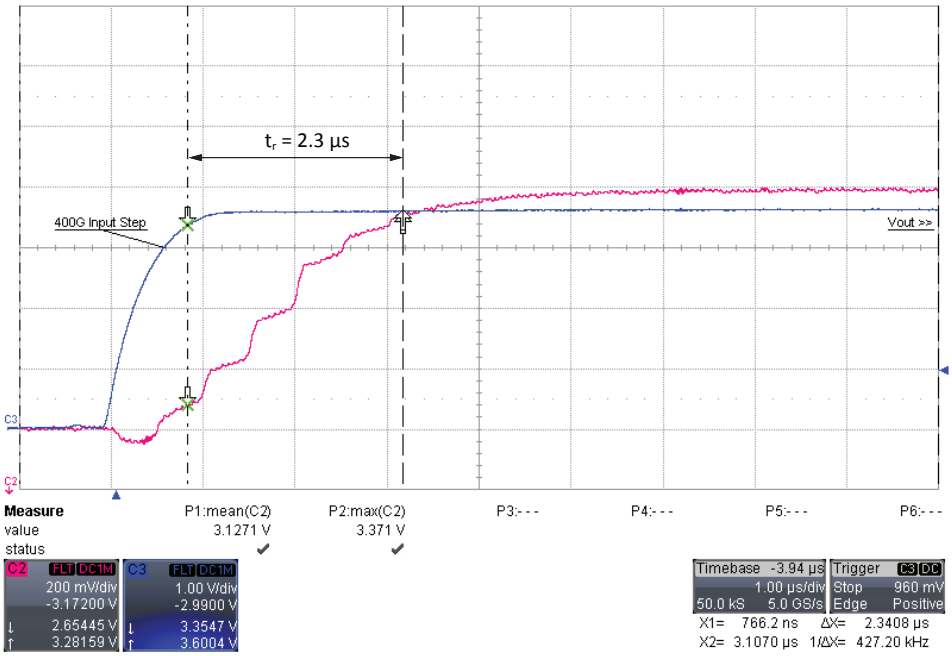
CHARACTERISTIC PERFORMANCE DATA (continued)

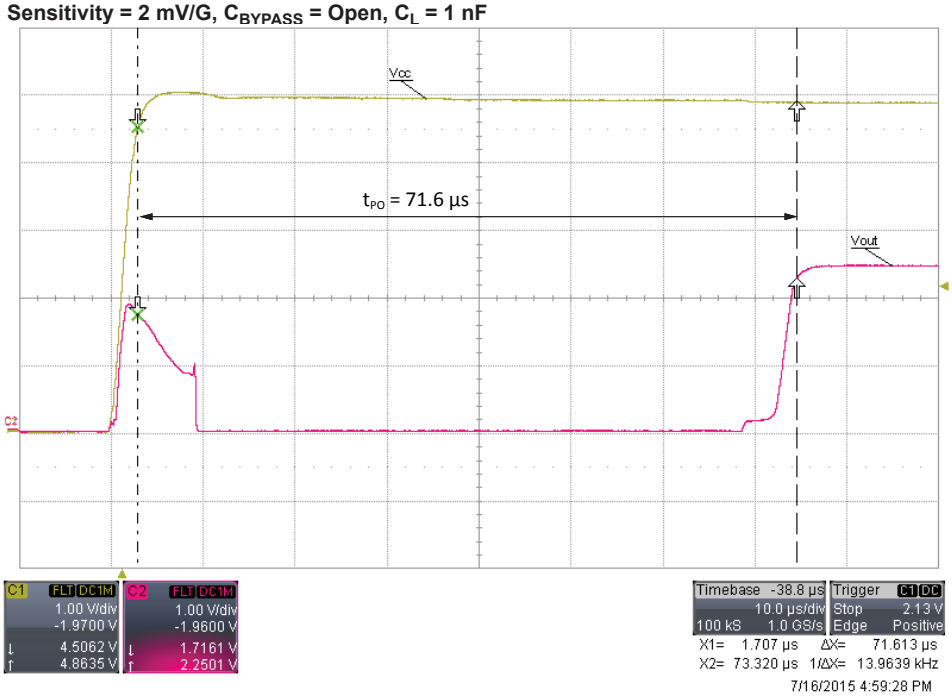
Rise Time (t_r)

400 G Excitation Signal with 10%-90% rise time = 1 µs
Sensitivity = 2 mV/G, C_{BYPASS} = 0.1 µF, C_L = 1 nF



Power-On Time (t_{PO})

400 G Constant Excitation Signal with t_{PO} = 81 µs
Sensitivity = 2 mV/G, C_{BYPASS} = Open, C_L = 1 nF



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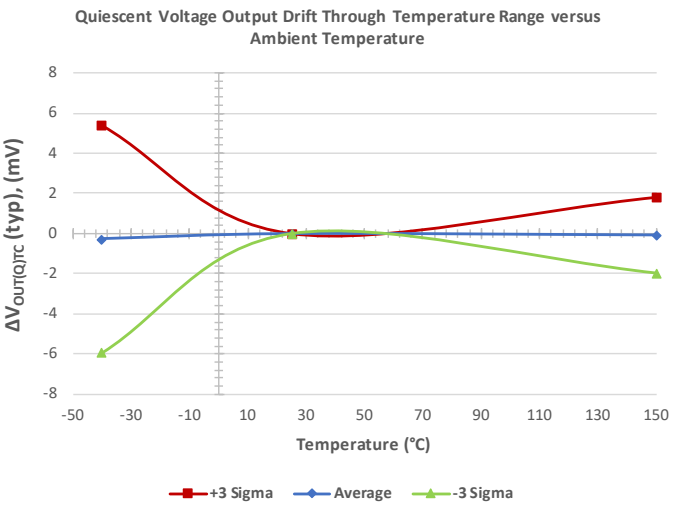
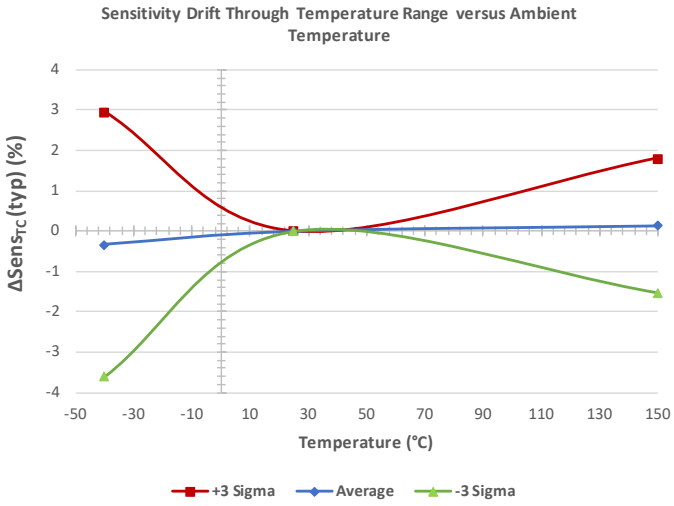
CHARACTERISTIC PERFORMANCE DATA (continued)

A1367LKTTN-1B-T





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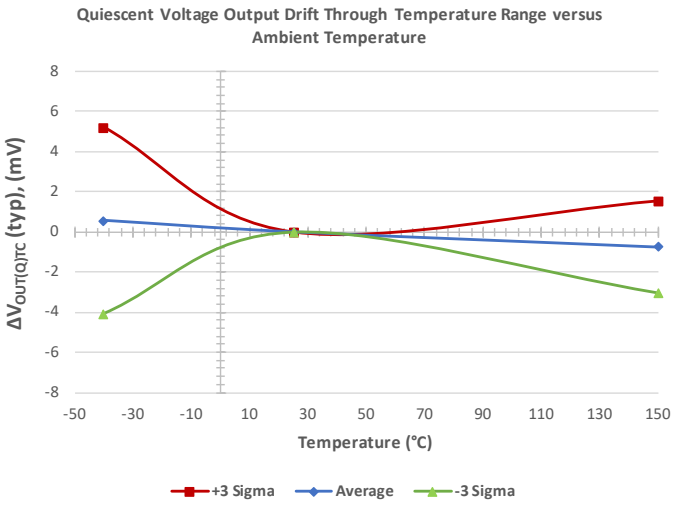

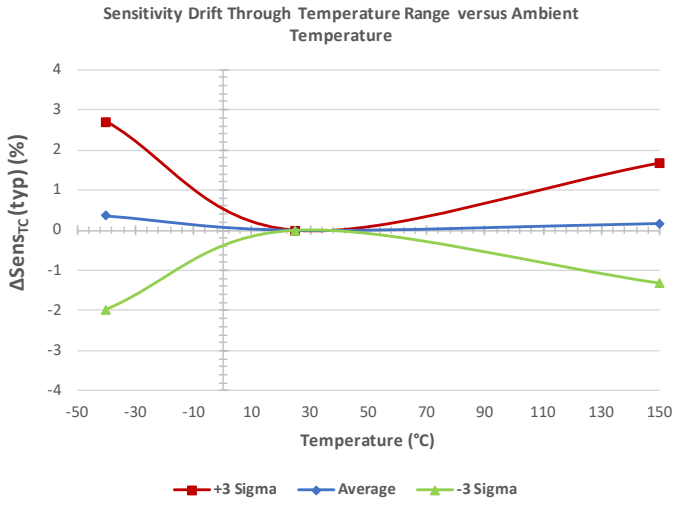

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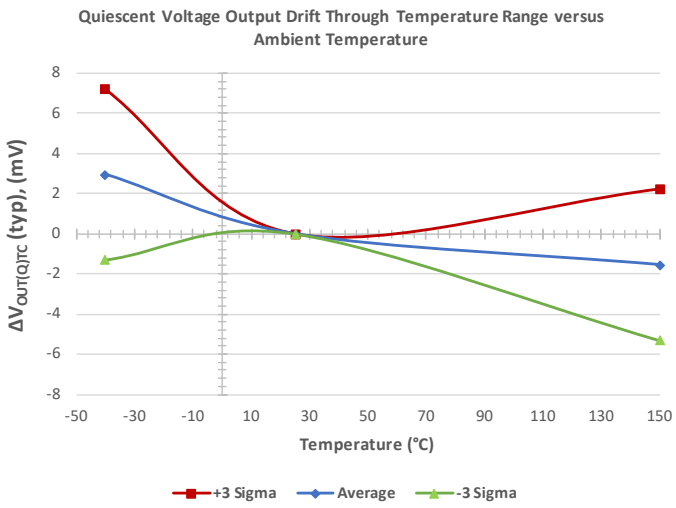
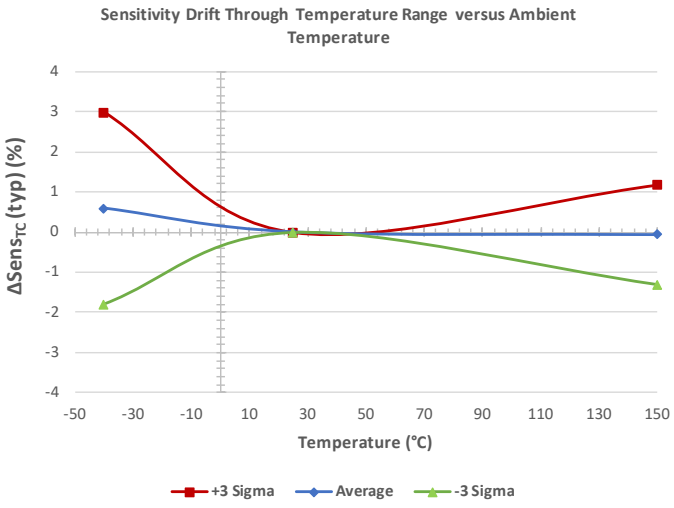
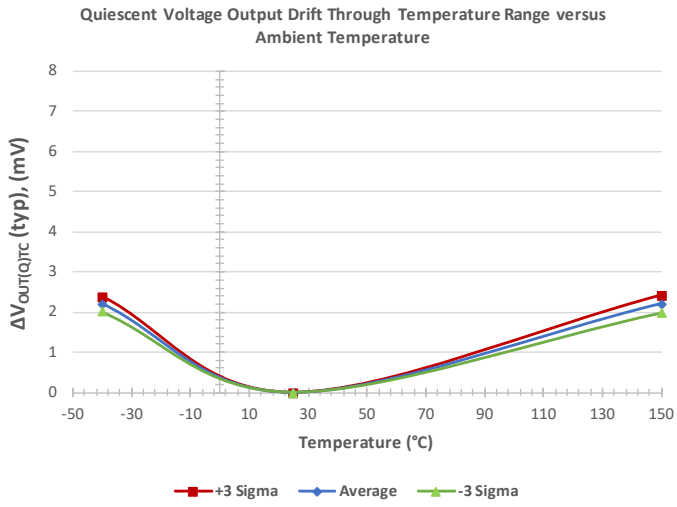
CHARACTERISTIC PERFORMANCE DATA (continued)

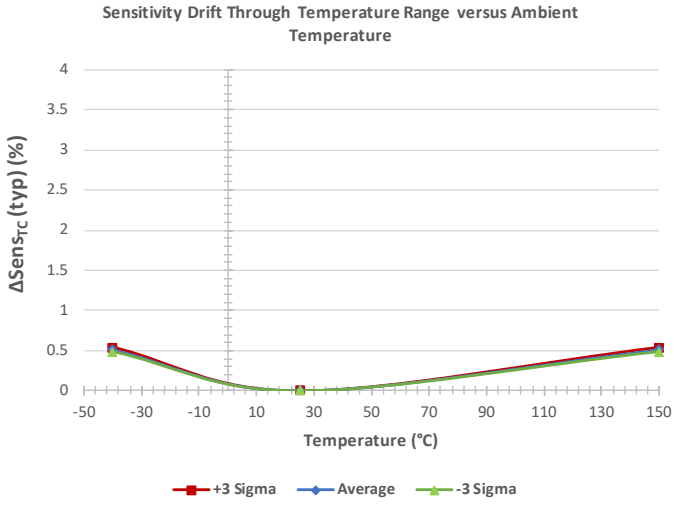
A1367LKTTN-5B-T





A1367LKTTN-2U-T





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CHARACTERISTIC DEFINITIONS

Power-On Time (t_{PO})

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

Power-On Time (t_{PO}) is defined as: the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage ($V_{CC(min)}$) as shown in Figure 1.

Temperature Compensation Power-On Time (t_{TC})

After Power-On Time (t_{PO}) elapses, t_{TC} is also required before a valid temperature compensated output.

Propagation Delay (t_{pd})

The time interval between a) when the applied magnetic field reaches 20% of its final value, and b) when the output reaches 20% of its final value (see Figure 2).

Rise Time (t_r)

The time interval between a) when the sensor IC reaches 10% of its final value, and b) when it reaches 90% of its final value (see Figure 2).

Response Time ($t_{RESPONSE}$)

The time interval between a) when the applied magnetic field reaches 80% of its final value, and b) when the sensor reaches 80% of its output corresponding to the applied magnetic field (see Figure 3). The 90%-90% is also shown in the Electrical Characteristics table.

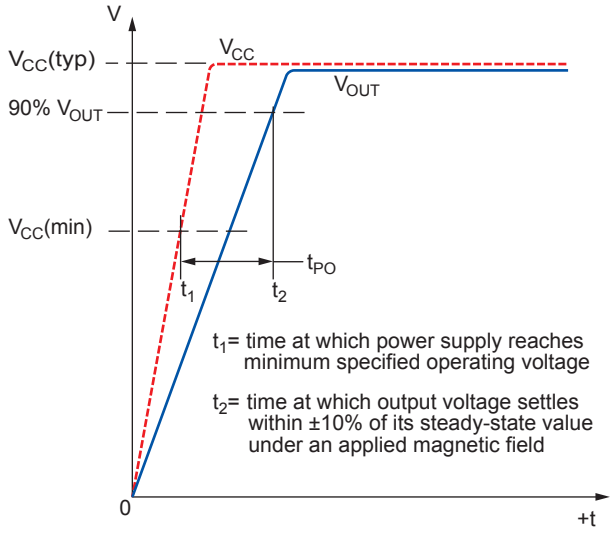

Figure 1: Power-On Time Definition

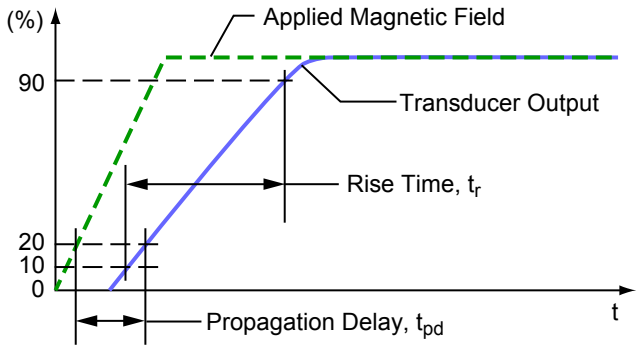

Figure 2: Propagation Delay and Rise Time Definitions

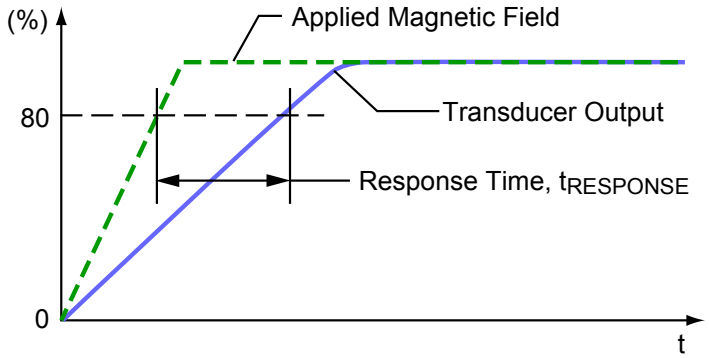

Figure 3: Response Time Definition

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Delay to Clamp (t_{CLP})

A large magnetic input step may cause the clamp to overshoot its steady-state value. The Delay to Clamp (t_{CLP}) is defined as: the time it takes for the output voltage to settle within ±1% of its steady-state value, after initially passing through its steady-state voltage, as shown in Figure 4.

Quiescent Voltage Output ($V_{OUT(Q)}$)

In the quiescent state (no significant magnetic field: B = 0 G), the output ($V_{OUT(Q)}$) has a constant ratio to the supply voltage (V_{CC}) throughout the entire operating ranges of V_{CC} and ambient temperature (T_A).

Initial Unprogrammed Quiescent Voltage Output ($V_{OUT(Q)init}$)

Before any programming, the Quiescent Voltage Output ($V_{OUT(Q)}$) has a nominal value of V_{CC} / 2, as shown in Figure 5.

Quiescent Voltage Output Programming Range ($V_{OUT(Q)PR}$)

The Quiescent Voltage Output ($V_{OUT(Q)}$) can be programmed within the Quiescent Voltage Output Range limits: $V_{OUT(Q)PR(min)}$ and $V_{OUT(Q)PR(max)}$. Exceeding the specified Quiescent Voltage Output Range will cause Quiescent Voltage Output Drift Through Temperature Range ($\Delta V_{OUT(Q)TC}$) to deteriorate beyond the specified values, as shown in Figure 5.

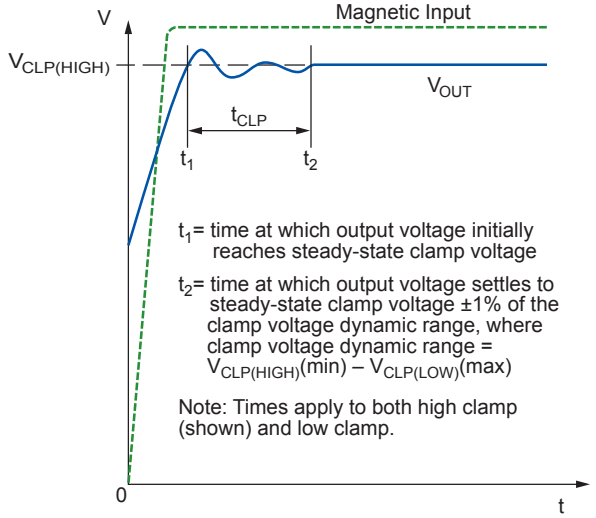

Figure 4: Delay to Clamp definition

Average Quiescent Voltage Output Programming Step Size ($Step_{VOUT(Q)}$)

The Average Quiescent Voltage Output Progamming Step Size ($Step_{VOUT(Q)}$) is determined using the following calculation:

$$Step_{VOUT(Q)} = \frac{V_{OUT(Q)maxcode} - V_{OUT(Q)mincode}}{2^n - 1}, \quad (1)$$

where n is the number of available programming bits in the trim range, 9 bits, $V_{OUT(Q)maxcode}$ is at decimal code 255, and $V_{OUT(Q)mincode}$ is at decimal code 256.

Quiescent Voltage Output Programming Resolution ($Err_{PGVOUT(Q)}$)

The programming resolution for any device is half of its programming step size. Therefore, the typical programming resolution will be:

$$Err_{PGVOUT(Q)}(typ) = 0.5 \times Step_{VOUT(Q)}(typ) \quad (2)$$

Quiescent Voltage Output Temperature Coefficient (TC_{QVO})

Device $V_{OUT(Q)}$ changes as temperature changes, with respect to its programmed Quiescent Voltage Output Temperature Coefficient, TC_{QVO}. TC_{QVO} is programmed at 150°C and calculated relative to the nominal $V_{OUT(Q)}$ programming temperature of 25°C. TC_{QVO} (mV/°C) is defined as:

$$TC_{QVO} = [V_{OUT(Q)T2} - V_{OUT(Q)T1}][1/(T2 - T1)] \quad (3)$$

where T1 is the nominal $V_{OUT(Q)}$ programming temperature of

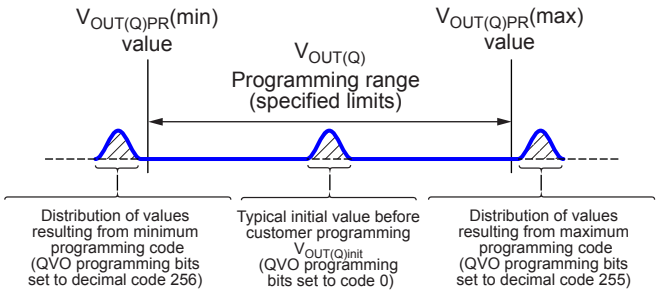

Figure 5: Quiescent Voltage Output Range definition

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25°C, and T2 is the TC_{QVO} programming temperature of 150°C. The expected $V_{OUT(Q)}$ through the full ambient temperature range ($V_{OUT(Q)EXPECTED(TA)}$) is defined as:

$$V_{OUT(Q)EXPECTED}(T_A) = V_{OUT(Q)T1} + TC_{QVO}(T_A - T1) \quad (4)$$

$V_{OUT(Q)EXPECTED(TA)}$ should be calculated using the actual measured values of $V_{OUT(Q)T1}$ and TC_{QVO} rather than programming target values.

Quiescent Voltage Output Drift Through Temperature Range ($\Delta V_{OUT(Q)TC}$)

Due to internal component tolerances and thermal considerations, the Quiescent Voltage Output ($V_{OUT(Q)}$) may drift from its nominal value through the operating ambient temperature (T_A). The Quiescent Voltage Output Drift Through Temperature Range ($\Delta_{VOUT(Q)TC}$) is defined as:

$$D_{VOUT(Q)TC} = V_{OUT(Q)(TA)} - V_{OUT(Q)EXPECTED(TA)} \quad (5)$$

$\Delta V_{OUT(Q)TC}$ should be calculated using the actual measured values of $\Delta V_{OUT(Q)(TA)}$ and $\Delta V_{OUT(Q)EXPECTED(TA)}$ rather than programming target values.

Sensitivity (Sens)

The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied.

Conversely, the application of a north polarity field decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mv/G), of the device, and it is defined as:

$$Sens = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{BPOS - BNEG}, \quad (6)$$

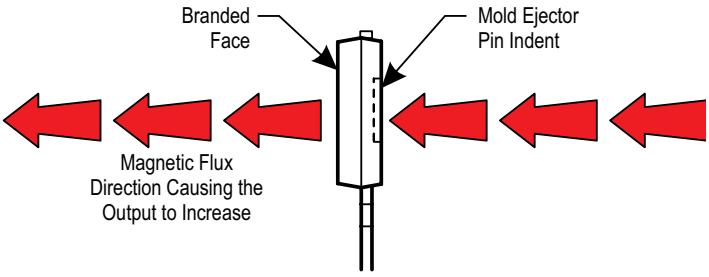

Figure 6: Magnetic Flux Polarity

where BPOS and BNEG are two magnetic fields with opposite polarities.

Initial Unprogrammed Sensitivity ($Sens_{init}$)

Before any programming, Sensitivity has a nominal value that depends on the SENS_COARSE bits setting. Each A1367 variant has a different SENS_COARSE setting.

Sensitivity Programming Range ($Sens_{PR}$)

The magnetic sensitivity (Sens) can be programmed around its initial value within the sensitivity range limits: $Sens_{PR}$(min) and $Sens_{PR}$(max). Exceeding the specified Sensitivity Range will cause Sensitivity Drift Through Temperature Range ($\Delta Sens_{TC}$) to deteriorate beyond the specified values. Refer to the Quiescent Voltage Output Range section for a conceptual explanation of how value distributions and ranges are related.

Average Fine Sensitivity Programming Step Size ($Step_{SENS}$)

Refer to the Average Quiescent Voltage Output Programming Step Size section for a conceptual explanation.

Sensitivity Programming Resolution (Err_{PGSENS})

Refer to the Quiescent Voltage Output Programming Resolution section for a conceptual explanation.

Sensitivity Temperature Coefficient (TC_{SENS})

Device sensitivity changes as temperature changes, with respect to its programmed sensitivity temperature coefficient, TC_{SENS}. TC_{SENS} is programmed at 150°C and is calculated relative to the nominal sensitivity programming temperature of 25°C. TC_{SENS} (%/°C) is defined as:

$$TC_{SENS} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\% \right) \left(\frac{1}{T2 - T1} \right), \quad (7)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the TC_{SENS} programming temperature of 150°C. The expected value of Sens over the full ambient temperature range, $Sens_{EXPECTED(TA)}$, is defined as:

$$Sens_{EXPECTED(TA)} = Sens_{T1} \times \left[100\% + \frac{TC_{SENS}(T_A - T1)}{100} \right] \quad (8)$$

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$Sens_{EXPECTED(TA)}$ should be calculated using the actual measured values of $Sens_{T1}$ rather than programming target values.

Sensitivity Drift Through Temperature Range ($\Delta Sens_{TC}$)

Second-order sensitivity temperature coefficient effects cause the magnetic sensitivity, Sens, to drift from its expected value over the operating ambient temperature range (T_A). The Sensitivity Drift Through Temperature Range ($\Delta Sens_{TC}$) is defined as:

$$\Delta Sens_{TC} = \frac{Sens_{TA} - Sens_{EXPECTED(TA)}}{Sens_{EXPECTED(TA)}} \times 100\% \quad . \qquad (9)$$

Sensitivity Drift Due to Package Hysteresis ($\Delta Sens_{PKG}$)

Package stress and relaxation can cause the device sensitivity at $T_A = 25°C$ to change during and after temperature cycling. The sensitivity drift due to package hysteresis ($\Delta Sens_{PKG}$) is defined as:

$$\Delta Sens_{PKG} = \frac{Sens_{(25°C)2} - Sens_{(25°C)1}}{Sens_{(25°C)1}} \times 100\% \quad , \qquad (10)$$

where $Sens_{(25°C)1}$ is the programmed value of sensitivity at $T_A = 25°C$, and $Sens_{(25°C)2}$ is the value of sensitivity at $T_A = 25°C$, after temperature cycling T_A up to 150°C and back to 25°C.

Linearity Sensitivity Error (Lin_{ERR})

The A1367 is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error

Linearity error is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity Error (%) is measured and defined as:

$$Lin_{ERRPOS} = \left(1 - \frac{Sens_{BPOS2}}{Sens_{BPOS1}}\right) \times 100\% \quad ,$$

$$Lin_{ERRNEG} = \left(1 - \frac{Sens_{BNEG2}}{Sens_{BNEG1}}\right) \times 100\% \quad , \qquad (11)$$

where:

$$Sens_{Bx} = \frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x} \quad , \qquad (12)$$

and BPOS*x* and BNEG*x* are positive and negative magnetic fields, with respect to the quiescent voltage output such that |BPOS2| = 2 × |BPOS1| and |BNEG2| = 2 × |BNEG1|.

Then:

$$Lin_{ERR} = \max(Lin_{ERRPOS}, Lin_{ERRNEG}) \quad . \qquad (13)$$

Symmetry Sensitivity Error (Sym_{ERR})

The magnetic sensitivity of an A1367 device is constant for any two applied magnetic fields of equal magnitude and opposite polarities. Symmetry Error, Sym_{ERR} (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{Sens_{BPOS}}{Sens_{BNEG}}\right) \times 100\% \quad , \qquad (14)$$

where $Sens_{Bx}$ is as defined in equation 12, and BPOSx and BNEGx are positive and negative magnetic fields such that |BPOSx| = |BNEGx|.

Ratiometry Error (Rat_{ERR})

The A1367 device features ratiometric output. This means that the Quiescent Voltage Output ($V_{OUT(Q)}$) magnetic sensitivity, Sens, and Output Voltage Clamp ($V_{CLP(HIGH)}$ and $V_{CLP(LOW)}$) are proportional to the Supply Voltage (V_{CC}). In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The ratiometric error in Quiescent Voltage Output, $Rat_{ERRVOUT(Q)}$ (%), for a given supply voltage (V_{CC}) is defined as:

$$Rat_{ERRVOUT(QBI)} = \left[1 - \frac{\left(\frac{V_{OUT(QBI)(VCC)}}{V_{OUT(QBI)(5V)}}\right)}{\frac{V_{CC}}{5\ V}}\right] \times 100\% \qquad (15)$$

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$Rat_{ERRVOUT(QU)}$ is defined in the same way as $Rat_{ERRVOUT(QBI)}$ with a factor of 1/5 multiplied.

$$Rat_{ERRVOUT(QU)} = \left[1 - \frac{\left(\frac{V_{OUT(QU)(VCC)}}{V_{OUT(QU)(5V)}} \right)}{\frac{V_{CC}}{5\ V}} \right] \times \frac{1}{5} \times 100\% \qquad (16)$$

This is to scale the ratiometry error of the unidirectional device so that it can be compared with the bidirectional device.

The ratiometric error in magnetic sensitivity, $Rat_{ERRSens}$ (%), for a given Supply Voltage (V_{CC}) is defined as:

$$Rat_{ERRSens} = \left(1 - \frac{Sens_{(VCC)} / Sens_{(5V)}}{V_{CC} / 5\ V} \right) \times 100\% \quad . \qquad (17)$$

The ratiometric error in the clamp voltages, Rat_{ERRCLP} (%), for a given supply voltage (V_{CC}) is defined as:

$$Rat_{ERRCLP} = \left(1 - \frac{V_{CLP(VCC)} / V_{CLP(5V)}}{V_{CC} / 5\ V} \right) \times 100\% \ , \qquad (18)$$

where V_{CLP} is either $V_{CLP(HIGH)}$ or $V_{CLP(LOW)}$.

Power-On Reset Voltage (V_{POR})

On power-up, to initialize to a known state and avoid current spikes, the A1367 is held in Reset state. The Reset signal is disabled when V_{CC} reaches V_{PORH} and time t_{PORR} has elapsed, allowing the output voltage to go from a high-impedance state into normal operation. During power-down, the Reset signal is enabled when V_{CC} reaches V_{PORL}, causing the output voltage to go into a high-impedance state. (Note that a detailed description of POR can be found in the Functional Description section).

Power-On Reset Release Time (t_{PORR})

When V_{CC} rises to V_{PORH}, the Power-On Reset Counter starts. The A1367 output voltage will transition from a high-impedance state to normal operation only when the Power-On Reset Counter has reached t_{PORR} and V_{CC} has been maintained above V_{PORH}.

Output Saturation Voltage (V_{SAT})

When output voltage clamps are disabled, the output voltage can swing to a maximum of $V_{SAT(HIGH)}$ and to a minimum of $V_{SAT(LOW)}$.

Broken Wire Voltage (V_{BRK})

If the GND pin is disconnected (broken wire event), output voltage will go to $V_{BRK(HIGH)}$ (if a load resistor is connected to VCC) or to $V_{BRK(LOW)}$ (if a load resistor is connected to GND).

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FUNCTIONAL DESCRIPTION

Programming Sensitivity and Quiescent Voltage Output

Sensitivity and $V_{OUT(Q)}$ can be adjusted by programming SENS_FINE and QVO bits, as illustrated in Figure 7 and Figure 8.

Customers should not program sensitivity or $V_{OUT(Q)}$ beyond the maximum or minimum programming ranges specified in the Operating Characteristics table. Exceeding the specified limits will cause the sensitivity and $V_{OUT(Q)}$ drift over the temperature range ($\Delta Sens_{TC}$ and $\Delta V_{OUT(Q)TC}$) to deteriorate beyond the specified values.

Programming sensitivity might cause a small drift in $V_{OUT(Q)}$. As a result, Allegro recommends programming sensitivity first, then $V_{OUT(Q)}$.

Coarse Sensitivity

Each A1367 variant is programmed to a different coarse sensitivity setting. Devices are tested, and temperature compensation is factory programmed under that specific coarse sensitivity setting. If the coarse sensitivity setting is changed by programming SENS_COARSE bits, Allegro cannot guarantee the specified sensitivity drift through temperature range limits ($\Delta Sens_{TC}$).

Memory-Locking Mechanisms

The A1367 is equipped with two distinct memory-locking mechanisms:

- ***Default Lock*** At power-up, all registers of the A1367 are locked by default. EEPROM and volatile memory cannot be read or written. To disable Default Lock, a specific 30 bit customer access code has to be written to address 0x24 within Access Code Timeout (t_{ACC} = 8 ms) from power-up. After doing so, registers can be accessed. If VCC is power-cycled, the Default Lock will automatically be re-enabled. This ensures that during normal operation, memory content will not be altered due to unwanted glitches on VCC or the output pin.
- ***Lock Bit*** After EEPROM has been programmed by the user, the EELOCK bit can be set high and VCC power-cycled to permanently disable the ability to write any register. This will prevent the ability to disable Default Lock using the method described above. Note that after the EELOCK bit is set high and the VCC pin is power-cycled, you will not have the ability to clear the EELOCK bit or write any register.

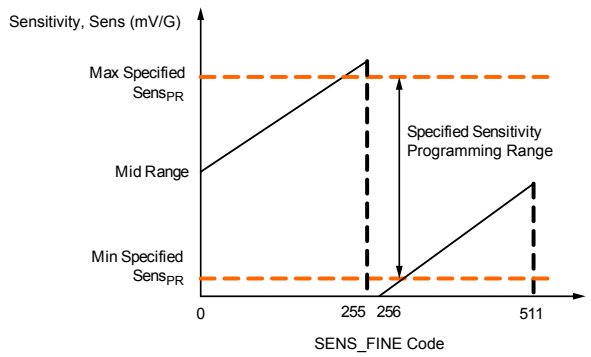

Figure 7: Device Sensitivity versus SENS_FINE Programmed Value

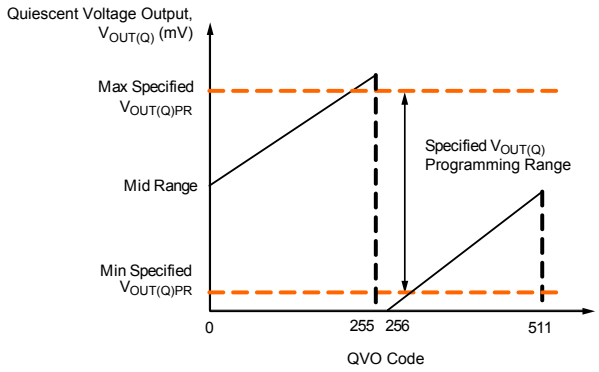

Figure 8: Device $V_{OUT(Q)}$ versus QVO Programmed Value

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Power-On Reset (POR) Operation

The descriptions in this section assume temperature = 25°C, no output load (R_L, C_L), and no significant magnetic field is present.

- ***Power-Up.*** At power-up, as V_{CC} ramps up, the output is in a high-impedance state. When V_{CC} crosses V_{PORH}, the output will go to $V_{CC}/2$ after t_{PORD}, where t_{PORD} = POR Release counter t_{PORR} + POR Analog delay t_{PORA}.
- ***V_{CC} drops below $V_{CC(min)}$ = 4.5 V.*** If V_{CC} drops below V_{PORL}, the output will be in a high-impedance state. If V_{CC} recovers and exceeds V_{PORH}, the output will go back to normal operation after t_{PORD}.

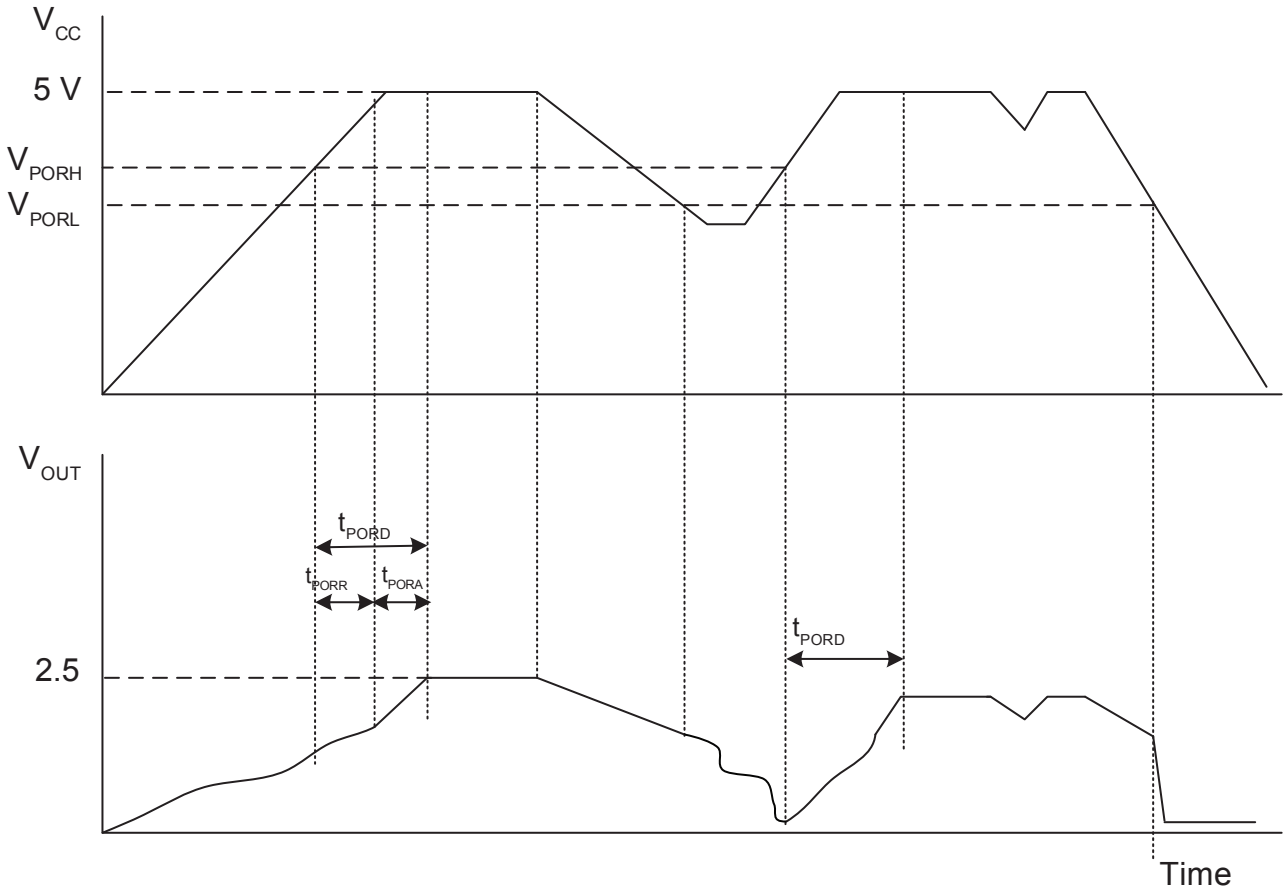

Figure 9: POR Operation

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Detecting Broken Ground Wire

If the GND pin is disconnected, node A becoming open (see Figure 11), the VOUT pin will go to a high-impedance state. The output voltage will go to $V_{BRK(HIGH)}$ if a load resistor $R_{L(PULLUP)}$ is connected to V_{CC} or to $V_{BRK(LOW)}$ if a load resistor $R_{L(PULLDWN)}$ is connected to GND. The device will not respond to any applied magnetic field.

If the ground wire is reconnected, the A1367 will resume normal operation.

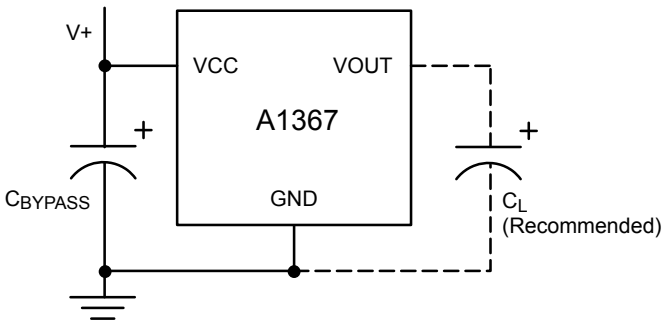

Figure 10: Typical Application Drawing

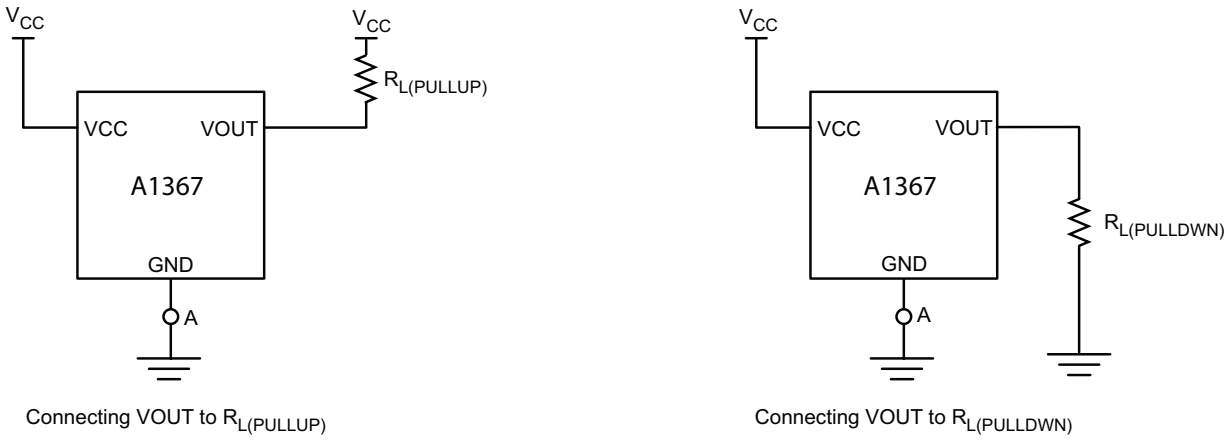

Figure 11: Connections for Detecting Broken Ground Wire

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Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for total accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip.

The technique removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal can then pass through a low-pass filter, while the modulated DC offset is suppressed. This high-frequency operation allows a greater sampling rate that results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and a proprietary, dynamic notch filter. The new Allegro filtering techniques are far more effective at suppressing chopper-induced signal noise compared to the previous generation of Allegro chopper-stabilized devices.

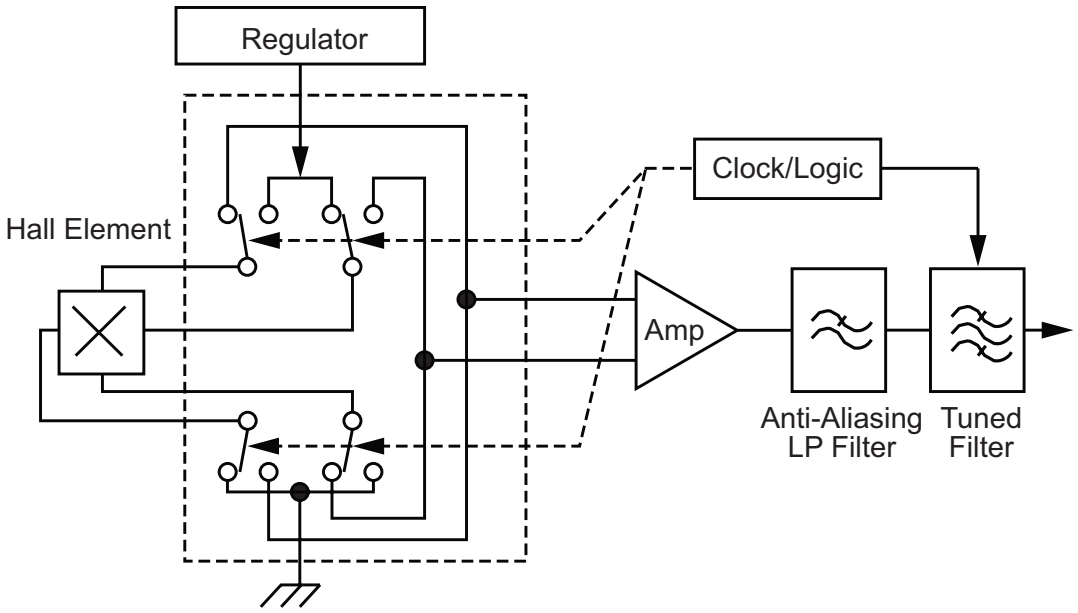

Figure 12: Concept of Chopper Stabilization

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PROGRAMMING GUIDELINES

Serial Communication

The serial interface allows an external controller to read and write registers, including EEPROM, in the A1367 using a point-to-point command/acknowledge protocol. The A1367 does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is no acknowledging from the A1367. If the command is a read, the A1367 responds by transmitting the requested data.

Serial interface timing parameters can be found in the Programming Levels table on page 22. Note that the external controller must avoid sending a Command frame that overlaps a Read Acknowledge frame.

The serial interface uses a Manchester-encoding-based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the A1367: Write Access Code, Write to Volatile Memory, Write to Non-Volatile Memory (EEPROM) and Read. One frame type, Read Acknowledge, is sent by the A1367 in response to a Read command.

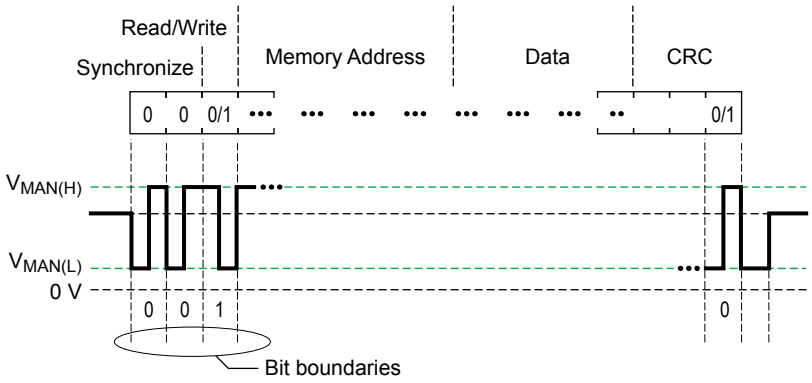

Figure 13: General Format for Serial Interface Commands

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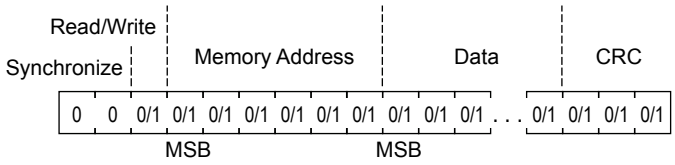
The A1367 device uses a three-wire programming interface, where VCC is used to control the program enable signal, data is transmitted on VOUT, and all signals are referenced to GND. This three-wire interface makes it possible to communicate with multiple devices with shared VCC and GND lines.

The four transactions (Write Access, Write to EEPROM, Write to Volatile Memory, and Read) are show in the figures on the following pages. To initialize any communication, V_{CC} should be increased to a level above V_{prgH}(min) without exceeding V_{prgH}(max). At this time, VOUT is disabled and acts as an input.

After program enable is asserted, the external controller must drive the output low in a time less than t_d. This prevents the device interpreting any false transients on VOUT as data pulses. After the command is completed, V_{CC} is reduced below V_{prgL}, back to normal operating level. Also, the output is enabled and responds to magnetic input.

When performing a Write to EEPROM transaction, the A1367 requires a delay of t_w to store the data into the EEPROM. The device will respond with a high-to-low transition on VOUT to indicate the Write to EEPROM sequence is complete.

When sending multiple command frames, it is necessary to toggle the program enable signal on VCC. After the first command frame is completed, and V_{CC} remains at V_{prgH}, the device will ignore any subsequent pulses on the output. When the program enable signal is brought below $V_{prgL(max)}$, the output will respond to the magnetic input. To send the next command, the program enable signal is increased to V_{prgH}.



Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read / Write	0	[As required] Write operation
		1	[As required] Read operation
6	Address	0/1	[Read/Write] Register address (volatile memory or EEPROM)
30	Data	0/1	24 data bits and 6 ECC bits. For a read command frame the data consists of 30 bits: [29:26] Don't Care, [25:24] ECC Pass/Fail, and [23:0] Data. Where bit 0 is the LSB. For a write command frame the data consists of 30 bits: [29:24] Don't Care and [23:0] Data. Where bit 0 is the LSB.
3	CRC	0/1	Bits to check the validity of frame.

Figure 14: Command Frame General Format

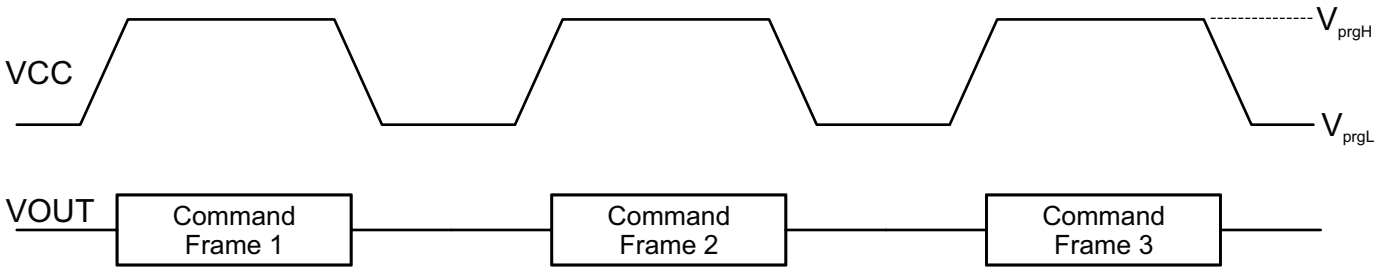


Figure 15: Format for Sending Multiple Transactions

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Programming Parameters, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
Program Enable Voltage (High)	V_{prgH}	Program enable signal high level on VCC	8	8.25	8.5	V
Program Enable Voltage (Low)	V_{prgL}	Program enable signal low level on VCC	V_{CC}	–	6	V
Output Enable Delay	t_e	External capacitance (C_{LX}) on VOUT may increase the Output Enable Delay	–	125	–	µs
Program Time Delay	t_d		–	15	–	µs
Program Write Delay	t_w		–	20	–	ms
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on VOUT	4	5	V_{CC}	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on VOUT	0	–	1	V
Bit Rate	t_{BITR}	Communication rate	0.3	80	100	kbps
Bit Time	t_{BIT}	Data bit pulse width at 100 kbps	–	(10)	–	µs

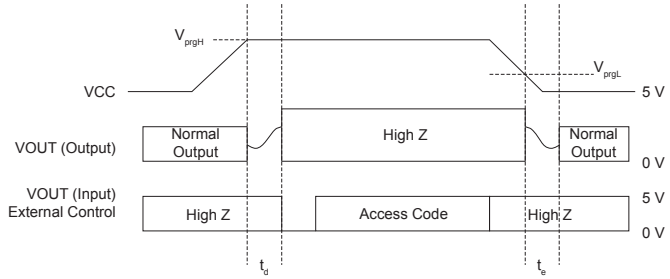

Figure 16: Write Access Code

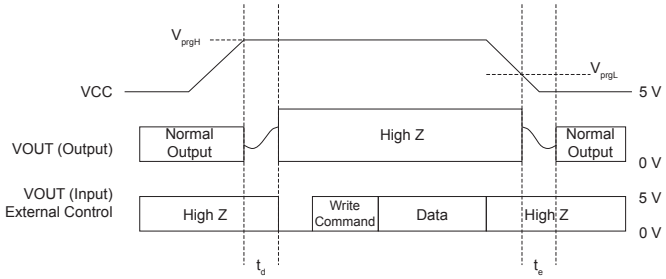

Figure 17: Write Volatile Memory

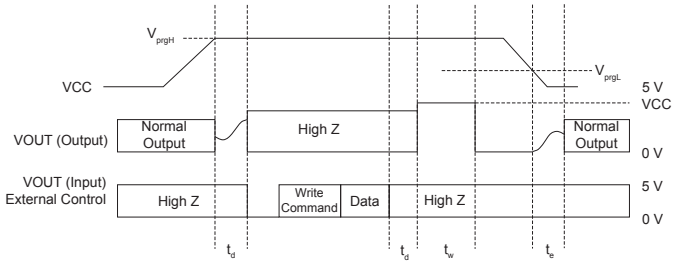

Figure 18: Write Non-Volatile Memory

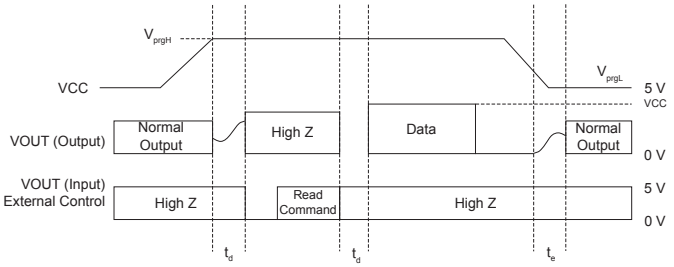

Figure 19: Read

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Read (Controller to A1367)

The fields for the Read command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 1 for read)
- CRC (3 bits)

Figure 20 shows the sequence for a Read command.

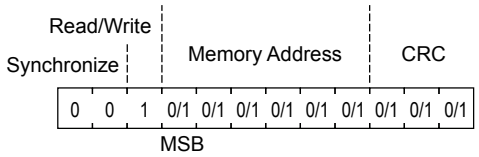

Figure 20: Read Sequence

Read Acknowledge (A1367 to Controller)

The fields for the data return frame are:

- Sync (2 zero bits)
- Data (30 bits):
  - □ [29:26] Don't Care
  - □ [25:24] ECC Pass/Fail
  - □ [23:0] Data

Figure 21 shows the sequence for a Read Acknowledge. Refer to the Detecting ECC Error section for instructions on how to detect Read/Write Synchronize Memory Address Data (30 bits) and ECC failure.

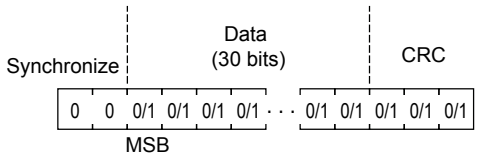

Figure 21: Read Acknowledgement Sequence

Write (Controller to A1367)

The fields for the Write command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits, ADDR[5] is for EEPROM, 1 for register; refer to the address map)
- Data (30 bits):
  - □ [29:24] Don't Care
  - □ [23:0] Data
- CRC (3 bits)

Figure 22 shows the sequence for a Write command. Bits [29:24] are Don't Care because the A1367 automatically generates 6 ECC bits based on the content of bits [23:0]. These ECC bits will be stored in EEPROM at locations [29:24].

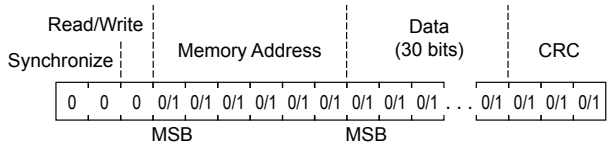

Figure 22: Write Sequence

Write Access Code (Controller to A1367)

The fields for the Access Code command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits, address 0x24 for Customer Access)
- Data (30 bits, 0x2C413737 for Customer Access)
- CRC (3 bits)

Figure 23 shows the sequence for an Access Code command.

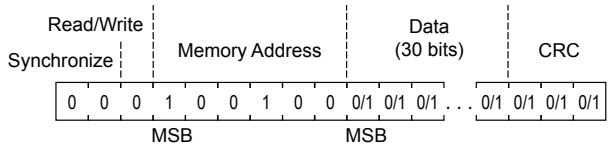

Figure 23: Write Access Code

The controller must open the serial communication with the A1367 device by sending an Access Code. It must be sent within Access Code Timeout, t_{ACC}, from power-up, or the device will be disabled for read and write access.

Access Codes Information

Name	Serial Interface Format	
	Register Address (Hex)	Data (Hex)
Customer	0x24	0x2C413737

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Memory Address Map

Address	Register Name	Parameter Name	Description	r/w	Bits	Location
0x02	ID_C	CUST_ID		r/w	24	23:0
0x03	SENSE_C	SENS_FINE	Sensitivity, fine adjustment	r/w	9	8:0
		SENS_COARSE [1]	Coarse sensitivity	r/w	2	10:9
		POL	Reverses output polarity	r/w	1	11
		RESERVED	Reserved scratch pad for SENS_FINE	r/w	9	20:12
		RESERVED	Reserved scratch pad for SENS_COARSE	r/w	2	22:21
		RESERVED	Reserved scratch pad for SENS polarity	r/w	1	23
0x04	QVO_C	QVO_FINE	Quiescent Output Voltage (QVO), fine adjustment	r/w	9	8:0
		UNI	Unidirectional bit	r/w	1	9
		CLAMP_EN	Enables output clamps high and low	r/w	1	10
		RATIOM_DIS	Ratiometry disable	r/w	1	11
		RESERVED	Reserved scratch pad for QVO_FINE	r/w	9	20:12
		RESERVED		r/w	3	23:21
0x06	COMCFG_C	DEV_LOCK	Bit to set the EELOCK (for new lock sequence)	r/w	1	0
		Unused		r/w	11	23:1

[1] SENS_COARSE[0..1] = 11 is factory reserved. Only 00, 01, and 10 are valid entries.

Enabling/Disabling Ratiometry

By default, this device has an output that is ratiometric, meaning that Quiescent Voltage Output ($V_{OUT(Q)}$) magnetic sensitivity, Sens, and Output Voltage Clamp ($V_{CLP(HIGH)}$ and $V_{CLP(LOW)}$) are proportional to the Supply Voltage (V_{CC}). There is an EEPROM bit (RATIOM_DIS) that can be used to disable the ratiometry of the output, making the above mentioned components of the output no longer proportional to V_{CC}. This bit can be found in the QVO_C register (0x04). Writing a 1 to this bit disables ratiometry; writing a 0 to this bit enables ratiometry.

EEPROM Cell Organization

Programming coefficients are stored in non-volatile EEPROM, which is separate from the digital subsystem, and accessed by the digital subsystem EEPROM Controller module. The EEPROM is organized as 30 bit wide words, each word is made up of 24 data bits and 6 ECC (Error Checking and Correction) check bits, stored as shown in table below.

EEPROM Bit	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15
Contents	C5	C4	C3	C2	C1	C0	D23	D22	D21	D20	D19	D18	D17	D16	D15

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

External EEPROM Word Bit Sequence; C# – Check Bit, D# – Data Bit

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Diagnostic Clamps

Diagnostic clamps can be enabled in EEPROM for this device. By writing a 1 to CLAMP_EN (bit 10 in QVO_C register (0x04)), the output voltage hits a maximum and minimum voltage that correspond to the specification Output Voltage Clamp in the above tables. Writing a 0 to this bit disables the clamps and allows the output to swing to the Output Saturation Voltage.

EEPROM Error Checking and Correction (ECC)

Hamming code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up.

The device always returns 30 bits.

The message received from controller is analyzed by the device EEPROM driver and ECC bits are added. The first 6 received bits from device to controller are dedicated to ECC.

Detecting ECC Error

If an uncorrectable error has occurred, bits 25:24 are set to 10, the VOUT pin will go to a high-impedance state, and the device will not respond to the applied magnetic field. To detect this high-impedance state, the circuit connection with $R_{L(PULLDWN)}$ shown in Figure 11 must be used and the output voltage will go to $V_{BRK(LOW)}$. The connection with $R_{L(PULLUP)}$ should not be used to detect this error.

EEPROM ECC Errors

Bits	Name	Description
29:26	–	No meaning
25:24	ECC	00 = No Error 01 = Error detected and message corrected 10 = Uncorrectable error 11 = No meaning
23:0	D[23:0]	EEPROM data

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PACKAGE OUTLINE DRAWINGS

For Reference Only - Not for Tooling Use

(Reference DWG-0000426, Rev. 2)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

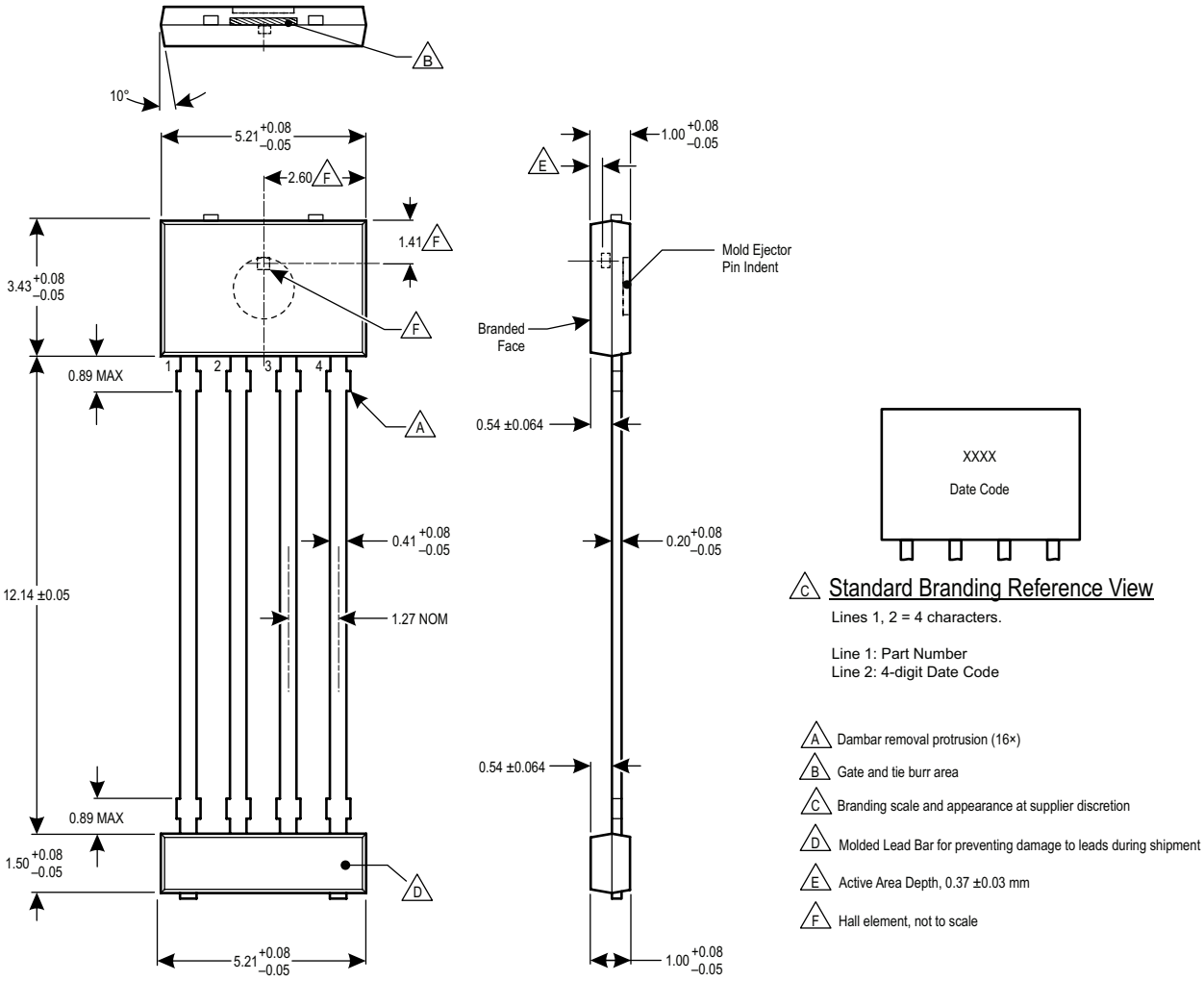

Figure 24: Package KT, 4-Pin SIP, TN Leadform

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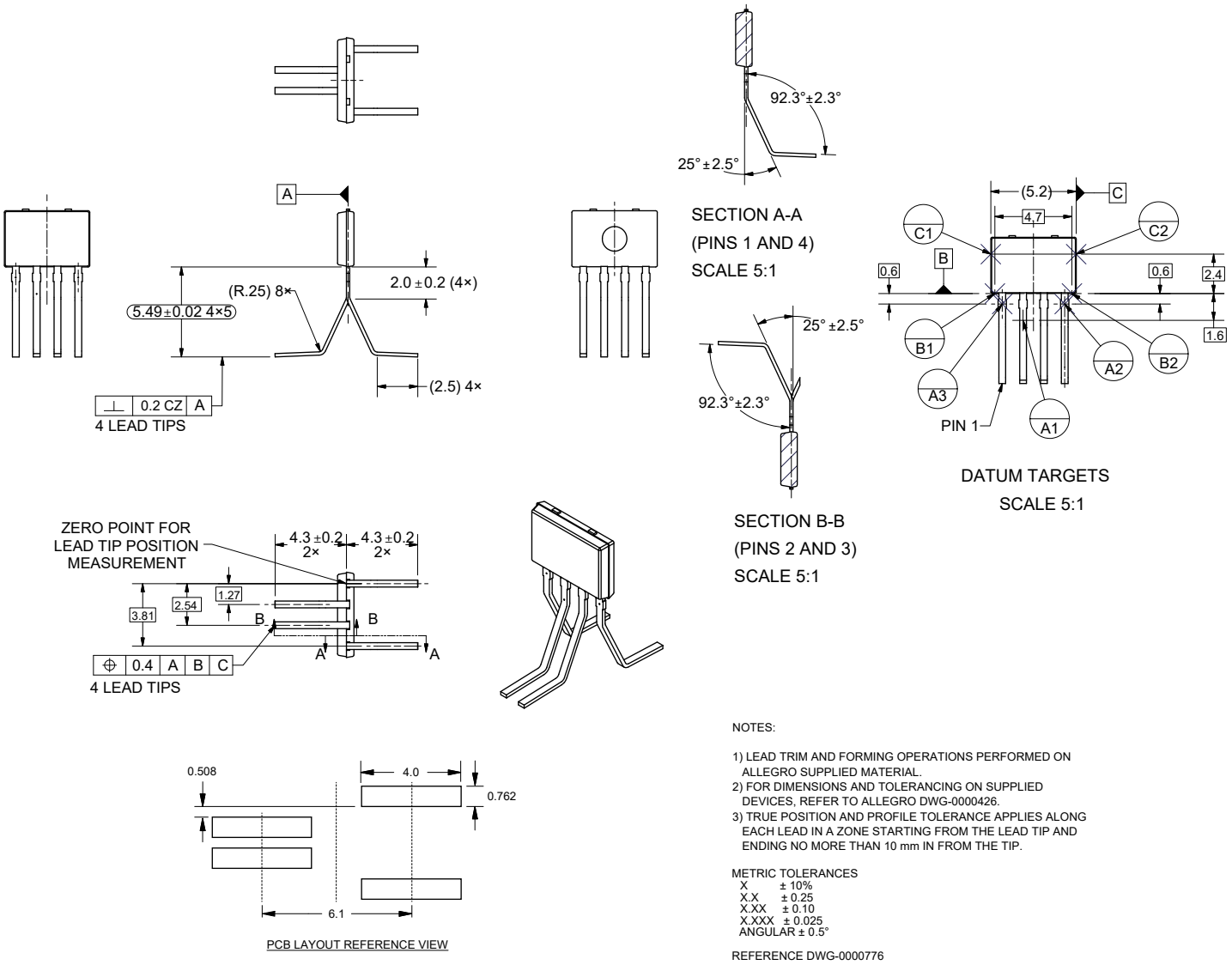

NOTES:

1) LEAD TRIM AND FORMING OPERATIONS PERFORMED ON ALLEGRO SUPPLIED MATERIAL.
2) FOR DIMENSIONS AND TOLERANCING ON SUPPLIED DEVICES, REFER TO ALLEGRO DWG-0000426.
3) TRUE POSITION AND PROFILE TOLERANCE APPLIES ALONG EACH LEAD IN A ZONE STARTING FROM THE LEAD TIP AND ENDING NO MORE THAN 10 mm IN FROM THE TIP.

METRIC TOLERANCES
X ± 10%
X.X ± 0.25
X.XX ± 0.10
X.XXX ± 0.025
ANGULAR ± 0.5°

REFERENCE DWG-0000776

Figure 25: Package KT, 4-Pin SIP, TH Leadform

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Revision History

Revision	Date	Description
–	March 9, 2016	Initial release
1	May 31, 2016	Updated Description (page 1), Features and Benefits (page 2), Noise (page 5), Quiescent Voltage Output Programming Range (page 6), Sensitivity Drift Due to Package Hysteresis (page 7), and Character Performance Data plots (pages 8-9).
2	August 19, 2016	Updated Selection Guide (page 2).
3	February 6, 2017	Corrected Functional Block Diagram (page 1).
4	November 13, 2017	Corrected Package Outline Drawing Standard Branding label (page 26).
5	May 23, 2018	Updated Supply Zener Clamp Voltage values (page 5).
6	December 4, 2018	Added TF and TG leadforms; updated Characteristic Performance Data plots (pages 10-11).
7	January 24, 2019	Updated footnote 7 (page 7).
8	April 26, 2019	Added TF and TG footprints
9	August 27, 2019	Added ESD ratings table (page 3)
10	September 30, 2020	Removed TF/TG leadforms and footprints (pages 1-2, 28-29); added TH leadform and footprint (pages 1, 28); updated package outline drawing (page 27)
11	March 31, 2021	Updated Lock Bit description (page 17).
12	April 6, 2022	Updated package drawing (page 27)
13	March 15, 2024	Part variants A1367LKTTN-2B-T, A1367LKTTN-2U-T, and A1367LKTTN-5B-T status changed to Last-Time Buy (page 2).

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