A4406

Constant On-Time Buck Regulator with External and Internal Linear Regulator

Last Time Buy

These parts are in production but have been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: April 1, 2024

Deadline for receipt of LAST TIME BUY orders: July 31, 2024

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, refer to the A4409KLPTR-T.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

A4406

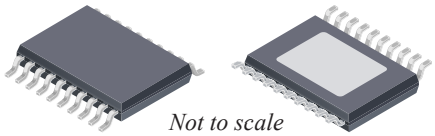
Constant On-Time Buck Regulator with External and Internal Linear Regulator

FEATURES AND BENEFITS

- AEC-Q100 Grade 0 qualified
- Internal buck pre-regulator followed by LDO outputs
- 5.5 to 36 V VIN operating range (50 V maximum); for start/stop, cold crank, and load dump requirements
- 2.2 MHz constant on-time buck regulator
- 50 V absolute maximum input voltage for surges
- Valley current sensing achieves shortest buck on-times
- 5.5 to 46 V input voltage range
- −40°C to 150°C junction temperature range
- Power-on reset (NPOR pin) with adjustable rising delay
- 5 V (V5P pin) internal low dropout tracking linear regulator with both overcurrent foldback and short-to-battery protection
- 3.3 V (V33 pin) external linear regulator DMOS driver with a programmable current limit (up to 500 mA) and overcurrent foldback protection

Continued on the next page…

PACKAGE: 20-pin TSSOP with exposed thermal pad (suffix LP)



Not to scale

DESCRIPTION

The A4406 is an automotive power management IC that uses a high frequency constant on-time 5.45 V pre-regulator to supply an internal 5 V linear regulator and a 3.3 V linear DMOS driver. Designed to supply CAN and microprocessor power supplies in high temperature environments, the A4406 is ideal for under hood applications. Efficient operation is achieved by using a buck pre-regulator to efficiently drop the input voltage before supplying the linear regulators; this reduces power dissipation and increases overall regulator efficiency.

The switching regulator is capable of operating at a nominal switching frequency of 2.2 MHz. The high switching frequency enables the customer to select low value inductors and ceramic capacitors while avoiding EMI in the AM frequency band.

Protection features include undervoltage lockout and thermal shutdown. The V5P output is protected from short-to-battery events. In case of a shorted load, all regulators feature overcurrent

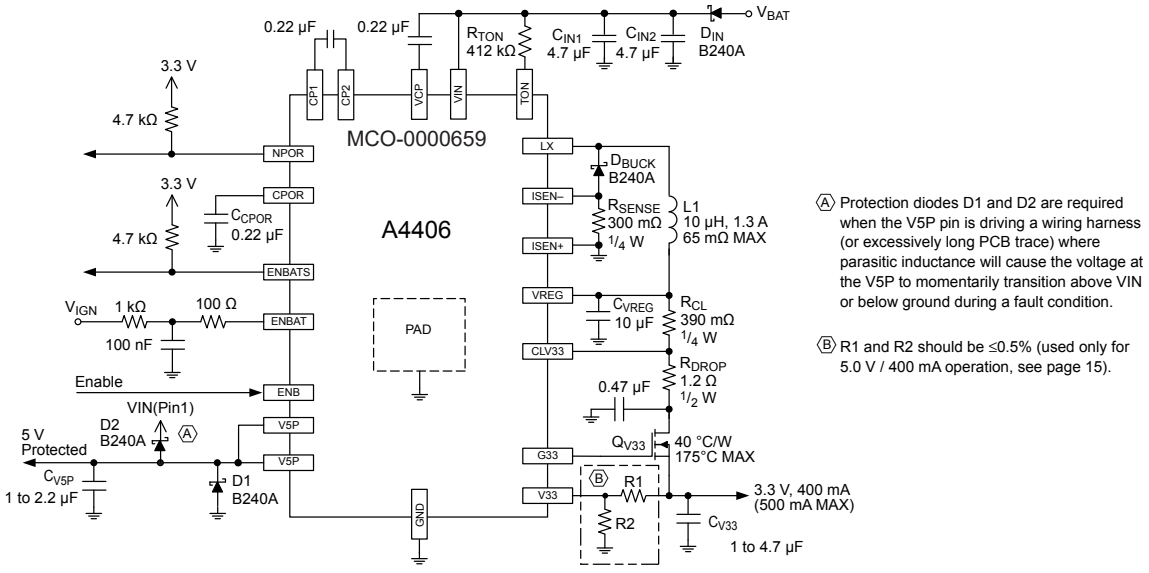
Continued on the next page…

APPLICATIONS:

Automotive Control Modules, such as:

- Electronic power steering (EPS)
- Transmission control (TCU)
- Antilock braking (ABS)
- Emissions control

Typical Application Circuit



Option with external LDO set to 3.3 V / 400 mA,
(Add R1 and R2 and remove R_{DROP} to set external LDO to 5.0 V / 400 mA)

Ⓐ Protection diodes D1 and D2 are required when the V5P pin is driving a wiring harness (or excessively long PCB trace) where parasitic inductance will cause the voltage at the V5P to momentarily transition above VIN or below ground during a fault condition.

Ⓑ R1 and R2 should be ≤0.5% (used only for 5.0 V / 400 mA operation, see page 15).

FEATURES AND BENEFITS (continued)

- Logic enable input (ENB pin)
- Ignition enable input (ENBAT pin)
- Ignition status indicator (ENBATS pin)
- Buck pulse-by-pulse overcurrent protection
- Buck LX short circuit protection (latched)
- Missing asynchronous diode protection (latched)
- Switcher (VREG pin), 3.3 V (V33 pin), and charge pump (VCP pin) undervoltage lockout protection (UVLO)
- Thermal shutdown protection (TSD)

DESCRIPTION (continued)

protection. The A4406 also features power-on-reset with adjustable delay for the microprocessor output.

The A4406 is supplied in a low profile (1.2 mm max) 20-pin TSSOP package with exposed thermal pad (suffix LP). The package is lead (Pb) free with 100% matte-tin leadframe plating

SELECTION GUIDE

Part Number	Packing
A4406KLPTR-T	4000 pieces per 13-in. reel

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
VIN Pin	V_{IN}		–0.3 to 50	V
LX Pin	V_{LX}		–0.3 to 50	V
		t < 250 ns	–1.5	V
VCP, CP1, and CP2 Pins	V_{VCP}, V_{CPx}		–0.3 to 60	V
ISEN– Pin	$V_{ISEN–}$		–0.5 to 1	V
ISEN+ Pin	V_{ISEN+}		–0.5 to 0.5	V
ENBAT Pin [2]	V_{ENBAT}		–0.3	V
ENBAT Pin Current	I_{ENBAT}		–50 to 50	mA
VREG Pin	V_{VREG}		–0.3 to 8	V
V33 Pin	V_{V33}		–0.3 to 7	V
G33 Pin [3]	V_{G33}		–0.3	V
CLV33 Pin	V_{CLV33}		–0.3 to 10	V
V5P Pin	V_{V5P}		–0.3 to V_{IN}+0.5	V
TON Pin	V_{TON}		–0.3 to 50	V
NPOR and CPOR Pins	V_{xPOR}		–0.3 to 7	V
ENB and ENBATS Pins	V_{EN}, V_{ENBATS}		–0.3 to 7	V
Operating Ambient Temperature	T_A	Range K	–40 to 135	°C
Junction Temperature	T_J(max)		–40 to 150	°C
Storage Temperature Range	T_{stg}		–40 to 150	°C

[1] Absolute maximum ratings are limiting values that should not be exceeded under worst case operating conditions or damage may occur.
[2] The ENBAT pin is internally clamped to approximately 8.5 V due to an ESD protection device.
[3] The G33 pin is internally clamped by an ESD protection device. Clamp voltages range from 10 V (min) to 15 V (max).

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Estimated on 4-layer PCB based on JEDEC standard	32	°C/W

*Additional thermal information available on the Allegro website.

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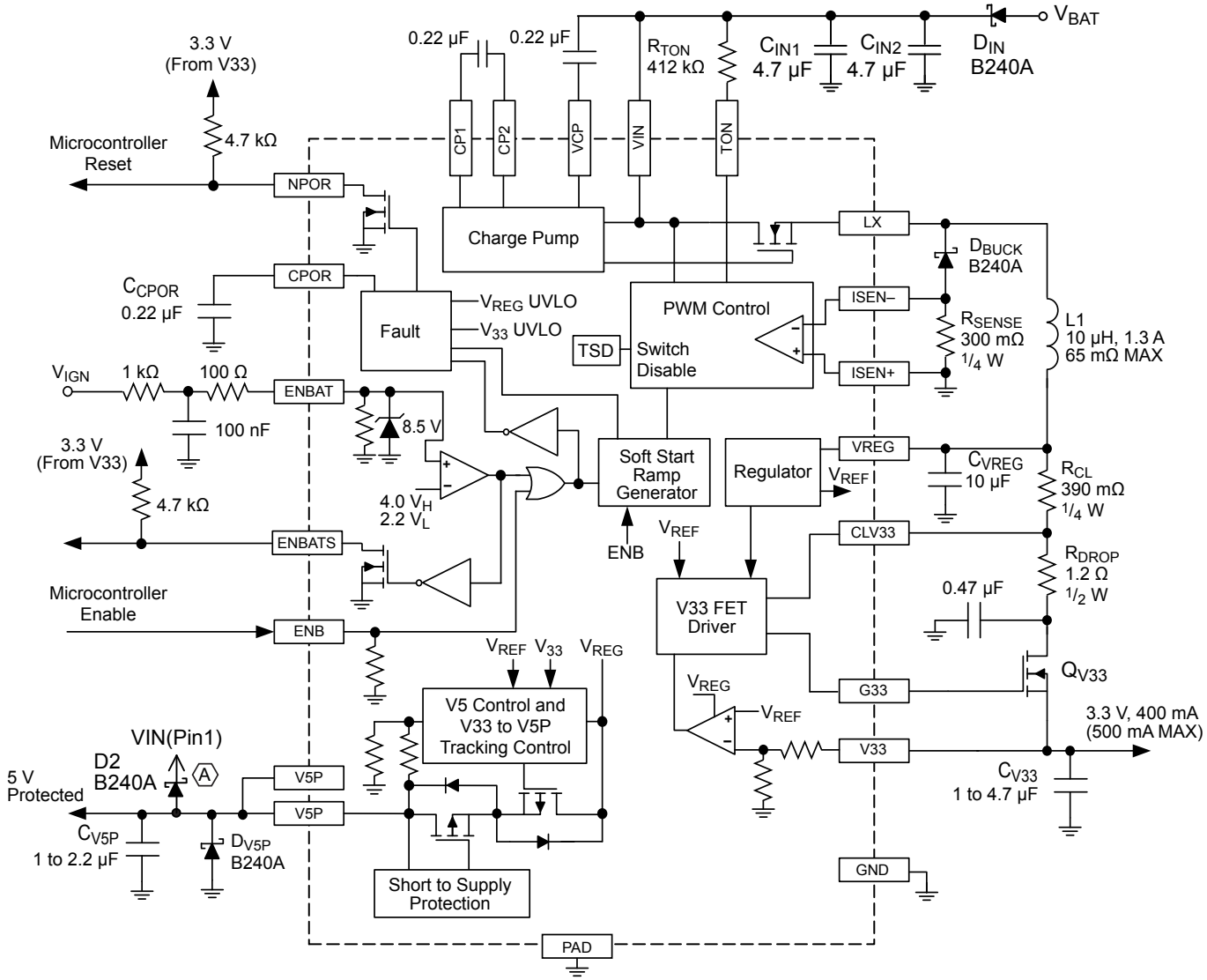
FUNCTIONAL BLOCK DIAGRAM



Ⓐ Protection diodes D1 and D2 are required when the V5P pin is driving a wiring harness (or excessively long PCB trace) where parasitic inductance will cause the voltage at the V5P to momentarily transition above VIN or below ground during a fault condition.

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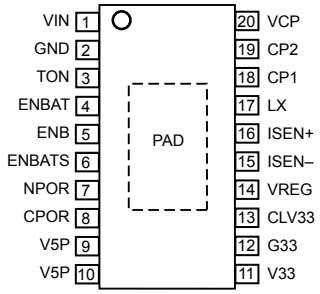
Pinout Diagram



Terminal List Table

Name	Number	Function
CLV33	13	3.3 V current sense and limit input
CP1	18	Charge pump capacitor terminal 1
CP2	19	Charge pump capacitor terminal 2
CPOR	8	NPOR delay programming pin
ENB	5	Logic enable input from the microcontroller
ENBAT	4	Ignition enable input from the key or switch via a 1 kΩ resistor
ENBATS	6	Open drain ignition status output
G33	12	Gate driver to the external MOSFET for 3.3 V regulation
GND	2	Ground terminal
ISEN–	15	Buck negative current sense pin, sense resistor and diode node
ISEN+	16	Buck positive current sense pin, sense resistor and ground node
LX	17	Buck regulator switching node
NPOR	7	Active low, open-drain fault indication output
PAD	–	Exposed pad for enhanced thermal dissipation
TON	3	Buck regulator on-time programming pin
V33	11	3.3 V regulator output
V5P	9,10	5 V tracking, protected regulator output
VCP	20	Charge pump reservoir capacitor terminal
VIN	1	Input voltage
VREG	14	Buck regulator DC output, and input to the 3.3 V external regulator

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ELECTRICAL CHARACTERISTICS: Valid at –40°C ≤ T_J ≤ 150°C, 5.5 V ≤ V_{IN} ≤ 36 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
Function Input Voltage	$V_{IN(f)}$	Device functional, parameters not guaranteed	5.5	–	46	V
Operating Input Voltage	$V_{IN(op)}$		5.5	13.5	36	V
Supply Quiescent Current [1]	I_Q	V_{IN} = 13.5 V, V_{IGN} > $V_{IGN(H)}$ or V_{ENB} > $V_{ENB(H)}$, no load on VREG	–	10	–	mA
	$I_{Q(SLEEP)}$	V_{IN} = 13.5 V, V_{IGN} < $V_{IGN(L)}$, V_{ENB} < $V_{ENB(L)}$, no load on VREG	–	–	10	µA
BUCK REGULATOR						
Switcher Output	V_{VREG}	ENB = high, $V_{INSW(L)}$ < V_{IN} < 27 V, 25 mA < I_{VREG} < 600 mA	5.25	5.45	5.60	V
		ENB = high, $V_{INSW(NOM)}$ < V_{IN} < 27 V, 25 mA < I_{VREG} < 750 mA	5.30	5.45	5.60	V
		ENB = high, 5.5 V < V_{IN} < 6.5 V, LX 100% on, 100 mA < I_{VREG} < 600 mA	5.15	–	6.46	V
Switcher Period [2]	$T_{SW(L)}$	$V_{INSW(L)}$ < V_{IN} < $V_{INSW(NOM)}$, R_{TON} = 412 kΩ	–	1.6	–	µs
	$T_{SW(NOM)}$	$V_{INSW(NOM)}$ < V_{IN} < $V_{INSW(H)}$, R_{TON} = 412 kΩ	–	450	–	ns
	$T_{SW(H)}$	$V_{INSW(H)}$ < V_{IN} < 36 V, R_{TON} = 412 kΩ	–	1.6	–	µs
Switcher On-Time	t_{ON}	V_{IN} = 7 V, R_{TON} = 412 kΩ	1070	1335	1600	ns
		V_{IN} = 13.5 V, R_{TON} = 412 kΩ	160	200	240	ns
		V_{IN} = 27 V, R_{TON} = 412 kΩ	80	118	135	ns
		V_{IN} = 35 V, R_{TON} = 412 kΩ	220	275	330	ns
Switcher Period V_{IN} Threshold	$V_{INSW(L)}$	V_{IN} falling, T_{SW} changes from $T_{SW(L)}$ to 100% duty cycle	5.9	6.2	6.5	V
	$V_{INSW(NOM)}$	V_{IN} falling, T_{SW} changes from $T_{SW(NOM)}$ to $T_{SW(L)}$	7.7	8.3	8.9	V
	$V_{INSW(H)}$	V_{IN} rising, T_{SW} changes from $T_{SW(NOM)}$ to $T_{SW(H)}$	28	31	34	V
Switcher Period V_{IN} Hysteresis	$V_{INSW(HYS)}$	$V_{INSW(L)}$ and $V_{INSW(NOM)}$ comparators, relative to the V_{IN} voltage that initially caused the switcher period to change	–	250	–	mV
		$V_{INSW(H)}$ comparator, relative to the V_{IN} voltage that initially caused the switcher period to change	–	700	–	mV
Buck Switch On-Resistance	$R_{DS(on)}$	T_J = 25°C, I_{DS} = 0.1 A	–	275	300	mΩ
		T_J = 150°C, I_{DS} = 0.1 A	–	400	470	mΩ
Minimum On-time	$t_{on(min)}$	V_{IN} = 13.5 V, R_{TON} = 49.9 kΩ	–	65	90	ns
Minimum Off-time	$t_{off(min)}$	V_{IN} = 13.5 V	85	110	140	ns
ISEN Voltage Threshold	V_{ISEN}	V_{ISEN+} – $V_{ISEN–}$	175	220	265	mV
VREG Valley Current Limit	$I_{LIM(VALLEY)}$	R_{SENSE} = 300 mΩ, V_{IN} > $V_{INSW(L)}$	–	733	–	mA
VREG Peak Current Limit	$I_{LIM(PEAK)}$		2.5	5.0	–	A

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ELECTRICAL CHARACTERISTICS (continued): Valid at –40°C ≤ T_J ≤ 150°C, 5.5 V ≤ V_{IN} ≤ 36 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
5 V LINEAR REGULATOR						
V5P Accuracy and Load Regulation	V_{V5P}	10 mA < I_{V5P} < 270 mA, V_{VREG} ≥ 5.25 V	4.9	5.0	5.1	V
V5P/V33 Tracking Ratio	$V5P_{track}$	V_{V5P} / V_{V33}	1.507	1.515	1.523	–
V5P/V33 Tracking Accuracy	$Err_{V5Ptrack}$	2.69 V < V_{V33} < 3.37 V, I_{V5P} = 75 mA, 5.5 V < V_{IN} < 27 V	−0.5	–	+0.5	%
LINEAR REGULATOR AND FET DRIVER						
V33 Accuracy	Err_{V33}	10 mA < I_{V33} < 500 mA	3.23	3.30	3.37	V
G33 Source Current [1]	$I_{G33(SRC)}$	V_{V33} = 3.0 V, V_{G33} = $V_{G33(MAX)}$ – 1 V	−175	−250	−400	µA
G33 Sink Current [1]	$I_{G33(SINK)}$	V_{V33} = 3.6 V, V_{G33} = 6 V	0.5	3	–	mA
G33 Maximum Voltage	$V_{G33(MAX)}$	V_{V33} = 3.0 V	9	–	15	V
G33 Minimum Voltage	$V_{G33(MIN)}$	V_{V33} = 3.6 V	–	0.7	1.0	V
G33 Output Impedance [2]	R_{OUT}		–	175	–	Ω
External FET Gate Capacitance [2]	C_{ISS}		250	–	5200	pF
CHARGE PUMP (VCP PIN)						
Output Voltage	ΔV_{VCP}	V_{VCP} – V_{IN}	4.1	6.6	–	V
Switching Frequency	$f_{SW(CP)}$		–	100	–	kHz
LOGIC ENABLE INPUT (ENB PIN)						
ENB Logic Input Threshold	$V_{ENB(H)}$	V_{ENB} rising	–	–	2.0	V
	$V_{ENB(L)}$	V_{ENB} falling	0.8	–	–	V
ENB Logic Input Current [1]	$I_{ENB(IN)}$	V_{ENB} = 3.3 V	–	–	100	µA
ENB Pull-Down Resistance	R_{ENB}		–	60	–	kΩ
IGNITION ENABLE INPUT (ENBAT AND ENBATS PINS)						
ENBAT and ENBATS Thresholds	$V_{IGN(H)}$	V_{IGN} rising via a 1 kΩ series resistance, measure V_{IGN} when I_Q occurs	–	–	4.0	V
	$V_{IGN(L)}$	V_{IGN} falling via a 1 kΩ series resistance, measure V_{IGN} when $I_{Q(SLEEP)}$ occurs	2.2	–	–	V
ENBAT Input Current [1]	$I_{ENBAT(IN)}$	V_{IGN} = 5.5 V via a 1 kΩ series resistance	–	50	100	µA
		V_{IGN} = 0.8 V via a 1 kΩ series resistance	0.5	–	5	µA
ENBAT Input Resistance	R_{ENBAT}		–	650	–	kΩ
IGNITION STATUS OUTPUT (ENBATS PIN)						
ENBATS Output Voltage	$V_{ENBATS(L)}$	I_{ENBATS} = 4 mA	–	–	400	mV
ENBATS Leakage Current [1]	I_{ENBATS}	V_{ENBATS} = 3.3 V	–	–	1	µA
ENBATS Turn-On Delay	t_{ENBATS}	Sleep mode to V_{ENBATS} = 3.3 V	–	11	–	ms

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ELECTRICAL CHARACTERISTICS (continued): Valid at –40°C ≤ T_J ≤ 150°C, 5.5 V ≤ V_{IN} ≤ 36 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NPOR PIN OUTPUT AND TIMING						
NPOR Power-Up Delay	t_{NPOR}	C_{POR} = 0.22 µF	–	20	–	ms
NPOR Output Voltage	$V_{NPOR(L)}$	ENB = high or ENBAT = high, $V_{VREG} < V_{REGNPOR(L)}$ or $V_{V33} < V_{33NPOR(L)}$, $I_{NPOR} \le 4$ mA	–	–	400	mV
		ENBAT = low, ENB transitioning to low, V_{VREG} = 5.45 V, $I_{NPOR} \le 0.3$ mA, 0.8 V < $V_{V33} < Err_{V33}$, 0°C ≤ T_J ≤ 150°C	–	350	800	mV
		ENBAT = low, ENB transitioning to low, V_{VREG} = 5.45 V, $I_{NPOR} \le 0.3$ mA, 1.0 V < $V_{V33} < Err_{V33}$, −40°C ≤ T_J ≤ 150°C	–	–	800	mV
NPOR Leakage Current [1]	$I_{NPOR(LEAK)}$	V_{NPOR} = 3.3 V	–	–	1	µA
CPOR PIN CHARACTERISTICS						
CPOR Charge Current [1]	$I_{CPOR(SRC)}$		–	−13	–	µA
CPOR Threshold	$V_{CPOR(H)}$	V_{CPOR} rising	1.0	1.2	1.4	V
VREG PIN SOFT-START TIMING						
Soft-Start	t_{SS}		–	10	–	ms
PROTECTION CIRCUITRY						
VREG Pin NPOR Thresholds	$V_{REGNPOR(H)}$	V_{VREG} rising, NPOR transitioning to high	4.80	5.00	5.20	V
	$V_{REGNPOR(L)}$	V_{VREG} falling, NPOR transitioning to low	4.75	4.94	5.14	V
VREG Pin NPOR Hysteresis	$V_{REG(HYS)}$		–	60	–	mV
V33 Regulator NPOR Thresholds	$V_{33NPOR(H)}$	V_{V33} rising, NPOR transitioning to high	2.80	2.95	3.10	V
	$V_{33NPOR(L)}$	V_{V33} falling, NPOR transitioning to low	2.69	2.83	2.97	V
V33 Regulator NPOR Hysteresis	$V_{33(HYS)}$		–	125	–	mV
V33 Regulator Overcurrent Threshold	V_{33OCP}	$V_{VREG} - V_{CLV33}$	175	200	245	mV
V33 Regulator Current Limit	$I_{V33ILIM}$	R_{CL} = 620 mΩ	–	323	–	mA
V33 Regulator Foldback Threshold	V_{33IFB}	V_{V33} = 0 V, $V_{VREG} - V_{CLV33}$	35	55	75	mV
V33 Regulator Foldback Current Limit	I_{V33IFB}	R_{CL} = 620 mΩ	–	89	–	mA
V5P Pin Current Limit [1]	$I_{V5PILIM}$	V_{V5P} = 5 V	−300	−405	–	mA
V5P Pin Foldback Current [1]	I_{V5PIFB}	V_{V5P} = 0 V	−70	−110	−150	mA
THERMAL PROTECTION (TSD)						
Thermal Shutdown Threshold	T_{JTSD}	T_J rising	155	170	–	°C
Thermal Shutdown Hysteresis	$T_{JTSD(HYS)}$		–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified pin.
[2] Determined by design and systems characterization. Not production tested.

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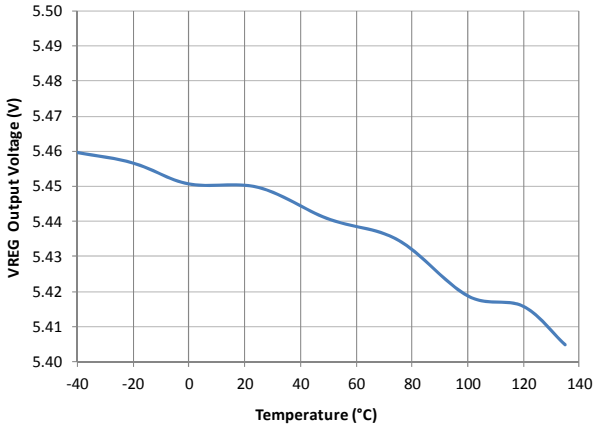
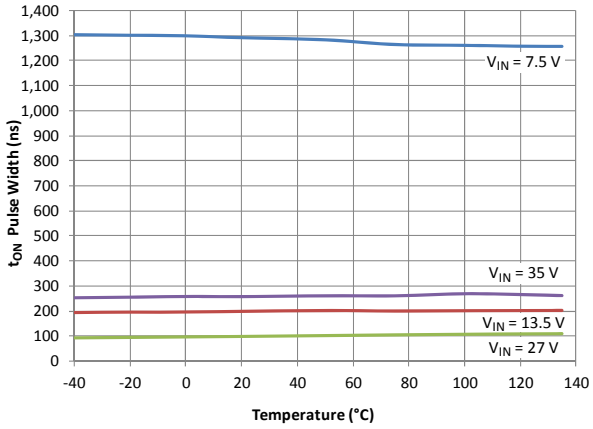
CHARACTERISTIC PERFORMANCE

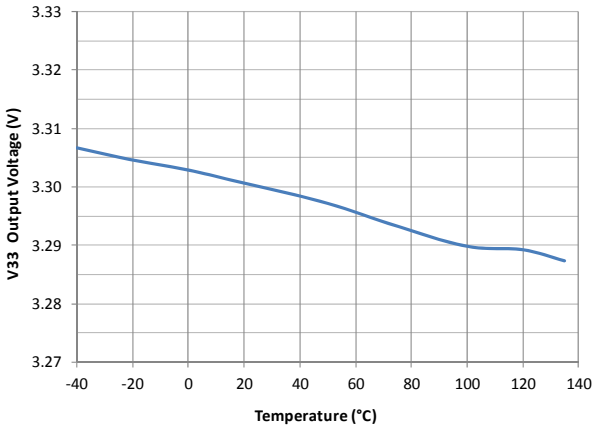
VREG Output versus Temperature



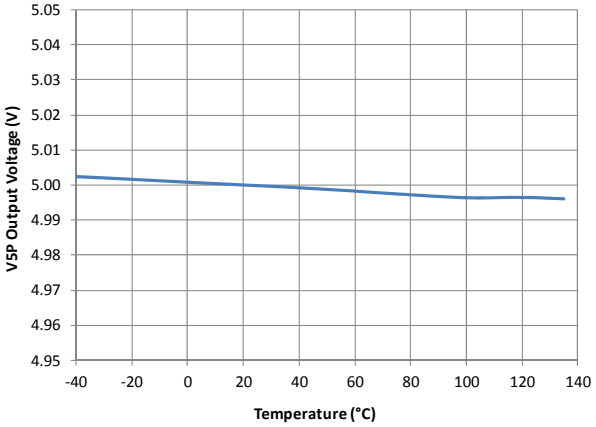
t_{ON} versus Temperature



V33 Output versus Temperature



V5P Output versus Temperature



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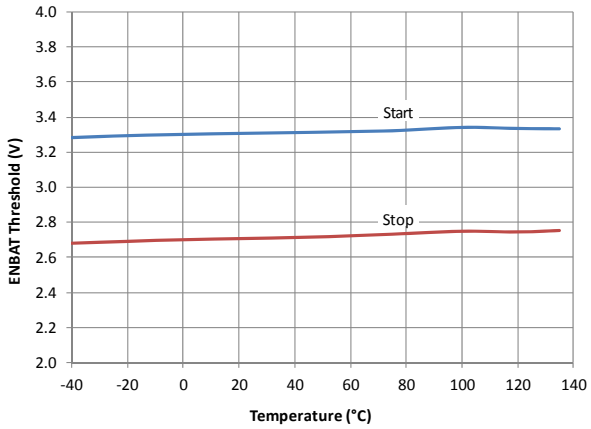
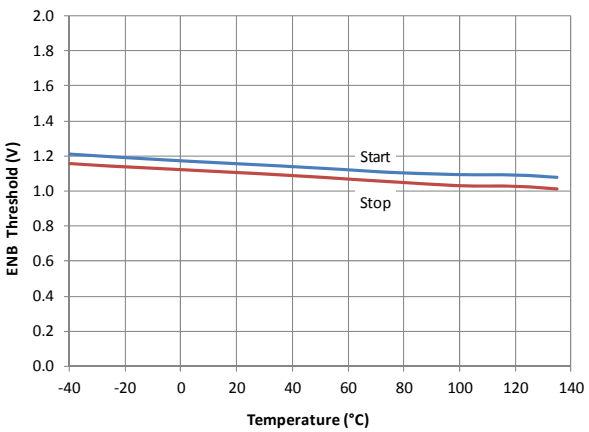
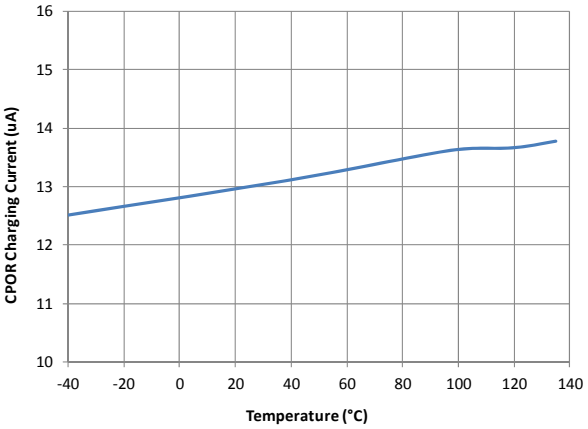
ENBAT Start / Stop Thresholds versus Temperature



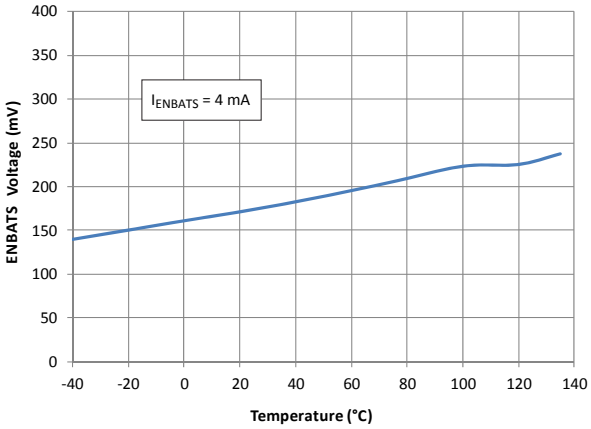
ENB Start / Stop Thresholds versus Temperature



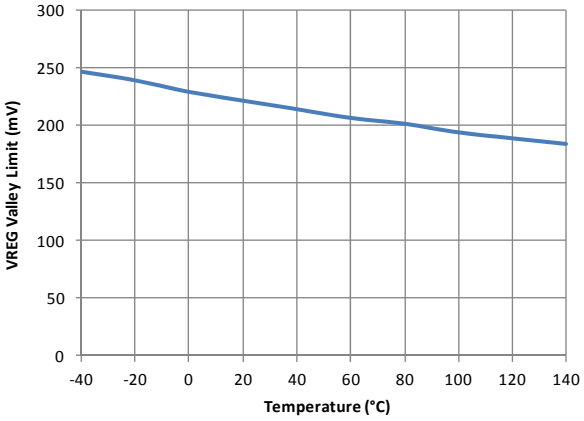
CPOR Charging Current versus Temperature



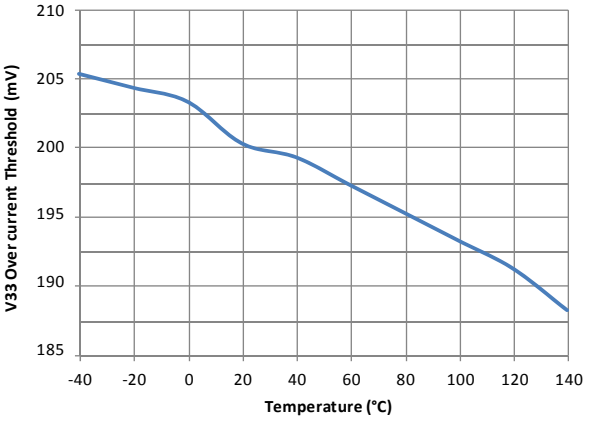
ENBATS (Low) Voltage versus Temperature



VREG Valley Current Limit versus Temperature



V33 Overcurrent Threshold versus Temperature



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FUNCTIONAL DESCRIPTION

Basic Operation

The A4406 contains a fixed on-time, buck switching pre-regulator with valley sensing current mode control, an integrated 5 V linear regulator, and an N-channel FET driver for a 3.3 V linear regulator. The constant on-time (COT) converter maintains a constant output frequency because the on-time is inversely proportional to the supply voltage. As the input voltage decreases the on-time is increased, which maintains a relatively constant period. Valley mode current control allows the converter to achieve very short on-times because current is measured during the off-time.

With very low input voltages the buck switch maintains a 100% duty cycle. This turns the buck switch on 100% of the time (no switching) and allows the regulator to operate in dropout mode.

The device is enabled via logic level ENB or high voltage ignition ENBAT input. When the device is enabled the converter starts up under the control of an internal soft-start routine. The two enable inputs are logically ORed together internally so either of the inputs can be used to enable the device.

Under light load conditions the switch enters pulse-skipping mode to ensure regulation is maintained. In order to maintain a wide input voltage range the switcher period is extended when the minimum on- or off-time is reached, or when the input supply is at either end of its range.

Overcurrent Protection

The A4406 features overcurrent protection on all regulators including the VREG pre-regulator. The buck switch current limit is determined by the selection of the sense resistor at the ISENx pins. Output current is also monitored on the 5VP and V33 linear regulators, and if shorted the outputs fold back. The external FET driver has a current limit tap that can be used with a sense resistor to trigger a current limit based on an external resistor and trip voltage.

Dropout Mode

The topology of a COT timer is ideal for systems that have high input voltages. Because current is measured during the off-time, very short on-times can be achieved. With low input voltages the switcher must maintain very short off-times. To prevent the switcher from reaching its minimum off-time, the switcher is designed to enter a 100% duty cycle mode. This causes the switcher to stop acting as a buck switch. The voltage at VREG then becomes the simply the supply voltage minus the drop across the buck switch and inductor. In this mode the maximum available current may be lower, depending on ambient temperature and supply voltage, while in dropout mode.

Soft-Start

An internal ramp generator and counter allow the output voltage to ramp-up. This limits the maximum demand on the external power supply by controlling the inrush current required to charge the external capacitor and any DC load at startup. Internally, the ramp is set to 10 ms nominal.

The following conditions are required to trigger a soft-start:

- ENBAT or ENB transition to high, and
- There is no thermal shutdown, and
- V33 voltage is below its UVLO threshold, and
- VREG voltage is below its UVLO threshold.

Buck Pulse Width (t_{ON})

A resistor from the TON input to VIN sets the on-time of the converter for a given input voltage. When the supply voltage is between 8.3 and 31 V, the switcher period remains constant based on the selected value of R_{TON}. At voltages lower than 6.5 V the switch is in dropout mode. For reasonable input voltage ranges the period of the converter is held constant resulting in a constant operating frequency over the input supply range. More information on how to choose R_{TON} can be found in the Application Information section.

The formula to calculate the value for the on-time resistor is:

$$t_{on} = (R_{TON} / V_{IN}) \times 6.36 \times 10^{-12} + 5 \times 10^{-9} \text{ (ns).} \quad (1)$$

ISEN+ and ISEN–

The sense inputs are used to sense the current in the buck, freewheeling diode during the off-time cycle. The value for R_{SENSE} is obtained by the formula:

$$R_{SENSE} = 220 \text{ (mV)} / I_{VALLEY} \quad , \quad (2)$$

where I_{VALLEY} is the lowest current measured through the inductor during the off-time cycle. It is recommended that the current sense resistor be sized so that, at peak output current, the voltage

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at the ISEN– pin does not exceed –0.75 V during PWM operation (that is, a transient condition). Because the diode current is measured when the inductor current is at the valley, the average output current is greater than the I_{VALLEY} value. The value for I_{VALLEY} should be:

$$I_{VALLEY} = I_{OUT(AVG)} - 0.5 \times I_{RIPPLE} + K \ , \quad (3)$$

where:

$I_{OUT(AVG)}$ is the average of the output currents of all the regulators,

I_{RIPPLE} is the inductor ripple current, and

K is a design margin allowing for component tolerances.

The peak current in the switch is simply:

$$I_{PEAK} = I_{VALLEY} + I_{RIPPLE} \ . \quad (4)$$

Information on how to calculate the ripple current is included in the Application Information section.

Switcher Overcurrent Protection

The converter utilizes pulse-by-pulse valley current limiting, which is activated when the current through the sense resistor (that is, the buck output current) is high enough to create 220 mV between the ISEN pins. During an overload condition, the switch is turned on for a period determined by the constant on-time circuitry. The switch off-time is extended until the current decays to the current limit value set by the selection of the sense resistor, at which point the switch is allowed to turn on again. Because no slope compensation is required in this control scheme, the current limit is maintained at a reasonably constant level across the input voltage range.

Figure 1 illustrates how the current is limited during an overload condition. The current decay (period with switch off) is proportional to the output voltage. As the overload is increased, the output voltage tends to decrease and the switching period increases.

LX Short Circuit Protection

If the LX node is shorted to ground there will be a relatively high peak current in the buck MOSFET within a very short time. The A4406 protects itself by detecting the unusually high current, turning off the buck MOSFET, and latching itself off. To avoid false tripping, the current required to activate the peak current protection ($I_{LIM(PEAK)}$, nominally 5 A) is set well above the normal range of currents. When the peak current limit is activated the A4406 is latched off until either V_{IN} is cycled below its UVLO threshold or the A4406 is disabled (both ENBAT and ENB must be brought low) and re-enabled. NPOR is not directly activated (pulled low) by the peak current protection circuitry. However, NPOR will certainly be in the correct state depending on VREG and V33.

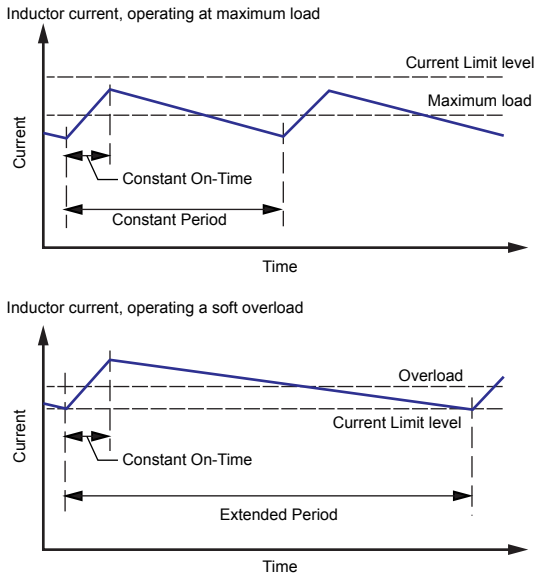

Figure 1. Current limiting during overload conditions

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Missing Asynchronous Diode Protection

In most high voltage asynchronous buck regulators, if the asynchronous diode is missing or damaged the LX pin will transition to a very high negative voltage when the upper MOSFET turns off, resulting in damage to the regulator. The A4406 includes protection circuitry to detect when the asynchronous diode is missing or damaged. If the LX pin becomes more negative than 1.2 V at 25°C for more than 157 ns, the A4406 will latch itself in the off state to prevent damage. After a missing diode fault occurs, the latch must be reset by either cycling VIN or ENBAT or ENB. See figure 2 for the missing diode voltage threshold and time filtering versus temperature.

Thermal Shutdown

If the A4406 junction temperature becomes too high, a thermal shutdown circuit disables the VREG output, thus protecting the A4406 from damage. When a thermal shutdown occurs, the buck regulator stops switching and the VREG voltage will decay. When V_{VREG} crosses its UVLO threshold, the NPOR signal is pulled low. Thermal shutdown is not a latched condition so, when the junction temperature cools to an acceptable level, the A4406 will automatically restart.

Power-On Reset (NPOR)

The NPOR output is an open drain pin that can be used to signal a reset event to a DSP or microcontroller. The NPOR function actively monitors ENBAT, ENB, V33, and VREG. During power-up, NPOR is held low for a programmable amount of time, t_{NPOR}, after both VREG and V33 transition above their upper UVLO thresholds. The rising edge delay allows time for the regulators to be within specification when the DSP or microcontroller begins processing. The amount of the rising edge delay is determined by the value of the external capacitor from the CPOR pin to ground.

The rising delay can be calculated from the following formula:

$$t_{NPOR} = 92.3 \times 10^3 \times C_{CPOR} \quad \text{(seconds)}. \qquad (5)$$

Any of the following conditions will force NPOR to transition to low immediately (within a few microseconds):

- V33 voltage falls below its UVLO threshold, or
- VREG voltage falls below its UVLO threshold, or
- ENBAT and ENB are both low, or
- Charge pump voltage is too low. or
- Internal IC regulation (V_{RAIL}) is too low.

If thermal shutdown occurs, PWM switching will terminate, V_{VREG} and/or V_{V33} will decay below the UVLO threshold, and NPOR will transition to low. Thus, a thermal shutdown event indirectly causes NPOR to transition to low.

When the A4406 is disabled (either both ENB and ENBAT are low, or V_{IN} is removed) the NPOR output is held low until the voltage from the 3.3 V regulator (V_{V33}) falls below 1.0 V. This assumes maximum initial current (4 mA) in the NPOR open drain DMOS. The NPOR voltages would be somewhat lower for lower values of I_{NPOR}. See figure 3.

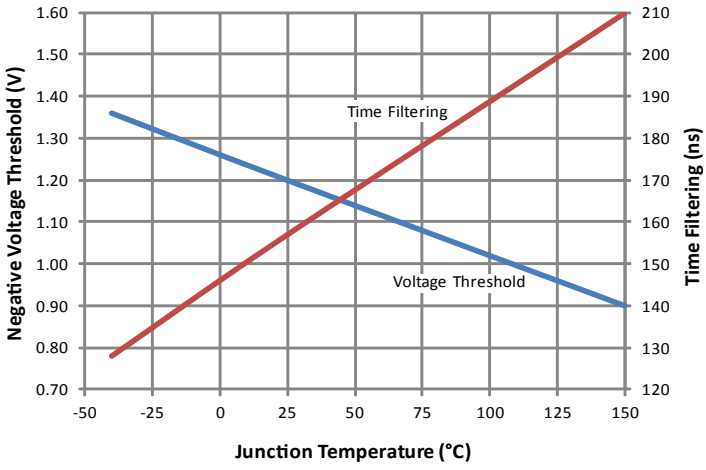

Figure 2. Missing diode protection versus device junction temperature

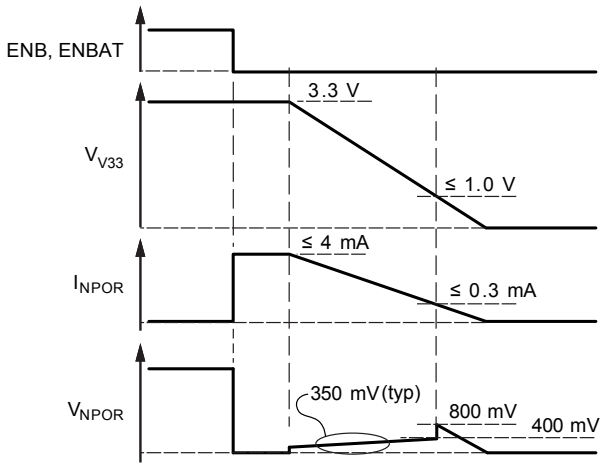

Figure 3. NPOR and V33 characteristics when the A4406 is disabled

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V5P Tracking Regulator

The 5VP linear tracking regulator is provided to supply remote circuitry such as off-board sensors. The V5P pin is monitored and if a short to ground or a short to battery occurs the V5P output is disabled and/or disconnected and the other outputs (VREG and V33) remain active until the short is removed. The regulator can deliver 375 mA (typ), 270 mA (min). When a direct short is applied to this regulator the output the current folds back to 0 V at approximately 112 mA (typ) (figure 4).

The V5P regulator is designed to track the V33 output during power-up and when the device is completing a soft-start ramp. The V5P regulator tracks the 3.3 V output to within ±0.5% under normal steady state operating conditions. If the V33 regulator is decreasing, the V5P regulator accurately tracks the V33 output down to the point at which a V33 undervoltage fault (2.825 V nominally: 2.95 V – 125 mV) results in the NPOR output going active.

The figures 5 and 6 show A4406 operation when the V5P pin is shorted to ground and VIN (battery). In both cases, the V5P output is disabled and/or disconnected while the other outputs (VREG and V33) remain active.

3.3 V Linear Regulator

An additional 3.3V linear regulator can be implemented using an external MOSFET. In the event the 3.3V regulator output is shorted to ground, the A4406 protects the external MOSFET by folding back when the programmed current limit, I_{CL}, is exceeded. The current limit is determined by the voltage devel-

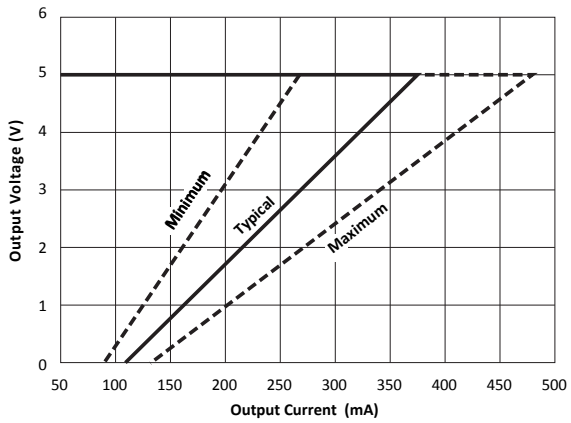

Figure 4. Foldback current limit of the 5VP regulator

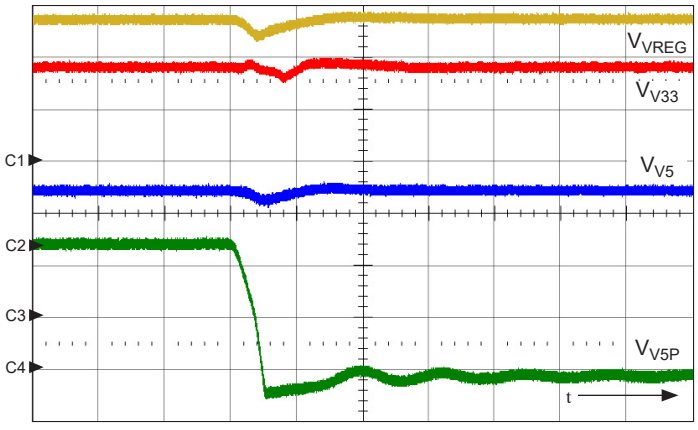

Figure 5. V5P is shorted to ground in 5 µs (D_{V5P} is populated); shows V_{VREG} (ch1, 2 V/div.), V_{V33} (ch2, 1 V/div.), V_{V5} (ch3, 2 V/div.), V_{V5P} (ch4, 2 V/div.), t = 10 µs/div.

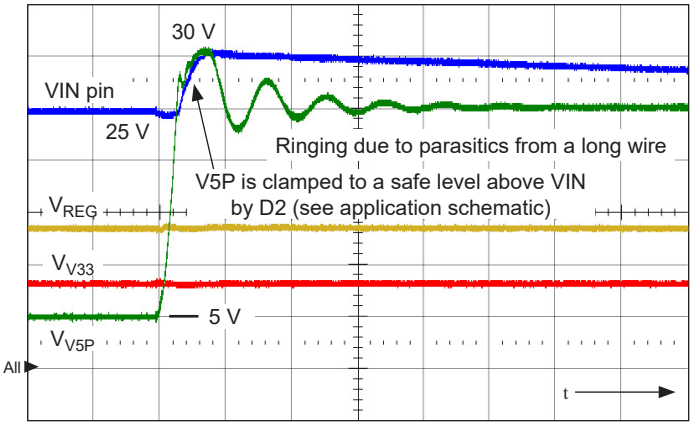

Figure 6. V5P is shorted to a 25 V battery; shows V_{VREG} (ch1, 2 V/div.), V_{V33} (ch2, 2 V/div.), VIN pin (ch3, 5 V/div.), V_{V5P} (ch4, 5 V/div.), t = 10 µs/div.

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oped across the external sense resistor, R_{CL}, shown in the Typical Application Circuit schematic. The 3.3V current limit can be calculated using the following formula:

$$I_{CL} = V_{CLV33} / R_{CL} \ , \quad (6)$$

where V_{CLV33} is as documented in the Electrical Characteristics table, nominally 200 mV. Typically R_{CL} will be a fairly low value so it will not dissipate significant power, $^1/_4$ W should be adequate, but the tolerance should be 1% or less.

When I_{CL} is exceeded, the maximum load current through the external MOSFET is typically folded back to 48% of I_{CL} as shown in figure 7.

Some applications require 5.0 V instead of 3.3 V. The external LDO controller will produce 5.0 V if a resistor divider is inserted between the controller output (that is, the source of the external MOSFET) and the V33 pin, as shown on page 1 of this datasheet. In this case, the 1.2 Ω/0.5 W power dropping resistor in series with the drain of the external MOSFET must be removed from the design.

Allegro recommends using resistors with ≤0.5% tolerance for two reasons: (1) the 5.0 V output will have the best accuracy, and (2) to maintain a low tracking error between the V5P and the 5.0 V output. A comparison of two sets of resistor values at 0.1% and 0.5% tolerance are shown in the following table.

R1 and R2 Values and Tolerances	5V Output Range (V)			V5P/V5 Tracking Accuracy (%)
	Min.	Typ.	Max.	
100 Ω and 196 Ω ±0.1%	4.887	4.999	5.112	±0.6
100 Ω and 196 Ω ±0.5%	4.874	4.999	5.125	±0.9
1.02 kΩ and 2.18 kΩ ±0.1%	4.867	5.002	5.141	–1.1, +1.2
1.02 kΩ and 2.18 kΩ ±0.5%	4.855	5.002	5.154	–1.4, +1.5

Charge Pump

The charge pump is used to generate a supply above V_{IN}. A 0.22 µF ceramic monolithic capacitor should be connected between VCP and VIN to act as a reservoir to run the DMOS switch. The VCP voltage is internally monitored to ensure that the charge pump is disabled in the case of a fault condition. A 0.22 µF ceramic monolithic capacitor should be connected between CP1 and CP2.

ENBAT

This is a level-triggered enable input, use for enabling the device based on a high voltage ignition or battery switch (via a 1 kΩ resistor). The ENBAT comparator thresholds are $V_{IGN(L)}$ = 2.2 V(min)and $V_{IGN(H)}$ = 4.0 V (max). ENBAT is used only as a momentary switch to enable or wake up the A4406. After ENBAT is removed, ENB must be high to keep the A4406 enabled. The ENB and ENBAT signals are logically ORed together internally so either one may wake up the A4406 and both must be low to disable the A4406. Only one of the two inputs must be pulled high in order to enable the part. If there is no requirement for an ignition switch, then ENBAT can be pulled low, which makes ENB a single reset control.

If an external resistor and capacitor are used to form a low-pass filter to the ENBAT pin, then a 100 Ω resistor must be used to prevent the external capacitor from discharging into and damaging the ENBAT pin. See the Typical Application Circuit schematic for connection of these 3 components.

ENBATS

When a logic high is sensed on the ENBAT input, the ENBATS output will go high, signaling to the user that the ignition input is high. When a logic low is sensed on the ENBAT input, then ENBATS will also transition to low. The ENBATS input logic levels are identical to the ENBAT input logic levels.

ENB

This pin can be used as an enable input from either a DSP or from a microcontroller. This input has an internal pull-down resistor so it may be left unconnected if not used.

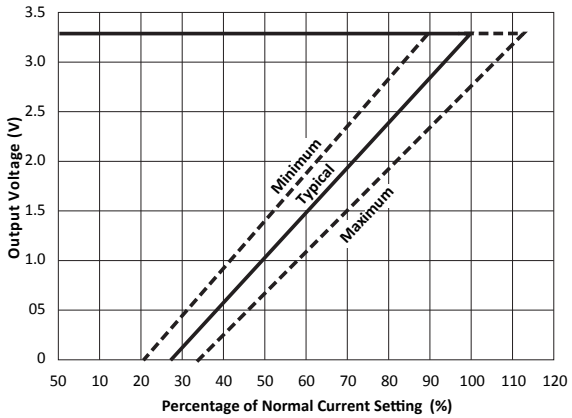

Figure 7. Foldback current limit of the V33 regulator

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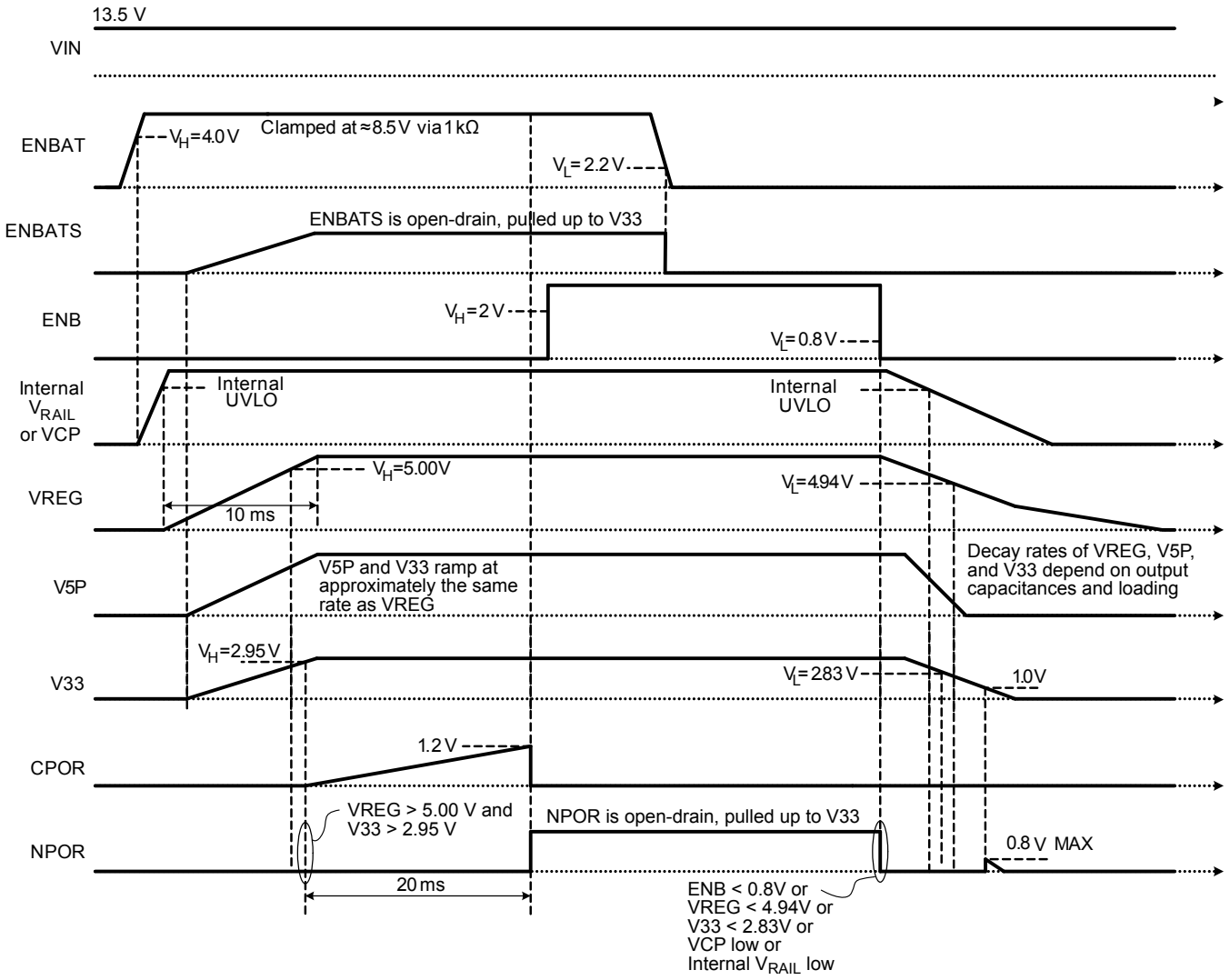
TIMING DIAGRAMS



Typical power-up and power-down by ENBAT and ENB with V_{IN} = 13.5 V; ENBATS is assumed to be connected to V33 via a pull-up resistor

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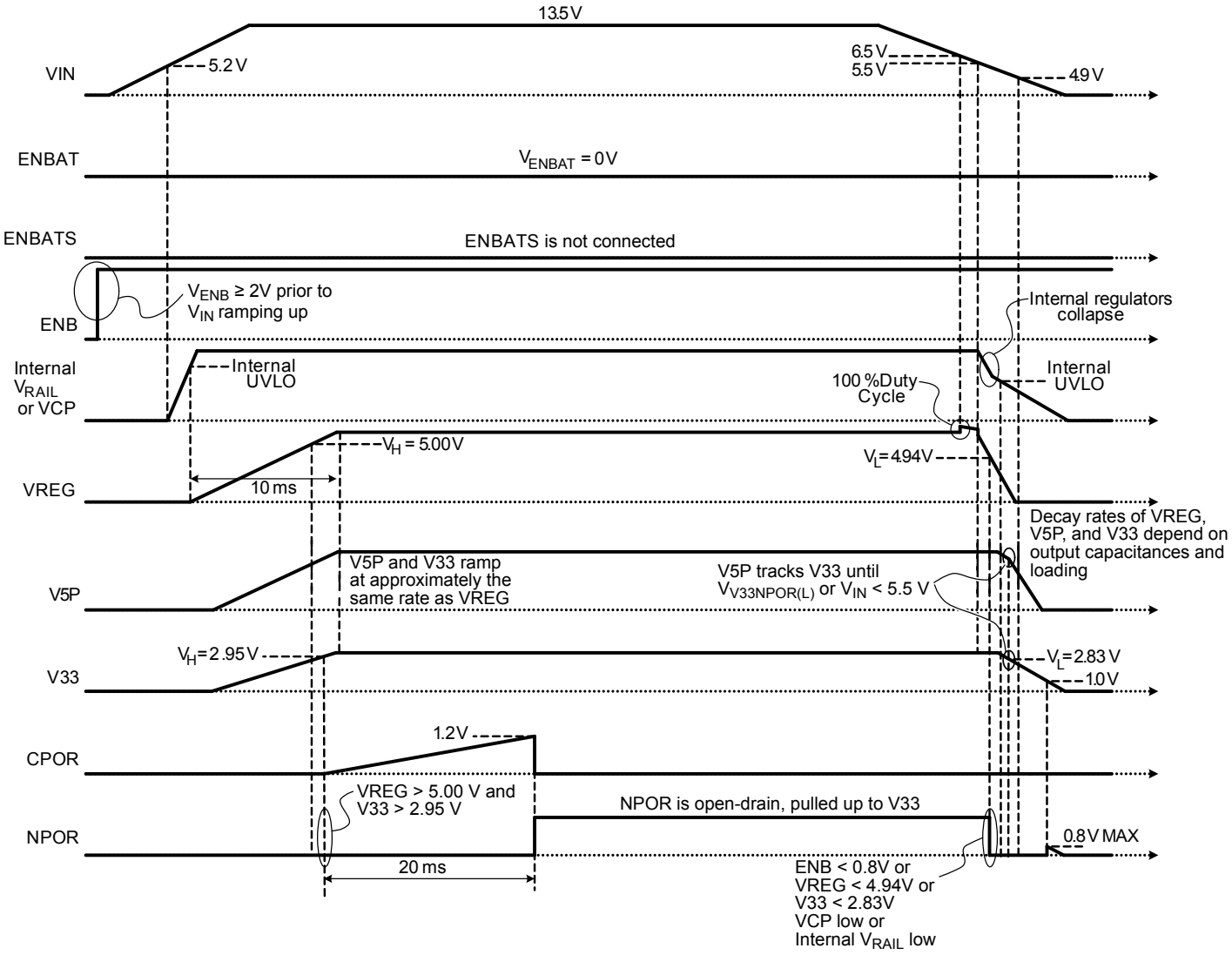

Typical power-up and power-down via VIN with ENB always logic high; ENBAT and ENBATS are not used

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APPLICATION INFORMATION

Switcher On-Time and Switching Frequency

In order for the switcher to maintain regulation, the energy that is transferred to the inductor during the on-time must be transferred to the capacitor during the off-time. Because of this relationship, the load current and IR drops, as well as input and output voltages, affect the on-time of the converter. The formula that governs switcher on-time is shown below:

$$t_{ON} = \frac{T_{SW} \times \{V_{VREG} + [(R_L + R_{SENSE}) \times I_{PEAK}] + V_f\}}{V_{IN} - R_{DS(on)} \times I_{PEAK} + V_f} \quad . \quad (7)$$

where V_f is the forward voltage on the diode D_{BUCK} in the Typical Application Circuit schematic.

The effects of the voltage drop on the inductor and trace resistance will affect the switching frequency. However, the frequency variation due to these factors is small and is covered in the variation of the switcher period, which is ±25% of the target. Removing these current dependent terms simplifies the formula:

$$t_{ON} = \frac{(1/f_{SW}) \times (V_{VREG} + R_{SENSE} \times I_{PEAK}) + V_f}{V_{IN} - R_{DS(on)} \times I_{PEAK} + V_f} \quad . \quad (8)$$

Be sure to use the worst-case sense voltage and forward voltage of the diode D_{BUCK}, including any effects due to temperature. For an example: assume a 1 A converter with a supply voltage of 13.5 V. The output voltage is 5.45 V, V_f is 0.45 V, $R_{SENSE} \times I_{PEAK}$ is 0.20 V, $R_{DS(ON)} \times I_{PEAK}$ is 0.15 V, and the required frequency is 2.2 MHz. Substituting into equation 8, we can solve for t_{ON}:

$$t_{ON} = 1 / 2.2\ (\text{MHz}) \times [(5.45+0.20+0.45) / (13.5 - 0.15 + 0.45)]$$
$$= 201\ (\text{ns}) \ .$$

The formulas above describe how t_{ON} changes based on input and load conditions. Because load changes are minimal and the output voltage is fixed, the only factor that will affect the on-time is the input voltage. The converter is able to maintain a constant period over a varying supply voltage because the on-time changes based on the input voltage. The current into the TON terminal is derived from a resistor tied to VIN, which sets the on-time proportional to the supply voltage. Selecting the resistor value based on the t_{ON} calculated above is done using the following formula:

$$R_{TON} = [V_{IN} \times (t_{ON} - 5\ (\text{ns}))] / 6.36 \times 10^{-12} \quad . \quad (9)$$

After the resistor is selected and a suitable t_{ON} is found, it must be demonstrated that t_{ON} does not, under worst-case conditions, exceed the minimum on-time or minimum off-time of the converter. The minimum on-time occurs at maximum input voltage and minimum load. The maximum off-time occurs at minimum supply voltage and maximum load. For supply voltages below 8.3 V and above 6.5 V, refer to the Low Voltage Operation section.

Low Voltage Operation

The converter can run at very low input voltages; with a 5.25 V output the minimum input supply can be as low as 5.5 V. When operating at high frequencies the on-time of the converter must be very short because the available period is short. At high input voltages the converter should not violate the minimum on-time, $t_{ON}(\text{min})$, while at low input voltages the converter should not violate the minimum off-time, $t_{OFF}(\text{min})$. Rather than limit the supply voltage range, the converter solves this problem by automatically increasing the period. With the period extended the converter will not violate the minimum on-time or off-time specifications. If the input voltage is between 8.3 and 31 V, the converter maintains a constant period. When calculating worst case on-times and off-times, make sure to use the highest switching frequency if the supply voltage is in that range.

When operating at voltages below 8.3 V, additional care must be taken when selecting the inductor and diode. At low voltages the maximum current may be limited due to the IR drops in the current path. When selecting external components for low voltage operation, the IR drops must be considered for determining on-time, so the complete equation (formula 8) should be used to make sure the converter does not violate the timing specification.

Inductor Selection

Choosing the right inductor is critical to the correct operation of the switcher. The converter is capable of running at frequencies above 2 MHz, this makes it possible to use small inductor values, which reduces cost and board area.

The inductor value is what determines the ripple current. It is important to size the inductor so that under worst-case conditions I_{TRIP} equals I_{AVG}, minus half of the ripple current, plus a reasonable margin. If the ripple current is too large, the converter will activate the current limit function. Typically peak-to-peak

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ripple current should be limited to a range of 20% to 25% of the maximum average load current.

Worst-case ripple current occurs at maximum supply voltage. After calculating the duty cycle for this condition, the ripple current can be calculated:

$$D = \frac{V_{VREG} + (R_{SENSE} \times I_{PEAK}) + V_f}{V_{IN}(max) - R_{DS(on)} \times I_{PEAK} + V_f} \quad . \qquad (10)$$

Using the duty cycle, a ripple current can be calculated using the formula below:

$$L = \frac{V_{IN} - V_{VREG}}{I_{RIPPLE}} \times D \times \frac{1}{f_{SW}(min)} \quad , \qquad (11)$$

where I_{RIPPLE} is 25% of the maximum load current, and f_{SW}(min) is the minimum switching frequency, nominal frequency minus 25%. For the example used above, a 1 A converter with a supply voltage of 13.5 V was the design objective. The supply voltage can vary by ±10%. The output voltage is 5.45 V, V_f is 0.5 V, V_{SENSE} is 0.20 V and the required frequency is 2.2 MHz. The duty cycle is calculated to be 36.45%. The worst-case frequency is 1.76 MHz, 2.2 MHz minus 20%. Using these numbers in formula 11 shows that the minimum inductance for this converter is 9.6 µH.

Output Capacitor

The converter is designed to operate with a low value ceramic output capacitor on VREG (C_{VREG}). When choosing a ceramic capacitor make sure the rated voltage is at least 3 times the maximum output voltage of the converter. This is because the capacitance of a ceramic decreases as it operates closer to the capacitor rated voltage. It is recommended that the VREG output be decoupled with a 10 µF X7R ceramic capacitor. Greater capacitance may be required on the output if load surges dramatically influence the output voltage.

Output ripple is determined by the output capacitance and the effects of ESR and ESL can be ignored assuming recommended layout techniques are followed. The output voltage ripple is approximated by:

$$V_{RIPPLE} = I_{RIPPLE} / (8 \times f_{SW} \times C_{VREG}) \qquad (12)$$

Input Capacitor

The value of the input capacitance affects the amount of current ripple on the input. This current ripple is usually the source of supply-side EMI. The amount of interference will depend on the impedance from the input capacitor and the bulk capacitance located on the supply bus. Placing a 0.1 µF ceramic capacitor very close to the input supply pin will help reduce EMI effects. The small capacitor will help reduce high frequency transient currents on the supply line. If further filtering is needed it is recommended that two ceramic capacitors be used in parallel to further reduce emissions.

Rectification Diode

The diode conducts the current during the off cycle. A Schottky diode is required to minimize the forward drop and switching losses. In order to size the diode correctly it is necessary to find the average diode conduction current using the formula below :

$$I_{diode(avg)} = I_{load} \times (1 - D(min)) \qquad (13)$$

where D(min) is the minimum duty cycle, defined as:

$$D(min) = (V_{VREG} + V_f) / (V_{IN} + V_f) \qquad (14)$$

where V_{IN} is the maximum input voltage and V_f is the maximum forward voltage of the diode.

The average power dissipation in the diode is:

$$P_{Ddiode(avg)} = I_{avg} \times D(min) \times V_f \qquad (15)$$

The power dissipation in the sense resistor must also be considered using I^2R and the minimum duty cycle.

External MOSFET Selection

To choose an external MOSFET for the 3.3 V linear regulator consider the maximum of: drain-to-source voltage (V_{DS}), continuous drain current (I_D), threshold voltage (V_{GSTH}), on-resistance ($R_{DS(on)}$), and thermal resistance ($R_{\theta JC}$).

The buck switcher pre-regulates the voltage to the external MOSFET, so even under worst case conditions, the MOSFET will not have to support more than 7 V from drain to source. Also, the 3.3 V current limit will usually be set from 200 to 500 mA using the external current setting resistor, R_{CL}. Numerous MOSFETs are available with V_{DS} ratings of at least 20 V that can support much more than 1 A. These two goals should not be difficult to achieve.

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The A4406 gate drive circuitry is guaranteed to pull the G33 voltage down to 1 V, maximum. Therefore, Allegro recommends using a MOSFET with a V_{GS} threshold (V_{GSTH}) higher than 1 V. Do not use a MOSFET that will conduct significant current when V_{GS} is at 1 V and the system is at the highest expected ambient temperature.

One of the more critical specifications is the MOSFET on-resistance, $R_{DS(on)}$. If the on-resistance is too high, then the 3.3 V regulator will not be able to maintain 3.3 V at the maximum required load current, $I_{LIM(V33)}$. Calculate the typical $R_{DS(on)}$ (at 25°C) using the following formula:

$$R_{DS(on)25°C} < 0.6 \times 1.56\ (V) / (I_{LIM(V33)} - R_{DROP}) \quad (16)$$

where $I_{LIM(V33)}$ is the maximum required 3.3 V output current, and R_{DROP} is the value of the resistor connected from the CLV33 pin to the drain of the MOSFET.

The multiplier of 0.6 in the following formula allows a 66% increase in $R_{DS(on)}$ when the MOSFET is very hot:

$$R_{DS(on)25°C} < 0.6 \times \left(\frac{1.56\ (V)}{I_{LIM(V33)}} - R_{DROP} \right) . \quad (17)$$

where $I_{LIM(V33)}$ is the maximum required 3.3 V output current.

The necessity and value of R_{DROP} is closely related to the thermal resistance ($R_{\theta JC}$) of the MOSFET. For a medium size MOSFET (such as an SOT-223) including R_{DROP} in the PCB layout is highly recommended. For a large size MOSFET with a very low thermal resistance (such as a DPAK) R_{DROP} is probably not necessary.

MOSFET thermal resistance is a function of die size, package size, and cost. So, choosing R_{DROP} and $R_{\theta JC}$ together should result in optimal performance, minimal component sizes, and lowest system cost. Determining the value and power dissipated by the series dropping resistor and MOSFET thermal resistance are addressed in detail in the 3.3 V Dropping Resistor section.

3.3 V Dropping Resistor (R_{DROP})

In the Typical Application Circuit schematic, there are two resistors, R_{CL} and R_{DROP}, from the output of the buck regulator to the drain of the external MOSFET. R_{CL} must always be present because it sets the 3.3 V regulator current limit threshold. However, R_{DROP}, if used, prevents the external MOSFET from dissipating too much power during certain conditions. In particular, when the battery voltage is extremely low ($V_{BAT} \leq 6.5$ V) and the buck regulator transitions to dropout mode (100% duty cycle) then V_{VREG} will be approximately 1 V higher than normal. In this situation, without R_{DROP}, the MOSFET could dissipate too much power.

The value of R_{DROP} depends on the maximum PCB temperature, the maximum current load on the 3.3 V regulator, $I_{LIM(V33)}$, the maximum allowable junction temperature of the MOSFET, and the thermal resistance of the MOSFET. As the thermal resistance of the MOSFET decreases, the required value of R_{DROP} will also decrease. If the MOSFET is relatively large and has a very low thermal resistance, then R_{DROP} is not required (0 Ω).

Figure 8 shows recommended values of R_{DROP} versus MOSFET thermal resistance at various 3.3 V regulator maximum current settings ($I_{LIM(V33)}$). This graph assumes a PCB temperature of 135°C, a maximum MOSFET junction temperature of 145°C, V_{BAT} of 6.5 V, and 3.23 V from the linear regulator. This graph takes into account the voltage drop across the 3.3 V current limit resistor, R_{CL}.

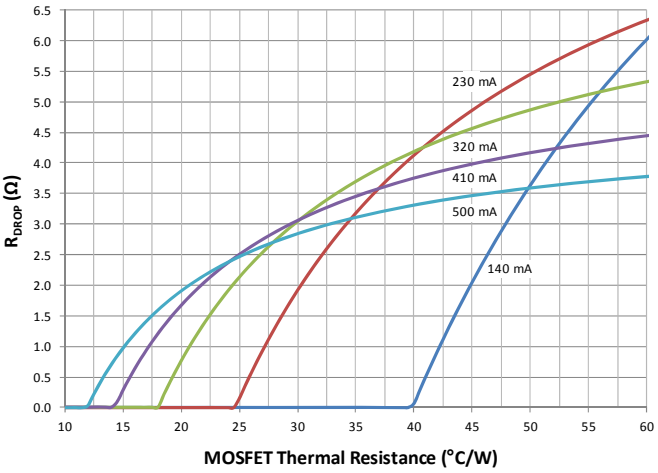

Figure 8. Value of R_{DROP} versus MOSFET thermal resistance at various V33 regulator maximum current settings, $I_{LIM(V33)}$

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After a value for R_{DROP} is determined, the designer should calculate its maximum power dissipation ($I^2 \times R$) and select an appropriate component, allowing adequate design margin. Assuming the R_{DROP} value was chosen referencing figure 8, then figure 9 can be used to determine the power dissipated by R_{DROP} versus MOSFET thermal resistance at various 3.3V regulator current settings. The exact value of R_{DROP} is not critical, so a component with 1% or 5% tolerance could be used.

PCB Layout

The board layout will have a large impact on the performance of the device. It is important to isolate high current ground returns to minimize ground bounce that could produce reference errors in the device. The method used to isolate power ground from noise sensitive circuitry is to use a star ground. This approach ensures that the high current components such as the input capacitor, output capacitor, and diode have very low impedance paths to each other. Figure 10 illustrates the technique.

The ground connections from each of the components should be very close to each other and be connected on the same surface as the components. Internal ground planes should not be used for the star ground connection, because vias add impedance to the current path.

In order to further reduce noise effects on the PCB, noise sensitive traces should not be connected to internal ground planes. The feedback network from the switcher output should have an independent ground trace that goes directly to the exposed pad underneath the device. The exposed pad should be connected to internal ground plans and any exposed copper used for heat dissipation. If the ground connections from the device are also connected directly to the exposed pad, the ground reference from the feedback network will be less susceptible to noise injection or ground bounce.

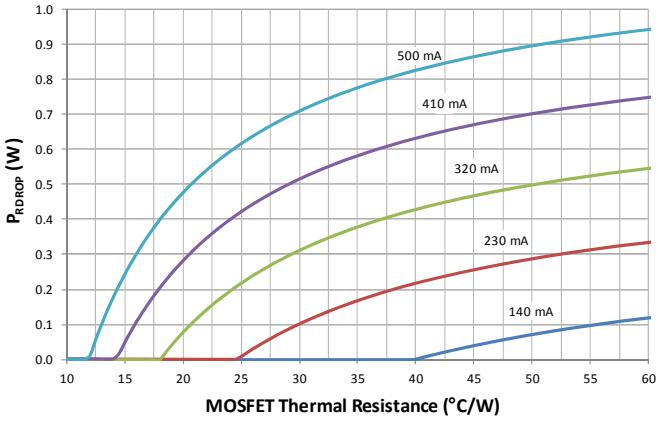

Figure 9. R_{DROP} Dissipation versus MOSFET thermal resistance at various V33 regulator maximum current settings, $I_{V33ILIM}$

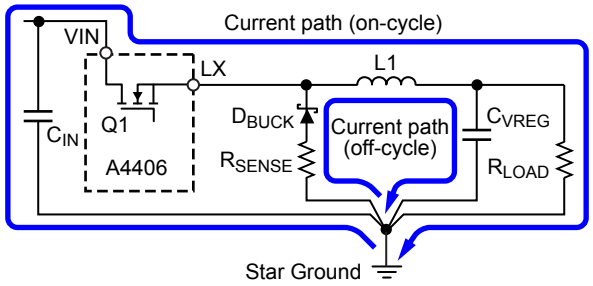

Figure 10. Illustration of star ground connection

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To reduce radiated emissions from the high frequency switching nodes, it is important to have an internal ground plane directly under the LX node. The plane should not be broken directly under the node because the lowest impedance path back to the star ground would then be directly under the signal trace. If another trace does break the return path, the energy will have to find another path, which is through radiated emissions.

For accurate current sensing, the current sense pins, ISEN+ and ISEN–, and the internal differential amplifier comprise a differential signal receiver, and a balanced pair of traces should be routed from the pins of the buck current sense resistor, R_{SENSE}, as shown in figure 11 (upper panel). The ISEN+ pin and the sense resistor ground should not be separated by simply using local via connections to the ground plane (figure 16 lower panel). Incorrect routing of the ISEN+ pin would likely add an offset error to the buck current sense signal.

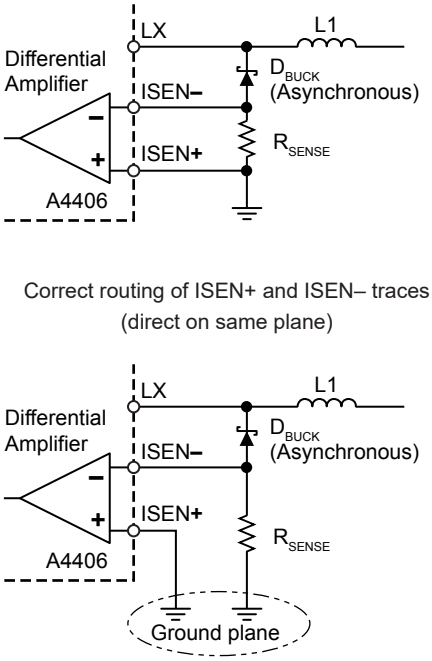

Figure 11. Comparison of routing paths for the traces between the A4406 ISEN+ and ISEN– traces and the sense resistor, R_{SENSE}

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Application Circuit Performance

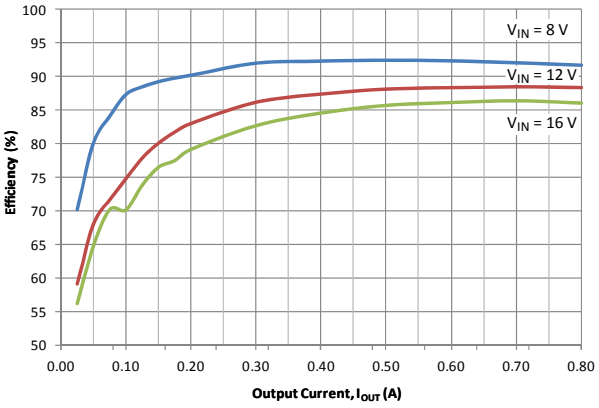
(Refer to Typical Application Circuit diagram.)

Bill of Materials for Critical Components

This design is capable of full load, 135°C ambient, and 5.5 V_{BAT} indefinitely with an adequate thermal solution

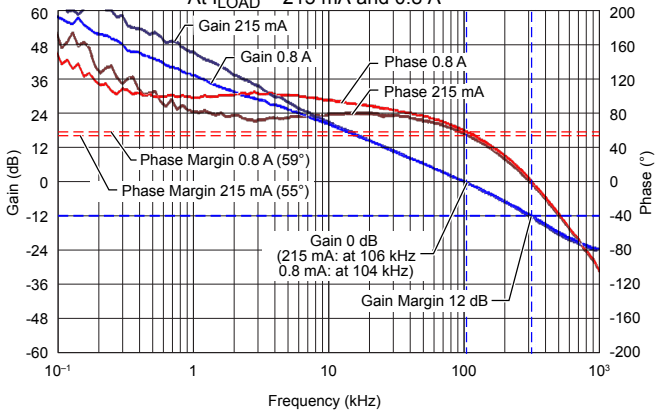
Component	Description	Package	Manufacturer	Part Number
Q_{V33}	MOSFET, 40 V, 90 A, 4.3 mΩ, T_J 175°C	DPAK	Infineon	IPD90N04S3-04
R_{SENSE}	Resistor, 0.300 Ω, 1/4 W, 1%	1206		
R_{CL}	Resistor, 0.390 Ω, 1/4 W, 1%	1206		
R_{DROP}	Resistor, 1.2 Ω total, 1/2 W, 1%	1210		
C_{IN1}, C_{IN2}	Capacitor, Ceramic, 4.7 µF, 50 V, 10%, X7R	1210	Murata	GCM32ER71H475KA55L
C_{VREG}	Capacitor, Ceramic, 10 µF, 16 V, 10%, X7R	1206	Kemet	C1206C106K4RACTU
C_{V33}, C_{V5P}	Capacitor, Ceramic, 2.2 µF, 16 V, 10%, X7R	1206	Murata	GRM31MR71C225KA35L
D_{BUCK}, D_{IN}, D_{V5P}	Diode, Schottky, 2 A, 40 V	SMA	Diodes, Inc.	B240A-13-F
L1	Inductor, 10 µH, 64 mΩ, 2.39 A_{sat}, 165°C	7.6 x 7.6 mm	Cooper/Bussman	DRA73-100-R

Buck Regulator (VREG) Efficiency

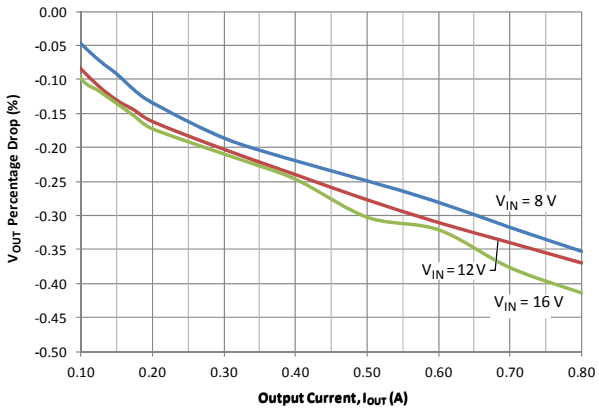


Buck Regulator Bode Plots

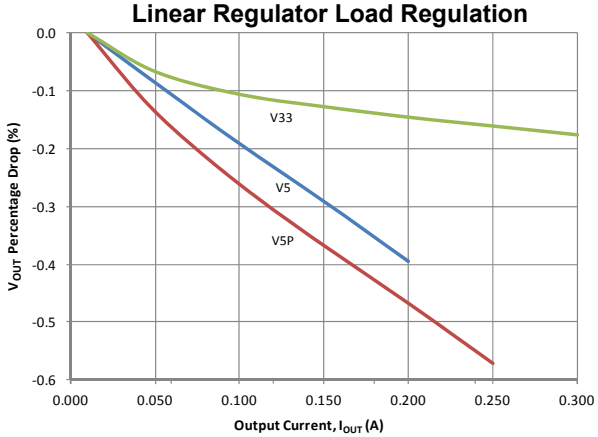
At I_{LOAD} = 215 mA and 0.8 A



Buck Regulator (VREG) Load Regulation



Linear Regulator Load Regulation



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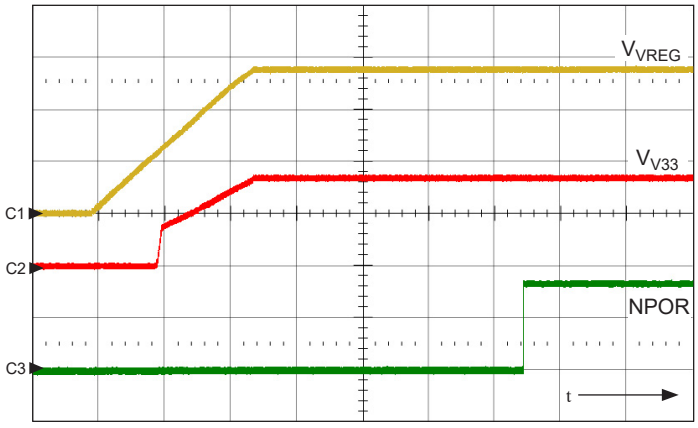
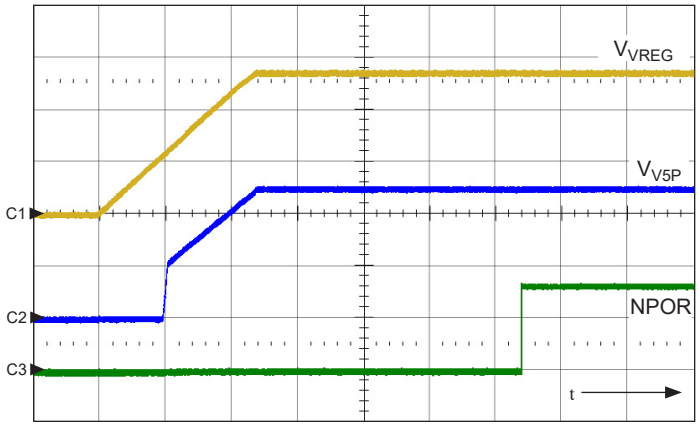
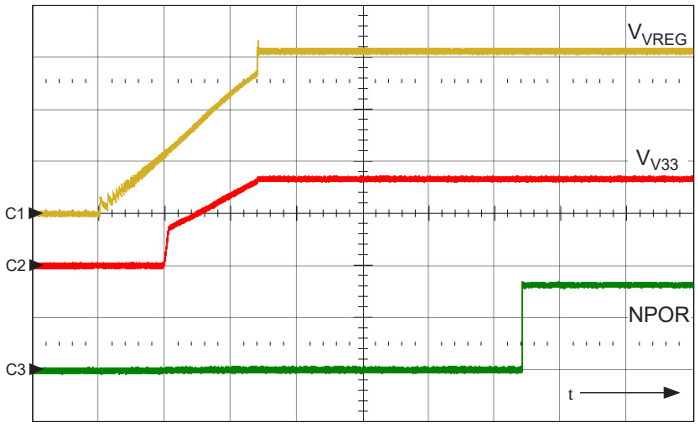


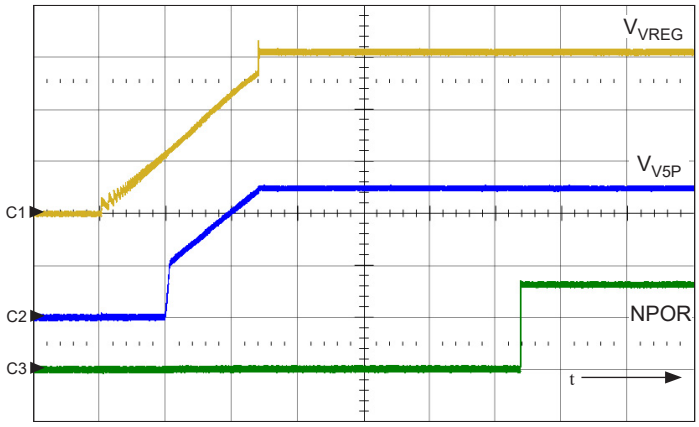
Startup at V_{IN} = 13.5 V; shows V_{VREG} (ch1, 2 V/div.), V_{V33} (ch2, 2 V/div.), NPOR (ch3, 2 V/div.), t = 5 ms/div.



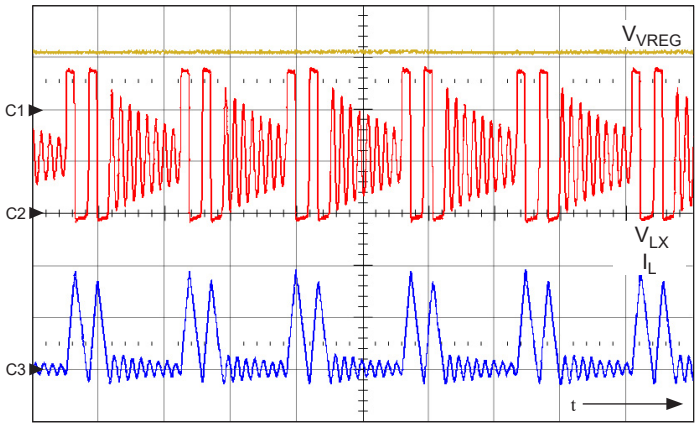
Startup at V_{IN} = 13.5 V; shows V_{VREG} (ch1, 2 V/div.), V_{V5P} (ch2, 2 V/div.), NPOR (ch3, 2 V/div.), t = 5 ms/div.



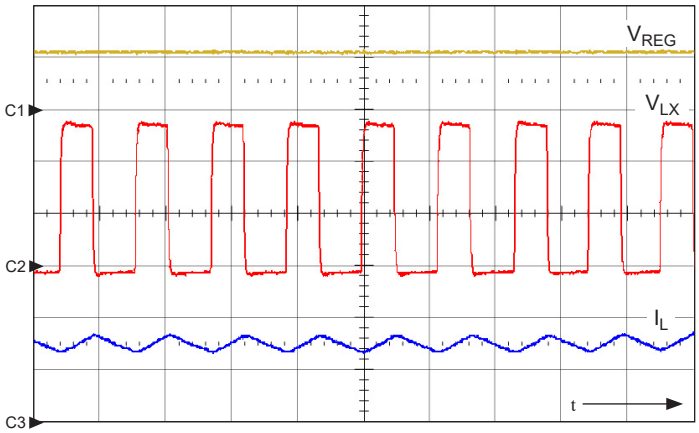
Startup at V_{IN} = 6.5 V; shows V_{VREG} (ch1, 2 V/div.), V_{V33} (ch2, 2 V/div.), NPOR (ch3, 2 V/div.), t = 5 ms/div.



Startup at V_{IN} = 6.5 V; shows V_{VREG} (ch1, 2 V/div.), V_{V5P} (ch2, 2 V/div.), NPOR (ch3, 2 V/div.), t = 5 ms/div.



PWM at V_{BAT} = 12 V with a VREG 25 mA load; shows V_{VREG} (ch1, 5 V/div.), V_{LX} (ch2, 5 V/div.), I_L (ch3, 100 mA/div.), t = 2 µs/div.



PWM at V_{BAT} = 12 V with a VREG 0.8 A load; shows V_{VREG} (ch1, 5 V/div.), V_{LX} (ch2, 5 V/div.), I_L (ch3, 500 mA/div.), t = 500 ns/div.

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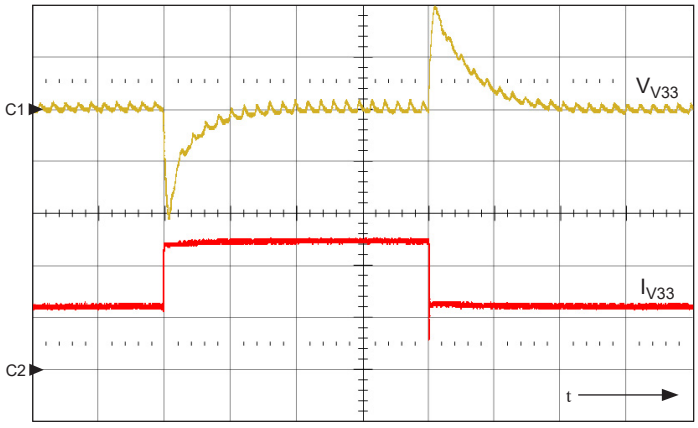
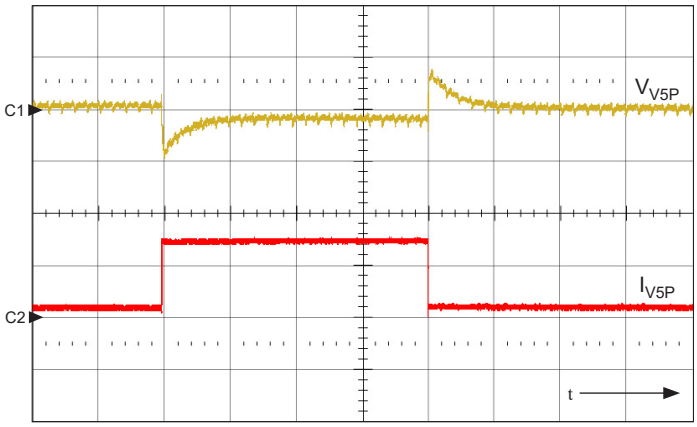
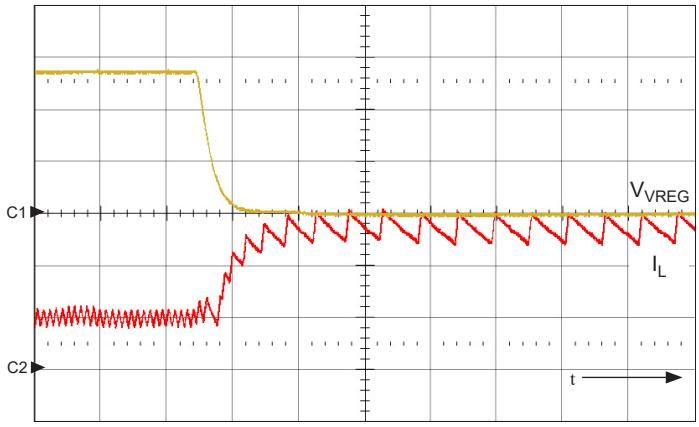


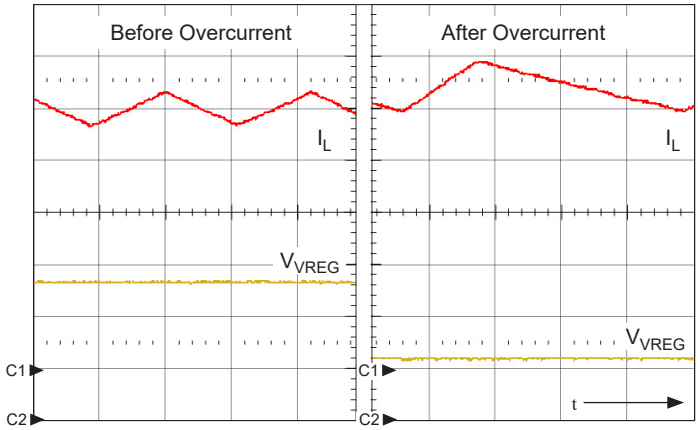
V_{V33} Transient Response: 125 mA to 250 mA; shows V_{V33} (ch1, 50 mV/div.), I_{V33} (ch2, 100 mA/div.), t = 50 µs/div.



V_{V5P} Transient Response: 125 mA to 250 mA; shows V_{V5P} (ch1, 50 mV/div.), I_{V5P} (ch2, 100 mA/div.), t = 50 µs/div.



VREG Short Circuit Operation, V_{IN} = 12 V; shows V_{VREG} (ch1, 2 V/div.), I_L (ch2, 500 mA/div.), t = 5 µs/div.



VREG Normal and Overloaded Operation, V_{IN} = 12 V; shows I_L (ch1, 250 mA/div.), V_{VREG} (ch2, 2 V/div.)

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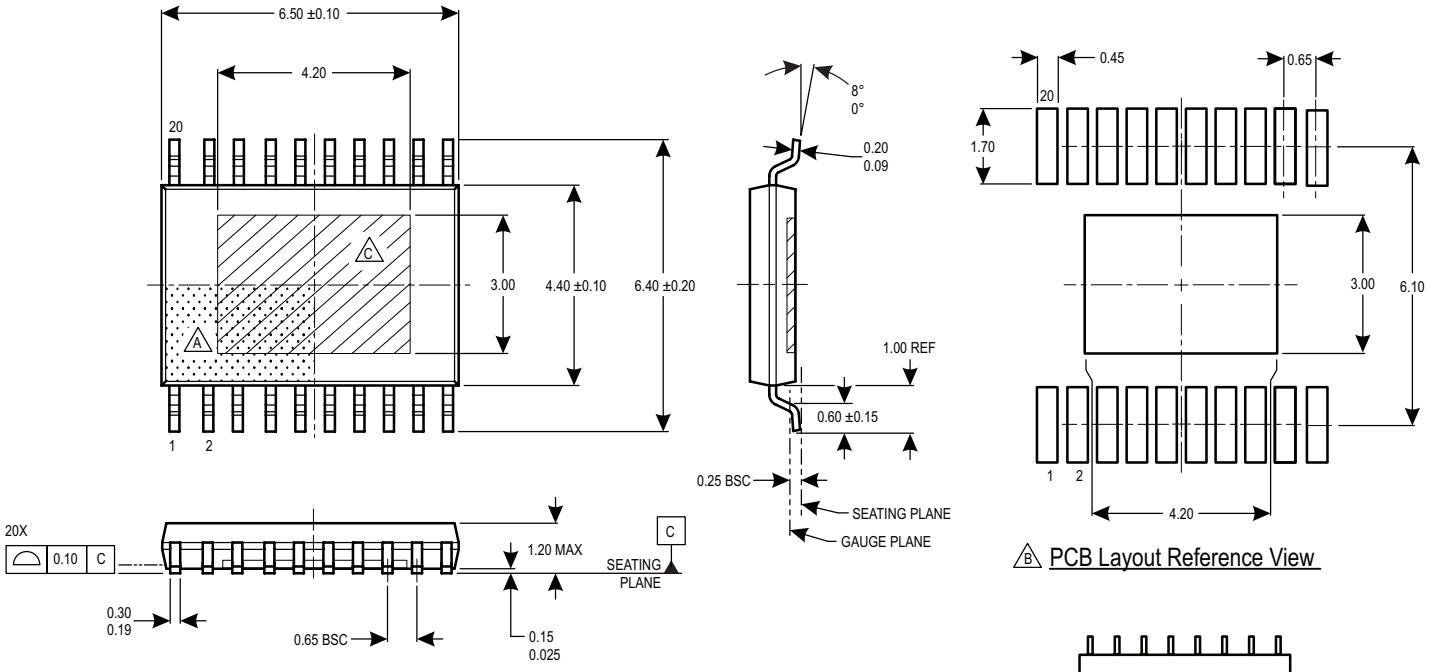
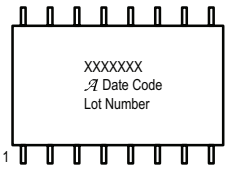
Package LP, 20-Pin TSSOP
with Exposed Thermal Pad

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153ACT; Allegro DWG-0000379, Rev. 3)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



B PCB Layout Reference View



D Standard Branding Reference View

Line 1, 2, 3 = 8 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-21M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface)

D Branding scale and appearance at supplier discretion

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Revision History

Number	Date	Description
2	February 11, 2013	Update typical application and asynchronous diode description
3	May 3, 2019	Minor editorial updates
4	May 11, 2022	Updated package drawing (page 26) and minor editorial updates
5	March 15, 2024	Updated product status to Last-Time Buy

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