A4927

Automotive Half-Bridge MOSFET Driver

Last Time Buy

These parts are in production but have been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: April 1, 2024

Deadline for receipt of LAST TIME BUY orders: July 31, 2024

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, refer to the A4928KLPTR-T.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Automotive Half-Bridge MOSFET Driver

FEATURES AND BENEFITS

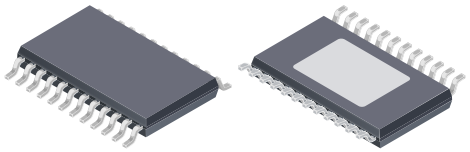
- Half-bridge MOSFET driver
- Bootstrap gate drive for N-channel MOSFET bridge
- Cross-conduction protection with adjustable dead time
- Charge pump regulator for low supply voltage operation
- 5.5 to 50 V supply voltage operating range
- SPI-compatible serial interface
- Bridge control by direct logic inputs or serial interface
- Programmable gate drive
- Current sense amplifier
- Programmable diagnostics
- A²SIL™ product—device features for safety-critical systems

APPLICATIONS

- Anti-lock braking systems (ABS)
- HVAC (blower fan)
- DC pumps (fuel, oil, water)
- Solenoids and actuators
- Similar industrial applications

PACKAGE:

24-lead TSSOP with exposed pad (suffix LP)



Not to scale

DESCRIPTION

The A4927 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a half-bridge arrangement and is specifically designed for automotive applications with high-power inductive loads, such as brush DC motors solenoids and actuators.

The A4927 is intended for automotive systems that must meet ASIL requirements. In common with other Allegro A²SIL™ products, this device incorporates features to complement proper system design, allowing users to achieve the required ASIL level.

A unique charge pump regulator provides full gate drive for battery voltages down to 5.5 V for most applications. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs.

The half bridge can be controlled by independent logic-level inputs or through the SPI-compatible serial interface. The external power MOSFETs are protected from shoot-through by a programmable dead time.

Integrated diagnostics provide indication of multiple internal faults, system faults, and power bridge faults, and can be configured to protect the power MOSFETs under most short-circuit conditions.

In addition to providing full access to the bridge control, the serial interface is also used to alter programmable settings such as dead time, V_{DS} threshold, and fault blank time. Detailed diagnostic information can be read through the serial interface.

The A4927 is supplied in a 24-lead eTSSOP (suffix LP). This package is lead (Pb) free, with 100% matte-tin leadframe plating (suffix –T).

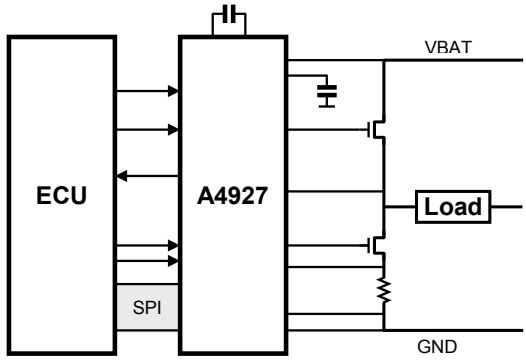


Figure 1: Typical Application

SPECIFICATIONS

SELECTION GUIDE

Part Number	Packing	Package
A4927KLPTR-T	4000 pieces per reel	7.8 mm × 4.4 mm, 1.2 mm max height 24-lead TSSOP with exposed thermal pad

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		–0.3 to 50	V
Regulator Output	V_{REG}	VREG	–0.3 to 16	V
Charge Pump Capacitor Terminal	V_{CP1}	CP1	–0.3 to 16	V
Charge Pump Capacitor Terminal	V_{CP2}	CP2	V_{CP1} – 0.3 to V_{REG} + 0.3	V
Battery-Compliant Logic Input Terminals	V_{IB}	HS, LSn, RESETn, ENABLE	–0.3 to 50	V
Logic Input Terminals	V_I	STRn, SCK, SDI	–0.3 to 6	V
Logic Output Terminal	V_O	SDO	–0.3 to 6	V
Diagnostics Output	V_{DIAG}	DIAG	–0.3 to 50	V
Sense Amplifier Inputs	V_{CSI}	CSP, CSM	–4 to 6.5	V
Sense Amplifier Output	V_{CSO}	CSO, OOS	–0.3 to 6	V
Bridge Drain Monitor Terminal	V_{BRG}	VBRG	–5 to 55	V
Bootstrap Supply Terminal	V_C	C	–0.3 to V_{REG} + 50	V
High-Side Gate Drive Output Terminal	V_{GH}	GH	V_C – 16 to V_C + 0.3	V
		GH (transient)	–18 to V_C + 0.3	V
High-Side Source (Load) Terminal	V_S	S	V_C – 16 to V_C + 0.3	V
		S (transient)	–18 to V_C + 0.3	V
Low-Side Gate Drive Output Terminal	V_{GL}	GL	V_{REG} – 16 to 18	V
		GL (transient)	–8 to 18	V
Bridge Low-Side Source Terminal	V_{LSS}	LSS	V_{REG} – 16 to 18	V
		LSS (transient)	–8 to 18	V
Ambient Operating Temperature Range	T_A	Limited by power dissipation	–40 to 150	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		165	°C
Transient Junction Temperature	T_{Jt}	Overtemperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, guaranteed by design characterization.	180	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[1] With respect to GND. Ratings apply when no other circuit operating constraints are present.

THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	28	°C/W
		2-layer PCB with 3.8 in.^{2} copper each side	38	°C/W
	$R_{\theta JP}$		2	°C/W

[2] Additional thermal information available on the Allegro website.

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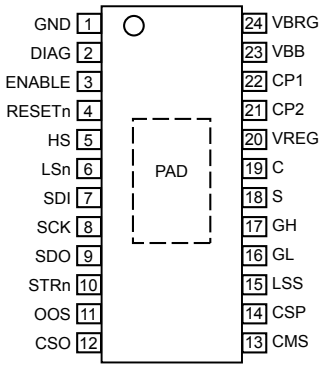
PINOUT DIAGRAM AND TERMINAL LIST TABLE



24-Lead eTSSOP (suffix LP)
Pinout Diagram

Terminal List Table

Name	Number	Function
C	19	Bootstrap capacitor
CP1	22	Pump capacitor CCP connection
CP2	21	Pump capacitor CCP connection
CSM	13	Current sense amplifier (–) input
CSO	12	Current sense amplifier output
CSP	14	Current sense amplifier (+) input
DIAG	2	Diagnostic output
ENABLE	3	Gate drive output control input
GH	17	High-side gate drive output
GL	16	Low-side gate drive output
GND	1	Power ground
HS	5	HS control input
LSn	6	LS control input
LSS	15	Low-side source
OOS	11	Sense amplifier offset output
RESETn	4	Standby mode control input
S	18	Load connection
SCK	8	Serial clock input
SDI	7	Serial data input
SDO	9	Serial data output
STRn	10	Serial strobe (chip select) input
VBB	23	Main power supply
VBRG	24	High-side drain voltage sense
VREG	20	Regulated gate drive supply
PAD	–	Thermal pad; connect to GND

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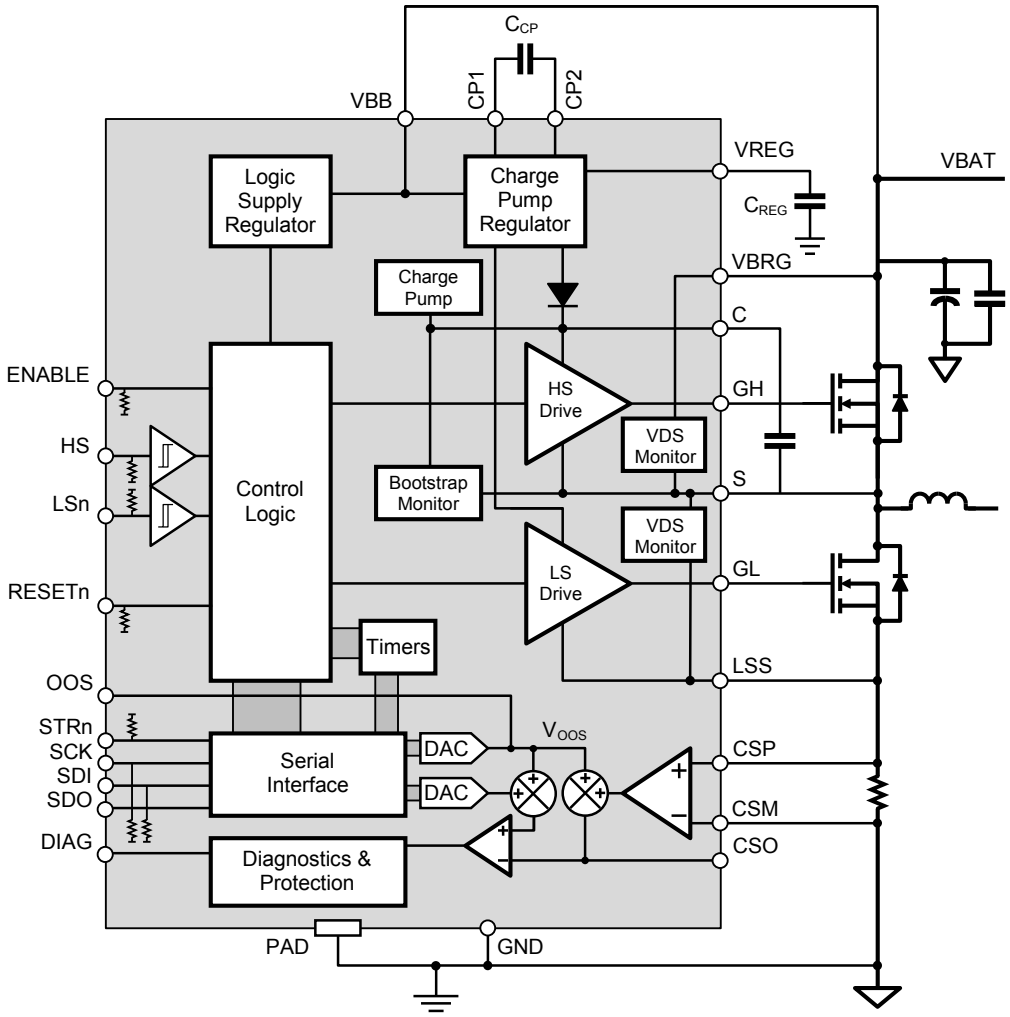

Figure 2: Functional Block Diagram

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ELECTRICAL CHARACTERISTICS: Valid for T_J = –40 to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
VBB Functional Operating Range	V_{BB}	Operating; outputs active	5.5	–	50	V
		Operating; outputs disabled	5	–	50	V
		No unsafe states	0	–	50	V
VBB Quiescent Current	I_{BBQ}	RESETn = high, V_{BB} = 12 V, All gate drive outputs low	–	8	20	mA
	I_{BBS}	RESETn ≤ 300 mV, sleep mode, V_{BB} < 35 V	–	–	20	µA
Internal Logic Supply Regulator Voltage [3][4]	V_{DL}		3.1	3.3	3.5	V
VREG Output Voltage, VRG = 0	V_{REG}	V_{BB} > 7.5 V, I_{VREG} = 0 to 30 mA	7.5	8	8.5	V
		6 V < V_{BB} ≤ 7.5 V, I_{VREG} = 0 to 13 mA	7.5	8	8.5	V
		5.5 V < V_{BB} ≤ 6 V, I_{VREG} < 8 mA	7.5	8	8.5	V
VREG Output Voltage, VRG = 1	V_{REG}	V_{BB} > 9 V, I_{VREG} = 0 to 30 mA	9	11	11.7	V
		7.5 V < V_{BB} ≤ 9 V, I_{VREG} = 0 to 20 mA	9	11	11.7	V
		6 V < V_{BB} ≤ 7.5V, I_{VREG} ≤ 0 to 13mA	7.9	–	–	V
		5.5 V < V_{BB} ≤ 6 V, I_{VREG} < 8 mA	7.9	9.5	–	V
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 10 mA	0.4	0.7	1.0	V
		I_D = 100 mA	1.2	1.9	2.5	V
Bootstrap Diode Current Limit	I_{DBOOT}		250	500	750	mA
Top-Off Charge Pump Current Limit	I_{TOCPM}		50	100	–	µA
High-Side Gate Drive Static Load Resistance	R_{GSH}		250	–	–	kΩ
System Clock Period	t_{OSC}		42.5	50	57.5	ns

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ELECTRICAL CHARACTERISTICS (continued): Valid for T_J = –40 to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE						
Turn-On Time	t_r	C_{LOAD} = 10 nF, 20% to 80%	–	190	–	ns
Turn-Off Time	t_f	C_{LOAD} = 10 nF, 80% to 20%	–	120	–	ns
Pull-Up Peak Source Current	I_{PUPK}		–	400	–	mA
Pull-Up On Resistance	$R_{DS(on)UP}$	IR1 = IR2 = 0, T_J = 25°C, I_{GH} = –150 mA [1]	4	6	10.5	Ω
		IR1 = IR2 = 0, T_J = 150°C, I_{GH} = –150 mA [1]	9.5	12	19	Ω
Pull-Down Peak Sink Current	I_{PDPK}		–	800	–	mA
Pull-Down On Resistance	$R_{DS(on)DN}$	IF1 = IF2 = 0, T_J = 25°C, I_{GL} = 150 mA	1.5	2.4	3.1	Ω
		IF1 = IF2 = 0, T_J = 150°C, I_{GL} = 150 mA	2.9	4	5.5	Ω
GH Output Voltage High	V_{GHH}		V_C – 0.2	–	–	V
GH Output Voltage Low	V_{GHL}	–10 µA < I_{GH} < 10 µA	–	–	V_S + 0.3	V
GL Output Voltage High	V_{GLH}		V_{REG} – 0.2	–	–	V
GL Output Voltage Low	V_{GLL}	–10 µA < I_{GL} < 10 µA	–	–	V_{LSS} + 0.3	V
GH Passive Pull-Down	R_{GHPD}	V_{BB} = 0 V, V_{GH} – V_S < 0.3 V	–	950	–	kΩ
		V_{BB} = 0 V, V_{GL} – V_{LSS} < 0.3 V	–	950	–	kΩ
Turn-Off Propagation Delay	$t_{P(off)}$	Input Change to unloaded Gate output change, (Figure 5) DT[5:0] = 0	60	90	140	ns
		Input Change to unloaded Gate output change, (Figure 5) DT[5:0] > 0	135	165	215	ns
Turn-On Propagation Delay	$t_{P(on)}$	Input Change to unloaded Gate output change, (Figure 5) DT[5:0] = 0	50	80	130	ns
		Input Change to unloaded Gate output change, (Figure 5) DT[5:0] > 0	125	155	205	ns
Propagation Delay Matching (On-to-Off)	Δt_{OO}	DT[5:0]=0	–	15	30	ns
Propagation Delay Matching (GH-to-GL)	Δt_{HL}	Same state change, DT[5:0] = 0	–	–	20	ns
Dead Time (Turn-Off To Turn-On Delay)	t_{DEAD}	Default power-up state (Figure 5)	1.36	1.6	1.84	µs
		Programmable range DT[5:0], nominal	0.1	–	3.15	µs

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ELECTRICAL CHARACTERISTICS (continued): Valid for T_J = –40 to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUT AND OUTPUTS						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}	All logic inputs	2.0	–	–	V
Input Hysteresis	V_{Ihys}	RESETn inputs	200	400	–	mV
Input Hysteresis	V_{Ihys}	All other logic inputs	250	550	–	mV
Input Pull-Down HS, ENABLE, RESETn	R_{PD}	0 < V_{IN} < 3 V	–	50	–	kΩ
	I_{PD}	3 V < V_{IN} < 50 V	–	70	–	µA
Input Pull-Down SDI, SCK	R_{PDS}	0 < V_{IN} < 3 V	–	50	–	kΩ
Input Pull-Up Current to VDL	I_{PU}	STRn	–	70	–	µA
Input Pull-Up to VDL	R_{PU}	LSn	–	170	–	kΩ
Output Low Voltage SDO, DIAG	V_{OL}	I_{OL} = 1 mA	–	0.1	0.4	V
Output High Voltage SDO	V_{OHS}	I_{OS} = –200 µA [1]	V_{DL} – 0.1	–	–	V
		I_{OS} = –1 mA [1]	V_{DL} – 0.4	–	–	V
Output Leakage SDO [1]	I_{OS}	0 V < V_{OS} < V_{DL}, STRn = 1	–1	–	1	µA
Output Current Limit (DIAG)	I_{OLDLIM}	0 V < V_{OD} < 12 V, DIAG active	–	10	17	mA
		18 V ≤ V_{OD} < 50 V, DIAG active	–	–	2.5	mA
Output Leakage [1] (DIAG)	I_{OD}	0 V < V_{OD} < 12 V, DIAG inactive	–1	–	1	µA
		18 V ≤ V_{OD} < 50 V, DIAG inactive	–	–	2.5	mA
LOGIC I/O – DYNAMIC PARAMETERS						
Reset Pulse Width	t_{RST}		0.5	–	4.5	µs
Reset Shutdown Time	t_{RSD}		30	–	–	µs
Input Pulse Filter Time	t_{PIN}	HS, LSn	–	35	–	ns
Clock High Time	t_{SCKH}	A in Figure 4	50	–	–	ns
Clock Low Time	t_{SCKL}	B in Figure 4	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in Figure 4	30	–	–	ns
Strobe Lag Time	t_{STLG}	D in Figure 4	30	–	–	ns
Strobe High Time	t_{STRH}	E in Figure 4	300	–	–	ns
Data Out Enable Time	t_{SDOE}	F in Figure 4	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G in Figure 4	–	–	30	ns
Data Out Valid Time From Clock Falling	t_{SDOV}	H in Figure 4	–	–	40	ns
Data Out Hold Time From Clock Falling	t_{SDOH}	I in Figure 4	5	–	–	ns
Data In Set-Up Time To Clock Rising	t_{SDIS}	J in Figure 4	15	–	–	ns
Data In Hold Time From Clock Rising	t_{SDIH}	K in Figure 4	10	–	–	ns
Wake Up From Sleep	t_{EN}		–	–	2	ms

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CURRENT SENSE AMPLIFIER						
Input Offset Voltage	V_{IOS}		–4	–	+4	mV
Input Offset Voltage Drift	ΔV_{IOS}		–	±4	–	µV/°C
Input Bias Current [1]	I_{BIAS}	0 V < V_{CSP} < V_{DL}, 0 V < V_{CSM} < V_{DL}	–16	–	31	µA
Input Offset Current [1]	I_{OS}	V_{ID} = 0 V, V_{CM} in range	–10	–	+10	µA
Input Common-Mode Range (DC)	V_{CM}	V_{ID} = 0 V	–1.8	–	+2	V
Gain	A_V	Default power-up value	–	35	–	V/V
		Programmable range, SAG[2:0], nominal	10	–	50	V/V
Gain Error	E_A	V_{CM} in range	–5	±2	+5	%
Output Offset	V_{OOS}	Default power-up value	–	2.5	–	V
		Programmable range, SAO[3:0], nominal	0	–	2.5	V
Output Offset Error	E_{VO}	V_{CM} in range, V_{OOS} > 0 V	–10	±2	+10	%
Small Signal –3 dB Bandwidth at Gain = 25	BW	V_{IN} = 10 mV_{pp}	500	–	–	kHz
Output Settling Time (to within 40 mV)	t_{SET}	V_{CSO} = 1 V_{pp} square wave Gain = 25, C_{OUT} = 200 pF	–	1	1.8	µs
Output Dynamic Range	V_{CSOUT}	–100 µA < I_{CSO} < 100 µA	0.3	–	4.8	V
Output Voltage Clamp	V_{CSC}	I_{CSO} = –2 mA	4.85	5.2	5.6	V
Output Current Sink [1]	I_{CSsink}	V_{ID} = 0 V, V_{CSO} = 1.5 V, Gain = 25	0.275	–	–	mA
Output Current Sink (Boosted) [1][5]	$I_{CSsinkb}$	V_{OOS} = 0 V, V_{ID} = –50 mV, V_{CSO} = 1.5 V, Gain = 25	1	–	–	mA
Output Current Source [1]	$I_{CSsource}$	V_{ID} = 200 mV, V_{CSO} = 1.5 V Gain = 25, Offset = 0 V	–	–	–1	mA
VBB Supply Ripple Rejection Ratio	PSRR	V_{ID} = 0 V, 100 kHz, Gain = 25	–	75	–	dB
		V_{CSP} = V_{CSM} = 0 V, DC, Gain = 25	75	–	–	dB
DC Common-Mode Rejection Ratio	CMRR	V_{CM} step from 0 to 200 mV Gain = 25	55	–	–	dB
AC Common-Mode Rejection Ratio	CMRR	V_{CM} = 200 mV_{pp}, 100 kHz, Gain = 25	–	62	–	dB
		V_{CM} = 200 mV_{pp}, 1 MHz, Gain = 25	–	43	–	dB
		V_{CM} = 200 mV_{pp}, 10 MHz, Gain = 25	–	25	–	dB
Common Mode Recovery Time (to within 100 mV)	t_{CMrec}	V_{CM} step from –4 V to +1 V Gain = 25, C_{OUT} = 200 pF	–	1	–	µs
Output Slew Rate 10% to 90%	SR	V_{ID} step from 0 to 175 mV Gain = 25, C_{OUT} = 200 pF	–	10	–	V/µs
Input Overload Recovery (to within 100 mV)	t_{IDrec}	V_{ID} step from 250 mV to 0 V Gain = 25, C_{OUT} = 200 pF	–	1	–	µs

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ELECTRICAL CHARACTERISTICS (continued): Valid for T_J = –40 to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTICS AND PROTECTION						
VREG Undervoltage VRG = 0	V_{RON}	V_{REG} rising	6.4	6.6	6.7	V
	V_{ROFF}	V_{REG} falling	5.5	5.7	5.9	V
VREG Undervoltage VRG = 1	V_{RON}	V_{REG} rising	7.6	7.95	8.2	V
	V_{ROFF}	V_{REG} falling	6.9	7.15	7.4	V
VREG Overvoltage Warning	V_{ROV}	V_{REG} rising	15.5	15.9	16.5	V
VREG Overvoltage Hysteresis	V_{ROVHys}		1200	1500	–	mV
VBB Overvoltage Warning	V_{BBOV}	V_{BB} rising	32	–	36	V
VBB Overvoltage Hysteresis	$V_{BBOVHys}$		1	–	–	V
VBB POR Voltage	V_{BBR}	V_{BB}	–	3.5	–	V
Bootstrap Undervoltage	V_{BCUV}	V_{BOOT} falling, $V_{BOOT} = V_C - V_S$	56	–	64	$\%V_{REG}$
Bootstrap Undervoltage Hysteresis	$V_{BCUVHys}$		–	13	–	$\%V_{REG}$
Gate Drive Undervoltage Warning HS	V_{GSHUV}	V_{GSH}	V_{BOOT} – 1.25	V_{BOOT} – 1	V_{BOOT} – 0.8	V
Gate Drive Undervoltage Warning LS	V_{GSLUV}	V_{GSL}	V_{REG} – 1.25	V_{REG} – 1	V_{REG} – 0.8	V
VBRG Input Voltage	V_{BRG}	When VDS monitor is active	5.5	V_{BB}	50	V
VBRG Input Current	I_{VBRG}	V_{DSTH} = default, V_{BB} = 12 V 0 V < V_{BRG} < V_{BB}	–	–	500	µA
	I_{VBRGQ}	Sleep mode V_{BB} < 35 V	–	–	5	µA
VDS Threshold – High Side	V_{DSTH}	Default power-up value	1.1	1.2	1.3	V
		Programmable range VT[5:0], nominal V_{BRG} ≥ 7 V	0	–	3.15	V
		Programmable range VT[5:0] 5.5 V ≤ V_{BRG} < 7 V [6]	0	–	1.5	V
High-Side VDS Threshold Offset [2]	V_{DSTHO}	High-side on, V_{DSTH} ≥1 V, V_{BRG} > 7 V	–200	±100	200	mV
		High-side on, V_{DSTH} < 1 V	–150	±50	150	mV
VDS Threshold – Low Side	V_{DSTL}	Default power-up value	1.1	1.2	1.3	V
		Programmable range, V_{BB} ≥ 5.5 V [6]	0	–	3.15	V
Low-Side VDS Threshold Offset [2]	V_{DSTLO}	Low-side on, V_{DSTL} ≥ 1 V, V_{BRG} > 7 V	–200	±100	200	mV
		Low-side on, V_{DSTL} < 1 V	–150	±50	150	mV
VDS Qualify Time	t_{VDQ}	Default power-up value (Figure 6)	1.36	1.6	1.84	µs
		Programmable range TVD[5:0], nominal	0	–	6.3	µs
Overcurrent Voltage	V_{OCT}	Default power-up value	2.7	3.0	3.3	V
		Programmable range, OCT[3:0], nominal	0.3	–	4.8	V
Overcurrent Qualify Time	t_{OCQ}		6.75	7.5	8.25	µs
Temperature Warning Threshold	T_{JWH}	Temperature increasing	125	135	145	°C
Temperature Warning Hysteresis	T_{JWHhys}	Recovery = $T_{JWH} - T_{JWHhys}$	–	15	–	°C
Overtemperature Threshold	T_{JF}	Temperature increasing	170	175	180	°C
Overtemperature Hysteresis	T_{JHys}	Recovery = $T_{JF} - T_{JHys}$	–	15	–	°C

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.
[2] VDS offset is the difference between the programmed threshold, V_{DSTH} or V_{DSTL} and the actual trip voltage.
[3] VDL derived from VBB for internal use only. Not accessible on any device terminal.
[4] Verified by design and characterization.
[5] If the amplifier output voltage (V_{CSO}) is more positive than the value demanded by the applied differential input (V_{ID}) and output offset (V_{OOS}) conditions, then output current sink capability is boosted to enhance negative-going transient response.
[6] Maximum value of VDS threshold that should be set in the configuration registers for correct operation when V_{BRG} is within the stated range.

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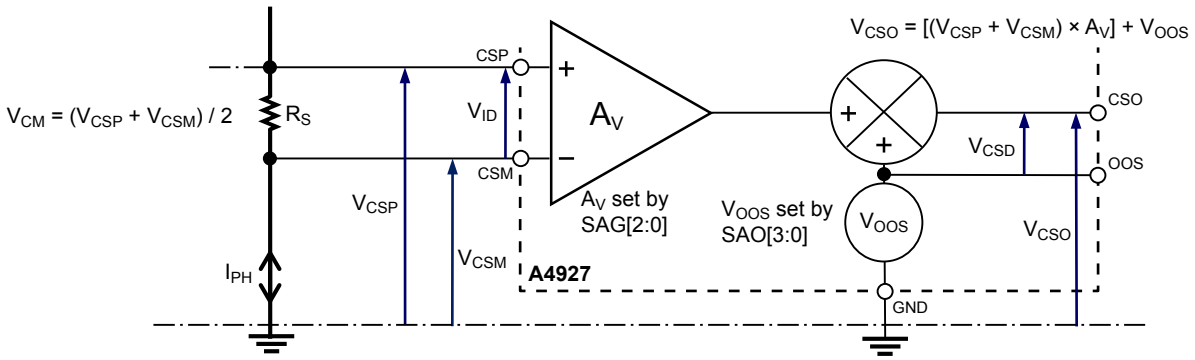

Figure 3: Sense Amplifier Voltage Definitions

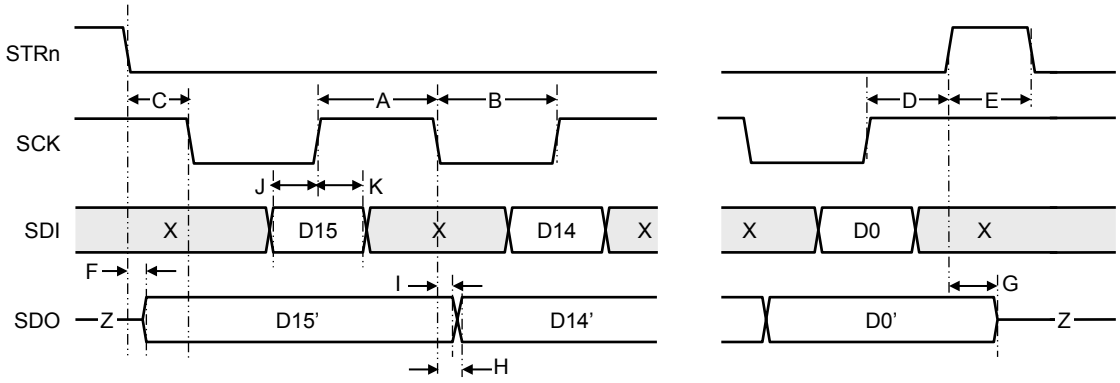

Figure 4: Serial Interface Timing (X = don't care, Z = high impedance (tri-state))

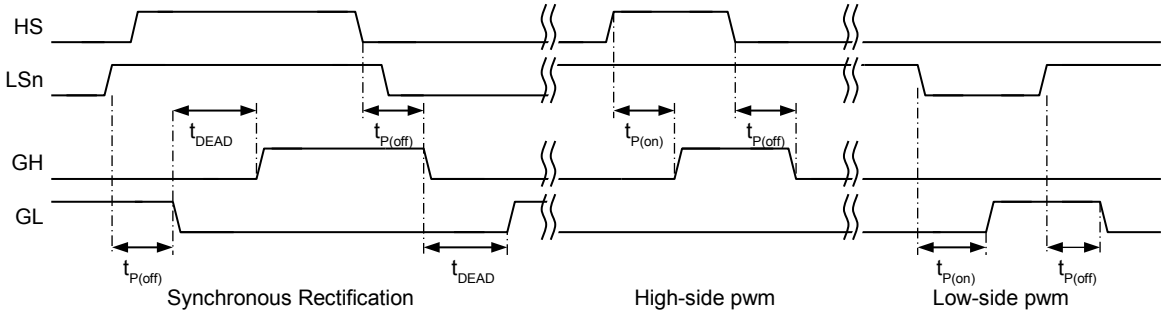

Figure 5: Gate Drive Timing – Control Inputs

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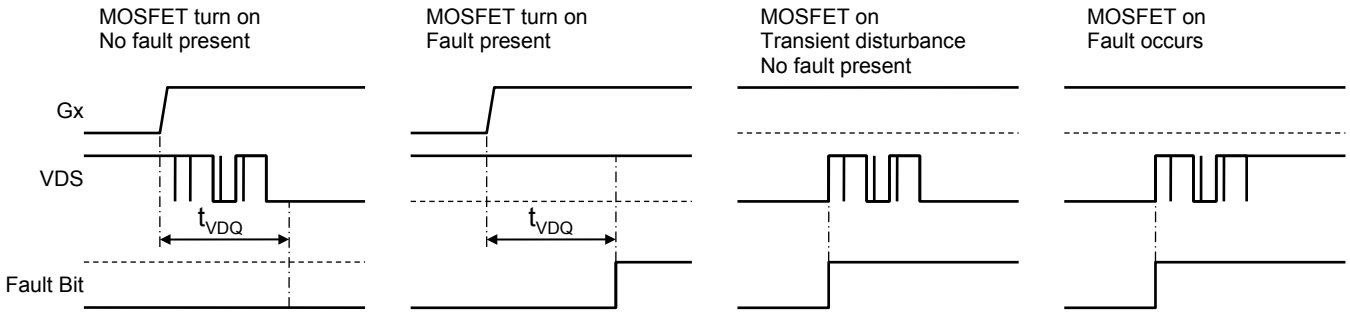

Figure 6a: VDS Fault Monitor – Blank Mode Timing (VDQ = 1)

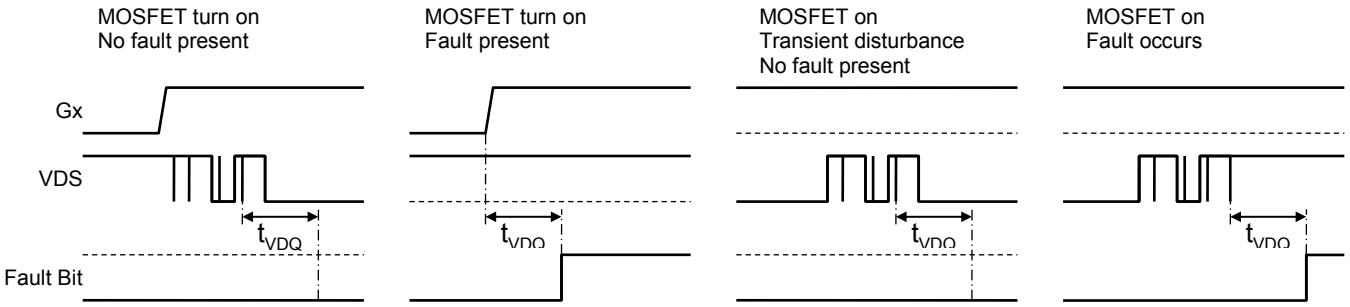

Figure 6b: VDS Fault Monitor – Debounce Mode Timing (VDQ = 0)

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LOGIC TRUTH TABLES

Table 1: Control Logic (Control by Logic Inputs)

HS	LSn	GH	GL	S
0	1	LO	LO	Z
0	0	LO	HI	LO
1	1	HI	LO	HI
1	0	LO	LO	Z

HI = high-side FET active, LO = low-side FET active
Z = high impedance, both FETs off
All control register bits set to 0, RESETn = 1, ENABLE = 1

Table 2: Control Logic (Control by Serial Register)

HSR	LSR	GH	GL	S
0	0	LO	LO	Z
0	1	LO	HI	LO
1	0	HI	LO	HI
1	1	LO	LO	Z

HI = high-side FET active, LO = low-side FET active
Z = high impedance, both FETs off
HS = 0, LSN = 1, RESETn = 1, ENABLE = 1

Table 3: Control combination logic table – Logic Inputs and Serial Register

Terminal	Register	Internal
HS	HSR	HI
0	0	0
0	1	1
1	0	1
1	1	1

Terminal	Register	Internal
LSn	LSR	LO
0	0	1
0	1	1
1	0	0
1	1	1

Internal control signals (HI, LO) are derived by combining the logic states applied to the control input terminals (HS, LS) with the bit patterns held in the Control register (HSR, LSR).

Normally the input terminals or the Control register method is used for control with the other being held inactive (all terminals or bits at logic 0).

ENABLE	HI	LO	GH	GL	S	Comment
1	0	0	L	L	Z	Bridge disabled
1	0	1	L	H	LO	Bridge sinking
1	1	0	H	L	HI	Bridge sourcing
1	1	1	L	L	Z	Bridge disabled
0	X	X	L	L	Z	Bridge disabled

X = don't care

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FUNCTIONAL DESCRIPTION

The A4927 is a half-bridge (H-bridge) MOSFET driver (pre-driver) requiring a single unregulated supply of 5.5 to 50 V. It includes an integrated linear regulator to supply the internal logic. All logic inputs are TTL compatible and can be driven by 3.3 or 5 V logic.

The two high-current gate drives are capable of driving a wide range of N-channel power MOSFETs, and are configured as a half-bridge driver with one high-side drive and one low-side drive. The A4927 provides all necessary circuits to ensure that the gate-source voltage of both high-side and low-side external FETs are above 10 V, at supply voltages down to 7 V. For extreme battery voltage drop conditions, correct functional operation is guaranteed at supply voltages down to 5.5 V, but with a reduced gate drive voltage.

Gate drives can be controlled directly through the logic input terminals or through an SPI-compatible serial interface. The sense of the logic inputs are arranged to allow the bridge to be driven by a single PWM input if required. The bridge can also be driven by direct logic inputs or by two PWM signals depending on the required complexity. The logic inputs are battery voltage compliant, meaning they can be shorted to ground or supply without damage, up to the maximum battery voltage of 50 V.

Bridge efficiency can be enhanced by using the synchronous rectification ability of the drives. When synchronous rectification is used, cross-conduction (shoot through) in the external bridge is avoided by an adjustable dead time. A hardwired logic lockout ensures that the high-side and the low-side cannot be permanently active at the same time.

A low-power sleep mode allows the A4927, the power bridge, and the load to remain connected to a vehicle battery supply without the need for an additional supply switch.

The A4927 includes a number of diagnostic features to provide indication and/or protection against undervoltage, overtemperature, and power bridge faults. A single diagnostic output provides basic fault indication and detailed diagnostic information is available through the serial interface. The serial interface also provides access to programmable dead time, fault blanking time and programmable VDS threshold for short detection.

The A4927 includes a low-side current sense amplifier with programmable gain and offset. The amplifier is specifically designed for current sensing in the presence of high voltage and current transients.

Input and Output Terminal Functions

VBB: Main power supply for internal regulators and charge pump. The main power supply should be connected to VBB through a reverse voltage protection circuit and should be decoupled with ceramic capacitors connected close to the supply and ground terminals.

VBRG: Sense input to the top of the external MOSFET bridge. Allows accurate measurement of the voltage at the drain of the high-side MOSFET in the bridge.

CP1, CP2: Pump capacitor connection for charge pump. Connect a minimum 220 nF, typically 470 nF, ceramic capacitor between CP1 and CP2.

VREG: programmable regulated voltage, 8 or 11 V, used to supply the low-side gate drivers and to provide current for the above supply charge pump. A sufficiently large storage capacitor must be connected to this terminal to provide the required transient charging current.

GND: Analog, digital, and power ground. Connect to supply ground–see Layout Recommendations.

C: High-side connection for the bootstrap capacitor and positive supply for the high-side gate driver.

GH: High-side, gate-drive output for an external N-channel MOSFET.

S: Source connection for high-side MOSFET providing the negative supply connections for the floating high-side driver.

GL: Low-side gate-drive output for an external N-channel MOSFET.

LSS: Low-side return path for discharge of the capacitance on the low-side MOSFET gate, connected to the source of the low-side external MOSFET independently through a low-impedance track.

HS: Logic inputs with pull-down to control the high-side gate drive. Battery voltage compliant terminal.

LSn: Logic input with pull-up to control the low-side gate drive. This is an active-low input. Battery voltage compliant terminal.

ENABLE: Logic input to enable the gate drive outputs. Battery voltage compliant terminal.

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RESETn: Clears latched faults that may have disabled the outputs when taken low for the reset pulse width, t_{RST}. Forces low-power shutdown (sleep) when held low for more than the RESET shutdown time, t_{RSD}. Battery voltage compliant terminal.

SDI: Serial data logic input with pull-down. 16-bit serial word input msb first.

SDO: Serial data output. High impedance when STRn is high. Outputs bit 15 of the diagnostic register, the fault flag, as soon as STRn goes low.

SCK: Serial clock logic input with pull-down. Data is latched in from SDI on the rising edge of SCK. There must be 16 rising edges per write and SCK must be held high when STRn changes.

STRn: Serial data strobe and serial access enable logic input with pull-up. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

CSP, CSM: Current sense amplifier inputs.

CSO: Current sense amplifier output.

OOS: Monitor point for programmable analogue output offset voltage applied to current sense amplifiers.

DIAG: Diagnostic output. Provides general fault flag output.

Power Supplies

A single power supply voltage is required. The main power supply, V_{BB}, should be connected to VBB through a reverse voltage protection circuit. A 100 nF ceramic decoupling capacitor must be connected close to the supply and ground terminals.

An internal regulator provides the supply to the internal logic. All logic is guaranteed to operate correctly to below the regulator undervoltage levels ensuring that the A4927 will continue to operate safely until all logic is reset when a power-on-reset state is present.

The A4927 will operate within specified parameters with V_{BB} from 7 to 50 V and will function correctly with a supply down to 5.5 V. This provides a rugged solution for use in the harsh automotive environment.

Pump Regulator

The gate drivers are powered by a programmable voltage internal regulator which limits the supply to the drivers and therefore the maximum gate voltage. At low supply voltage, the regulated supply is maintained by a charge pump boost converter which requires a pump capacitor, typically 470 nF, connected between the CP1 and CP2 terminals.

The regulated voltage, V_{REG}, can be programmed to 8 or 11 V and is available on the VREG terminal. The voltage level is selected by the value of the VRG bit. When VRG = 1, the voltage is set to 11 V; when VRG = 0 the voltage is set to 8 V. A sufficiently large storage capacitor (see Application Information section) must be connected to this terminal to provide the transient charging current to the low-side drivers and the bootstrap capacitors.

Gate Drives

The A4927 is designed to drive external, low on-resistance, power N-channel MOSFETs. It will supply the large transient currents necessary to quickly charge and discharge the external MOSFET gate capacitance in order to reduce dissipation in the external MOSFET during switching. The charge current for the low-side drive is provided by the capacitor on the VREG terminal. The charge current for the high-side drives is provided by the bootstrap capacitor connected between the C and S terminals. MOSFET gate charge and discharge rates may be controlled by setting a group of parameters via the serial interface or by using an external gate resistor between the gate drive output and the gate terminal of the MOSFET.

Bootstrap Supply

When the high-side drivers are active, the reference voltage for the driver will rise to close to the bridge supply voltage. The supply to the driver will then have to be above the bridge supply voltage to ensure that the driver remains active. This temporary high-side supply is provided by a bootstrap capacitor connected between the bootstrap supply terminal, C, and the high-side reference terminal, S.

The bootstrap capacitor is independently charged to approximately V_{REG} when the associated reference S terminal is low. When the output swings high, the voltage on the bootstrap supply terminal rises with the output to provide the boosted gate voltage needed for the high-side N-channel power MOSFETs.

Bootstrap Charge Management

The A4927 monitors the bootstrap capacitor charge voltage to ensure sufficient high-side drive. It also includes an optional bootstrap capacitor charge management system (bootstrap manager) to ensure that the bootstrap capacitor remains sufficiently charged under all conditions. The bootstrap manager is enabled by default but may be disabled by setting the DBM bit to 1. This

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may be required in systems where the output MOSFET switching must only be allowed by the controlling processor.

Before a high-side drive can be turned on, the bootstrap capacitor voltage must be higher than the turn-on voltage threshold, V_{BCUV} + $V_{BCUVHys}$. If this is not the case, then the A4927 will attempt to charge the bootstrap capacitor by activating the low-side drive. Under normal circumstances this will charge the capacitor above the turn-on voltage in a few microseconds and the high-side drive will then be enabled. The bootstrap voltage monitor remains active while the high-side drive is active and if the voltage drops below the turn-off voltage threshold, V_{BCUV}, a charge cycle is also initiated.

The bootstrap charge management circuit may actively charge the bootstrap capacitor regularly when the PWM duty cycle is very high, particularly when the PWM off-time is too short to permit the bootstrap capacitor to become sufficiently charged.

In some systems, it may not be desirable to permit this feature. In this case the bootstrap manager may be disabled by setting the DBM bit to 1. If the bootstrap manager is disabled, then the user must ensure that the bootstrap capacitor does not become discharged below the bootstrap undervoltage threshold, V_{BCUV}, or a bootstrap fault will be indicated and the outputs disabled. This can happen with very high PWM duty cycles when the charge time for the bootstrap capacitor is insufficient to ensure a sufficient recharge to match the MOSFET gate charge transfer during turn on.

If, for any reason, the bootstrap capacitor cannot be sufficiently charged a bootstrap fault will occur—see diagnostics section for further details.

Top-Off Charge Pump

An additional “top-off” charge pump is provided, which will allow the high-side drive to maintain the gate voltage on the external MOSFET indefinitely, ensuring so-called 100% PWM if required. This is a low-current trickle charge pump and is only operated after a high side has been signaled to turn on. There is a small amount of bias current drawn from the C terminal to operate the floating high side circuit (<40 µA) and the charge pump simply provides enough drive to ensure the bootstrap voltage, and hence the gate voltage, will not droop due to this bias current.

In some applications, a safety resistor is added between the gate and source of each MOSFET in the bridge. When a high-side MOSFET is held in the on state, the current through the associated high-side gate-source resistor (R_{GSH}) is provided by the high-side driver and therefore appears as a static resistive load on the top-off charge pump. The minimum value of R_{GSH} for which the top-off charge pump can provide current, without dropping below the bootstrap undervoltage threshold, is defined in the Electrical Characteristics table.

In all cases, the charge required for initial turn-on of the high-side gate is always supplied by the bootstrap capacitor. If the bootstrap capacitor becomes discharged, the top-off charge pump alone will not provide sufficient current to allow the MOSFET to turn on.

High-Side Gate Drive

A high-side gate-drive output for an external N-channel MOSFETs is provided on the GH terminal. GH = 1 (or “high”) means that the upper-half of the driver is turned on and its drain will source current to the gate of the high-side MOSFET in the external load-driving bridge, turning it on. GH = 0 (or “low”) means that the lower-half of the driver is turned on and its drain will sink current from the external MOSFET’s gate circuit to the S terminal, turning it off.

The reference point for the high-side drive is the load connections, S. This terminal senses the voltage at the load connections. This terminal is also connected to the negative side of the bootstrap capacitor and is the negative supply reference connections for the floating high-side driver. The discharge current from the high-side MOSFET gate capacitance flows through these connections which should have low-impedance traces to the MOSFET bridge.

Low-Side Gate Drive

The low-side gate-drive output on GL is referenced to the LSS terminal. This output is designed to drive an external N-channel power MOSFET. GL = 1 (or “high”) means that the upper-half of the driver is turned on and its drain will source current to the gate of the low-side MOSFET in the external power bridge, turning it on. GL = 0 (or “low”) means that the lower-half of the driver is turned on and its drain will sink current from the external MOSFET’s gate circuit to the LSS terminal, turning it off.

The LSS terminal provides the return path for discharge of the capacitance on the low-side MOSFET gate. This terminal is connected independently to the source of the low-side external MOSFETs through a low-impedance track.

An integrated slew control feature allows the MOSFET gate charge and discharge rates to be controlled via the serial interface as detailed in the Gate Drive Control section.

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Either the internal slew control or an external resistor between the gate drive output and the gate connection to the MOSFET (as close as possible to the MOSFET) can be used to control the slew rate seen at the gate, thereby controlling the di/dt and dv/dt of the voltage at the S terminal.

Gate Drive Passive Pull-Down

Each gate drive output includes a discharge circuit to ensure that any external MOSFET connected to the gate drive output is held off when the power is removed. This discharge circuit appears as 950 kΩ between the gate drive and the source connections for each MOSFET. It is only active when the A4927 is not driving the output to ensure that any charge accumulated on the MOSFET gate has a discharge path even when the power is not connected.

Dead Time

To prevent cross-conduction (shoot through) of the power MOSFET bridge, it is necessary to have a dead-time delay between a high- or low-side turn-off and the next turn-on event. The potential for cross-conduction occurs when the high-side and low-side pair of MOSFETs is switched at the same time, for example, at the PWM switch point. In the A4927, the dead time is set by the contents of the DT[5:0] bits in configuration register 0. These six bits contain a positive integer that determines the dead time by division from the system clock.

The dead time is defined as:

$$t_{DEAD} = n \times 50\ ns$$

where n is a positive integer defined by DT[5:0] and

t_{DEAD} has a minimum active value of 100 ns.

The accuracy of t_{DEAD} is determined by the accuracy of the system clock as defined in the electrical characteristics table. The range of it is 100 ns to 3.15 µs. A value of 1 or 2 in DT[5:0] will set the minimum active dead time of 100 ns.

If DT[5:0] is left at the default value of zero, the dead timer is disabled and no minimum dead time is generated by the A4927. The logic that prevents permanent cross-conduction is, however, still active. Adequate dead time must be generated externally by, for example, the microcontroller producing the drive signals applied to the A4927 logic inputs or Control register.

The internally generated dead time is only present if the on command for one MOSFET occurs within one dead time after the off command for the complimentary MOSFET. In the case where one side of the drive is permanently off the dead time will not occur. In this case the gate drive will turn on within the specified propagation delay after the input goes high. (see Figure 5).

Gate Drive Control

MOSFET gate drives are controlled according to the values set in Config 6, 7, and 8 registers.

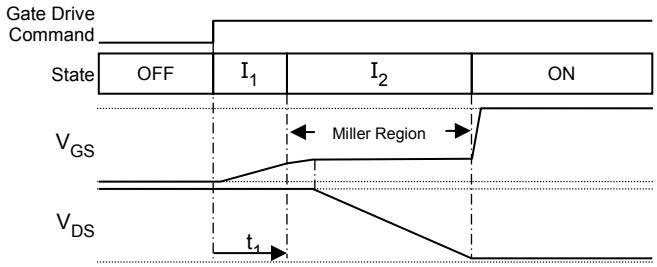

Figure 7a: Off-to-On Transition (Gate Drive)

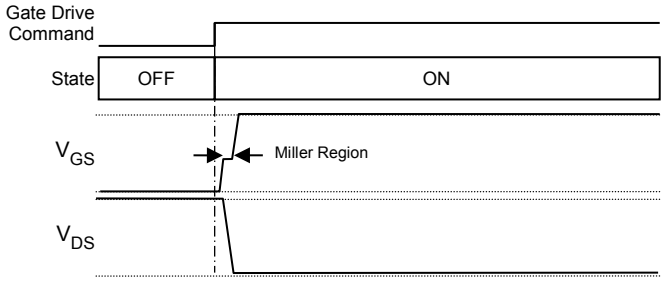

Figure 7b: Off-to-On Transition (Switched)

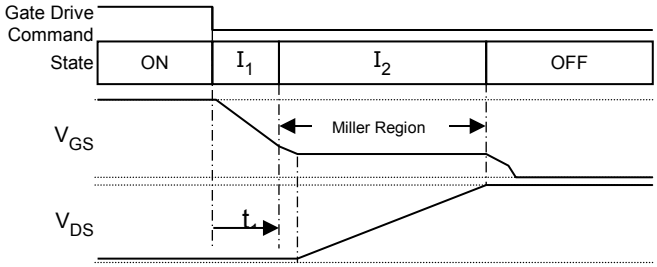

Figure 7c: On-to-Off Transition (Gate Drive)

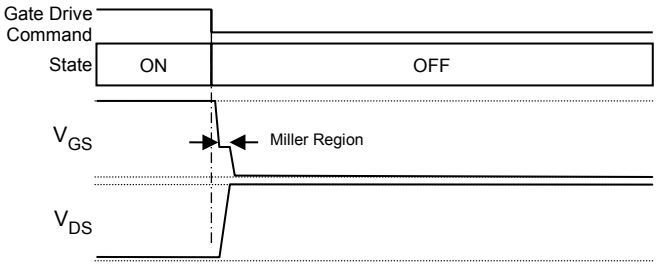

Figure 7d: On-to-Off Transition (Switched)

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MOSFET off-to-on transitions are controlled as detailed in Figure 7a. When a gate drive is commanded to turn on a current, I_1 (as defined by IR1[3:0]), is sourced on the GH or GL terminal for a duration, t_1 (defined by TR[3:0]). These parameters should typically be set so as to quickly charge the MOSFET input capacitance to the start of the Miller region as drain-source voltage does not change during this period. Thereafter, the current sourced on GH or GL is set to a value of I_2 (as defined by IR2[3:0]) and remains at this value while the MOSFET transitions through the Miller region, and reaches the fully on state. For the high-side MOSFET, fully on is assumed when the drain-source voltage, $V_{DS} = V_{BRG} – V_S, < V_{DSTH}$. For the low-side MOSFET, fully on is assumed when $V_{DS} = V_S – V_{LSS}, < V_{DSTL}$.

I_2 should be set to achieve the required input capacitance charge time. Once in the fully on state, the GH or GL output switches from current to voltage drive to hold the MOSFET in the on state.

If the values of IR1[3:0] and IR2[3:0] are set to 0, GH or GL produces maximum drive to turn on the MOSFET as quickly as possible without attempting to control the MOSFET input capacitance charge time (Figure 7b). The value of TR[3:0] has no effect on switching speed.

MOSFET on-to-off transitions are controlled as detailed in Figure 7c. When a gate drive is commanded to turn off, a current, I_1 (as defined by IF1[3:0]), is sunk by the GH or GL terminal for a duration, t1 (defined by TF[3:0]). These parameters should typically be set so as to quickly discharge the MOSFET input capacitance to the start of the Miller region as drain-source voltage does not change during this period. Thereafter, the current sunk by GH or GL is set to a value of I_2 (as defined by IF2[3:0]) and remains at this value while the MOSFET transitions through the Miller region and reaches the fully off state. For the high-side MOSFET, fully off is assumed when V_{DS}(low side) = $V_S – V_{LSS} < V_{DSTH}$. For the low-side MOSFET, fully off is assumed when V_{DS}(high side) = $V_{BRG} – V_S < V_{DSTH}$. I_2 should be set to achieve the required MOSFET input capacitance discharge time. Once in the fully off condition, the GH or GL output switches from current to voltage drive to hold the MOSFET in the off state.

If the values of IF1[3:0] and IF2[3:0] are set to 0, GH or GL produces maximum drive to turn off the MOSFET as quickly as possible without attempting to control the MOSFET input capacitance discharge time (Figure 7d). The value of TF[3:0] has no effect on switching speed.

Dead time, DT[5:0] in the Config 0 register, must be set to a non-zero value for gate drive control to be operational. Otherwise, maximum drive will be produced on all switching transitions to minimize MOSFET switching times.

Logic Control Inputs

Two logic level digital inputs provide direct control for the gate drives, one for each drive. These TTL threshold logic inputs can be driven from 3.3 or 5 V logic and all have a typical hysteresis of 500 mV to improve noise performance. Each input can be shorted to the VBB supply, up to the absolute maximum supply voltage, without damage to the input.

Input HS is active high and controls the high-side drive. LSn is active low and controls the low-side drive. The logical relationship between the inputs and the gate drive outputs is defined in Table 1.

The logic sense of the inputs (active high or active low) are arranged to permit the bridge to be controlled with 1 or 2 inputs. The control inputs can be driven together to control both high-side and low-side drives with a single PWM input to provide synchronous rectification.

The gate drive outputs can also be controlled through the serial interface by setting the appropriate bit in the control register. In the control register all bits are active high. The logical relationship between the register bit setting and the gate drive outputs is defined in Table 2.

The logic inputs are combined, using logical OR, with the corresponding bits in the serial interface control register to determine the state of the gate drive. The logical relationship between the combination of logic input and register bit setting and the gate drive outputs is defined in Table 3. In most applications, either the logic inputs or the serial control will be used. When using only the logic inputs to control the bridge the serial register should be left in the reset condition with all control bits set to 0. When using only the serial interface to control the bridge, the inputs should be tied such that the active-low inputs are pulled high and the active-high inputs connected to GND—that is, HS tied to GND and LSn tied high. The internal pull-up and pull-down resistors on these inputs ensure that they go to the inactive state should they become disconnected from the control signal level.

Internal lockout logic ensures that the high-side output drive and low-side output drive cannot be active simultaneously. When the control inputs request active high-side and low-side at the same time, then both high-side and low side gate drives will be forced low.

Output Disable

The ENABLE input is connected directly to the gate drive output command signal, bypassing all gate drive control logic. This can be used to provide a fast output disable (emergency cutoff).

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Sleep Mode

RESETn is an active-low input which allows the A4927 to enter sleep mode, in which the current consumption from the VBB supply and internal logic regulator is reduced to its minimum level. When RESETn is held low for longer than the reset shutdown time, t_{RSD}, the regulator and all internal circuitry is disabled and the A4927 enters sleep mode. In sleep mode, the latched faults and corresponding fault flags are cleared. When coming out of sleep mode, the protection logic ensures that the gate drive outputs are off until the charge pump reaches its correct operating condition. The charge pump will stabilize in approximately 2 ms under nominal conditions.

To allow the A4927 to start up without the need for an external logic input, the RESETn terminal can be pulled to VBB with an external pull-up resistor.

RESETn can also be used to clear any fault conditions without entering sleep mode by taking it low for the reset pulse width, t_{RST}. Any latched short detection fault, which disables the outputs, will be cleared, as will the serial fault register.

Current Sense Amplifier

A programmable gain, differential sense amplifier is provided to allow the use of low-value sense resistors or current shunt as a low-side current sensing element. The input common mode range of the CSP and CSM inputs and programmable output offset allow below ground current sensing typically required for low-side current sense in PWM control of motors, or other inductive loads, during switching transients. The output of the sense amplifier is available at the CSO output and can be used in peak or average current control systems. The output can drive up to 4.8 V to permit maximum dynamic range with higher input voltage A-to-D converters.

The gain of the sense amplifier is defined by the contents of the SAG[2:0] variable as:

SAG	Gain
0	10
1	15
2	20
3	25

SAG	Gain
4	30
5	35
6	40
7	50

The output offset, V_{OOS}, of the sense amplifier is defined by the contents of the SAO[3:0] variable as:

SAO	V_{OOS}
0	0
1	0
2	100 mV
3	100 mV
4	200 mV
5	300 mV
6	400 mV
7	500 mV

SAO	V_{OOS}
8	750 mV
9	1 V
10	1.25 V
11	1.5 V
12	1.75 V
13	2 V
14	2.25 V
15	2.5 V

Diagnostic Monitors

Multiple diagnostic features provide three levels of fault monitoring. These include critical protection for the A4927, monitors for operational voltages and states, and detection of the power bridge and load fault conditions. All diagnostics, except for POR, serial transfer error and overtemperature, can be masked by setting the appropriate bit in the mask registers.

Table 4: Diagnostic Functions

Name	Diagnostic	Level
POR	Internal logic supply undervoltage causing power-on reset	Chip
SE	Serial transmission error	Chip
OT	Chip junction overtemperature	Chip
TW	High chip junction temperature warning	Monitor
VSO	VBB supply overvoltage (Load dump detection)	Monitor
VRO	VREG output overvoltage	Monitor
VRU	VREG output undervoltage	Monitor
OC	Overcurrent	Bridge
VBS	Bootstrap undervoltage	Bridge
HU	High-side VGS undervoltage	Bridge
LU	Low-side VGS undervoltage	Bridge
HO	High-side VDS overvoltage	Bridge
LO	Low-side VDS overvoltage	Bridge

The fault status is available from the status and diagnostic registers accessed through the serial interface.

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DIAG Output

The DIAG terminal provides a single diagnostic signal that outputs a general logic-level active-low fault flag. DIAG remains low while any fault except SE or OC is present or if one of the latched faults has been detected and the outputs disabled. When the general fault flag is reset the DIAG output will be high.

Status and Diagnostic Registers

The serial interface allows detailed diagnostic information to be read from the diagnostic registers on the SDO output terminal at any time.

A system status register provides a summary of all faults in a single read transaction. The status register is always output on SDO when any register is written.

The first bit (bit 15) of the status register contains a common fault flag, FF, which will be high if any of the fault bits in the status register have been set. This allows fault condition to be detected using the serial interface by simply taking STRn low. As soon as STRn goes low the first bit in the status register can be read on SDO to determine if a fault has been detected at any time since the last fault register reset. In all cases the fault bits in the diagnostic registers are latched and only cleared after a fault register reset.

FF provides an indication that a fault has occurred since the last fault reset and one or more fault bits have been set.

Note that FF (bit 15) does not provide the same function as the general fault flag output on the DIAG terminal. The fault flag output on the DIAG terminal provides an indication that either a fault is present or the outputs have been disabled due to a latched fault state. FF provides an indication that a fault has occurred since the last fault reset and one or more fault bits have been set.

Chip-Level Protection

Chip-wide parameters critical for correct operation of the A4927 are monitored. These include maximum chip temperature, minimum internal logic supply voltage and the serial interface transmission. These three monitors are necessary to ensure that the A4927 is able to respond as specified.

CHIP FAULT STATE: INTERNAL LOGIC UNDERVOLTAGE (POR)

The A4927 has an independent internal logic regulator to supply the internal logic. This is to ensure that external events, other than loss of supply, do not prevent the A4927 from operating correctly. The internal logic supply regulator will continue to operate with a low supply voltage, for example, if the main supply voltage drops to a very low value during a severe cold crank event. In extreme low supply circumstances, or during power-up or power-down, an undervoltage detector ensures that the A4927 operates correctly. The logic supply undervoltage lockout cannot be masked as it is essential to guarantee correct operation over the full supply range.

When power is first applied to the A4927, the internal logic is prevented from operating, and all gate drive outputs held in the off state until the internal regulator voltage, V_{DL}, exceeds the logic supply undervoltage lockout rising (turn-on) threshold, V_{DLON}. At this point, all serial control registers will be reset to their power-on state and all fault states will be reset. The FF bit and the POR bit in the status register will be set to one to indicate that a power-on-reset has taken place. The A4927 then goes into its fully operational state and begins operating as specified.

Once the A4927 is operational, the internal logic supply continues to be monitored. If, during the operational state, V_{DL} drops below logic supply undervoltage lockout falling (turn-off) threshold, V_{DLOFF}, then the logical function of the A4927 cannot be guaranteed and the outputs will be immediately disabled. The A4927 will enter a power-down state and all internal activity, other than the logic regulator voltage monitor will be suspended. If the logic supply undervoltage is a transient event, then the A4927 will follow the power-up sequence above as the voltage rises.

CHIP FAULT STATE: OVERTEMPERATURE (OT)

If the chip temperature rises above the overtemperature threshold, T_{JF}, the overtemperature bit, OT, will be set in the status register. If ESF = 1 when an overtemperature is detected, all gate drive outputs will be disabled automatically. If ESF = 0, then no circuitry will be disabled and action must be taken by the user to limit the power dissipation in some way so as to prevent overtemperature damage to the chip and unpredictable device operation. When the temperature drops below T_{JF} by more than the hysteresis value, T_{JFHys}, the fault state is cleared, and when ESF = 1, the outputs are re-enabled. The overtemperature bit remains in the status register until reset.

CHIP FAULT STATE: SERIAL ERROR (SE)

If there are more than 16 rising edges on SCK or if STRn goes high and there are fewer than 16 rising edges on SCK or the parity is not odd, then the write will be cancelled without writing data to the registers and the SE bit will be set to indicate a data transfer error. If the transfer is a write, then the status register will not be reset. If the transfer is a diagnostic register read, then the addressed register will not be reset.

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Operational Monitors

Parameters related to the safe operation of the A4927 in a system are monitored. These include parameters associated with external active and passive components, power supplies, and interaction with external controllers.

Voltages relating to driving the external power MOSFETs are monitored, specifically V_{REG}, the bootstrap capacitor voltage, and the V_{GS} of each gate drive output. The main supply voltage, V_{BB}, is only monitored for overvoltage events. It is not monitored for minimum voltage since the critical minimum voltage is generated by the VREG charge pump regulator provided by the A4927.

MONITOR: VREG VOLTAGE (VR: VRO, VRU)

The internal charge-pump regulator supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that the regulated voltage, V_{REG}, at the VREG terminal is sufficiently high before enabling any of the outputs.

If V_{REG} goes below the VREG undervoltage threshold, V_{ROFF}, the VREG undervoltage bit, VRU, will be set in the diagnostic register. All gate drive outputs will go low, the motor drive will be disabled, and the motor will coast. When V_{REG} rises above the rising threshold, V_{RUON}, the gate drive outputs are re-enabled and the fault state is cleared. The VRU bit remains in the diagnostic register until cleared.

The VREG undervoltage monitor circuit is active during power up and all gate drives will be low until V_{REG} is greater than approximately 8 V(with VRG = 1). Note that this is sufficient to turn on standard threshold external power MOSFETs at a battery voltage as low as 5.5 V, but the on-resistance of the MOSFET may be higher than its specified maximum.

The VREG undervoltage monitor can be disabled by setting the VRU bit in the mask register. Although not recommended, this can allow the A4927 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters will not be valid in this condition.

The output of the VREG regulator is also monitored to detect any overvoltage applied to the VREG terminal. If V_{REG} goes above the VREG overvoltage threshold, V_{ROV}, the VREG overvoltage bit, VRO, will be set in the diagnostic register. No action will be taken as the gate drive outputs are protected from overvoltage by independent Zener clamps. When V_{REG} falls below V_{ROV} by more than the hysteresis voltage, V_{ROVHys}, the fault state is cleared but VRO bit remains in the diagnostic register until cleared.

MONITOR: TEMPERATURE WARNING (TW)

If the chip temperature rises above the temperature warning threshold, T_{JW}, the hot warning bit, TW, will be set in the status register. No action will be taken by the A4927. When the temperature drops below T_{JW} by more than the hysteresis value, T_{JWHys}, the fault state is cleared and the TW bit remains in the status register until reset.

MONITOR: VBB SUPPLY OVERVOLTAGE (VSO)

If V_{BB} rises above the VBB overvoltage warning threshold, V_{BBOV}, then the VSO bit will be set in the Diagnostic 2 register and the VS bit will be set in the Status register. The general fault flag will be set but all gate drive outputs will continue to function. When V_{BB} drops below the falling VBB overvoltage warning threshold, $V_{BBOV} - V_{BBOVHys}$, the general fault flag will be cleared but the VSO and VS bits will remain set. The fault state will only be reset by a low pulse on the RESETn input, by a serial read of the diagnostic or status register or by a power-on reset.

Power Bridge and Load Faults

BRIDGE: OVERCURRENT DETECT (OC)

The output from the sense amplifier can be compared to an overcurrent threshold voltage, V_{OCT}, to provide indication of overcurrent events. V_{OCT}, is generated by a 4-bit DAC with a resolution of 300 mV and defined by the contents of the OC[3:0] variable and the contents of the SAO[3:0] variable. V_{OCT} is approximately defined as:

$$V_{OCT} = [(n + 1) \times 300\ mV]$$

where n is a positive integer defined by OCT[3:0]

Any offset programmed on SAO[3:0] is applied to both the current sense amplifier output, V_{CSO}, and the Overcurrent threshold, V_{OCT}, and has no effect on the overcurrent threshold, I_{OCT}. The relationship between the threshold voltage and the threshold current is approximately defined as:

$$I_{OCT} = V_{OCT} / (R_S \times A_V)$$

where V_{OCT} is the overcurrent threshold voltage programmed by OCT[3:0], R_S is the sense resistor value in Ω and A_V is the sense amp gain defined by SAG[2:0].

The output from the overcurrent comparator is filtered by an overcurrent qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid overcurrent event. The qualifier can operate in one of two ways, debounce or blanking, selected by the OCQ bit.

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In the default debounce mode, a timer is started each time the comparator output indicates an overcurrent. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{OCQ}, then the overcurrent event is considered valid and the overcurrent bit, OC, will be set in the Diag 2 register.

In the optional blanking mode, a timer is started when a low-side gate drive is turned on. The output from the comparator is ignored (blanked) for the duration of the timeout period, set by t_{OCQ}. If a comparator output indicates an overcurrent event when the blanking timer is not active then the overcurrent event is considered valid and the overcurrent bit, OC, will be set in the Diag 2 register.

When a valid overcurrent is detected, no action is taken and only the OC bit is set. The fault state will be reset by a low pulse on the RESETn input, by a serial read of the diagnostic or status register or by a power-on reset.

BRIDGE: BOOTSTRAP CAPACITOR UNDERVOLTAGE FAULT (VBS)

The A4927 monitors the bootstrap capacitor charge voltage to ensure sufficient high-side drive. It also includes an optional bootstrap capacitor charge management system (bootstrap manager) to ensure that the bootstrap capacitor remains sufficiently charged under all conditions. The bootstrap manager is enabled by default but may be disabled by setting the DBM bit to 1. This may be required in systems where the output MOSFET switching must only be allowed by the controlling processor.

If the bootstrap manager is disabled, then the user must ensure that the bootstrap capacitor does not become discharged below the bootstrap undervoltage threshold, V_{BCUV}, or a bootstrap fault will be indicated and the outputs disabled. This can happen with very high PWM duty cycles when the charge time for the bootstrap capacitor is insufficient to ensure a sufficient recharge to match the MOSFET gate charge transfer during turn on.

When the bootstrap manager is active, the bootstrap capacitor voltage must be higher than the turn-on voltage limit before a high-side drive can be turned on. If this is not the case, then the A4927 will attempt to charge the bootstrap capacitor by activating the low-side drive. Under normal circumstances, this will charge the capacitor above the turn-on voltage in a few microseconds and the high-side drive will then be enabled. The bootstrap voltage monitor remains active while the high-side drive is active, and if the voltage drops below the turn-off voltage, a charge cycle is also initiated.

If there is a fault that prevents the bootstrap capacitor charging during the managed recharge cycle, then the charge cycle will timeout after typically 200 µs and the bootstrap undervoltage fault is considered to be valid. If the bootstrap manager is disabled and a bootstrap undervoltage is detected when a high-side MOSFET is active or being switched on, then the bootstrap undervoltage is immediately valid.

The action taken when a valid bootstrap undervoltage fault is detected and the fault reset conditions depend on the state of the ESF bit.

If ESF = 0, the fault state will be latched, the bootstrap undervoltage fault bit in the status register, V_{BS}, will be set, and the high-side MOSFET will be disabled. The fault state, but not the bootstrap undervoltage fault bit, will be reset by a low pulse on the RESETn input or the next time the MOSFET is commanded to switch on. If the MOSFET is being driven with a PWM signal, then this will usually mean that the MOSFET will be turned on again each PWM cycle. If this is the case, and the fault condition remains, then a valid fault will again be detected after the timeout period and the sequence will repeat. The fault state will be reset by a low pulse on the RESETn input, by a serial read of the diagnostic or status register or by a power-on reset.

If ESF = 1, the fault will be latched, the associated bootstrap undervoltage fault bit will be set, and all MOSFETs will be disabled. The fault state will be reset by a low pulse on the RESETn input, by a serial read of the diagnostic or status register or by a power-on reset.

The bootstrap undervoltage monitor can be disabled by setting the VBS bit in the mask register. Although not recommended, this can allow the A4927 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters may not be valid in this condition.

BRIDGE: MOSFET VDS OVERVOLTAGE FAULT (DSO: HO, LO)

Faults on the external MOSFETs are determined by monitoring the drain-source voltage of the MOSFET and comparing it to a drain-source overvoltage threshold, V_{DST}. V_{DST} is generated by an internal DAC and is defined by the values in the VT[5:0] variable. This variable provides the input to a 6-bit DAC with a least significant bit value of typically 50 mV. The output of the DAC produces the threshold voltage approximately defined as:

$$V_{DST} = n \times 50\ mV$$

where n is a positive integer defined by VT[5:0]

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The drain-source voltage for the low-side MOSFET is measured between the S terminal and the LSS terminal. Using the LSS terminal rather than the ground connection avoids adding any low-side current sense voltage to the real low-side drain-source voltage and avoids false VDS fault detection.

The drain-source voltage for the high-side MOSFET is measured between the S terminal and the VBRG terminal. Using the VBRG terminal rather than VBB avoids adding any reverse diode voltage or high-side current sense voltage to the real high-side drain-source voltage and avoids false VDS fault detection.

The VBRG terminal is an independent low-current sense input to the top of the MOSFET bridge. It should be connected independently and directly to the common connection point for the drain of the power bridge MOSFET at the positive supply connection point in the bridge. The input current to the VBRG terminal is proportional to the drain-source threshold voltage, V_{DST}, and is approximately:

$$I_{VBRG} = 72 \times V_{DST} + 52$$

where I_{VBRG} is the current into the VBRG terminal in µA and V_{DST} is the drain-source threshold voltage described above.

Note that the VBRG terminal can withstand a negative voltage up to –5 V. This allows the terminal to remain connected directly to the top of the power bridge during reverse battery conditions where the body diodes of the power MOSFETs are used to clamp the negative voltage.

The output from each VDS overvoltage comparator is filtered by a VDS fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid VDS fault. The duration of the VDS fault qualifying timer, t_{VDQ}, is determined by the contents of the TVD[5:0] variable. t_{VDQ} is approximately defined as:

$$t_{VDQ} = n \times 100\ ns$$

where n is a positive integer defined by TVD[5:0].

The qualifier can operate in one of two ways: debounce mode or blanking mode, selected by the VDQ bit.

In the default debounce mode, a timer is started each time the comparator output indicates a VDS fault detection when the corresponding MOSFET is active. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period set by t_{VDQ}, then the VDS fault is considered valid and the corresponding VDS fault bit, LO or HO, will be set in the diagnostic register.

In the optional blanking mode, a timer is started when a gate drive is turned on. The output from the VDS overvoltage comparator for the MOSFET being switched on is ignored (blanked) for the duration of the timeout period, set by t_{VDQ}. If the comparator output indicates an overvoltage event when the MOSFET is switched on and the blanking timer is not active then the VDS fault is considered valid and the corresponding VDS fault bit, LO or HO will be set in the diagnostic register.

If a valid VDS fault is detected, the fault will be latched and the associated MOSFET will be disabled. This state will remain until reset depending on the value set in the ESF bit.

If ESF = 1, the fault state will only be reset by a low pulse on the RESETn input, by a serial read of the diagnostic register, or by a power-on reset.

If ESF = 0, the fault state, but not the VDS fault bit, will be reset the next time the MOSFET is commanded to switch on. If the MOSFET is being driven with a PWM signal, then this will usually mean that the MOSFET will be turned on again each PWM cycle. If this is the case, and the fault conditions remains, then a valid fault will again be detected after the timeout period and the sequence will repeat. The fault state will be reset by a low pulse on the RESETn input, by a serial read of the diagnostic register, or by a power-on reset.

If ESF = 0, care must be taken to avoid damage to the MOSFET where the VDS fault is detected. Although the MOSFET will be switched off as soon as the fault is detected at the end of the fault validation timeout, it is possible that it could still be damaged by excessive power dissipation and heating. To limit any damage to the external MOSFETs or the load, the MOSFET should be fully disabled by logic inputs from the external controller.

BRIDGE: VGS UNDERVOLTAGE (GSU: HU, LU)

To ensure that the gate drive output is operating correctly, each gate drive output voltage is independently monitored, when active, to ensure the drive voltage, V_{GS}, is sufficient to fully enhance the power MOSFET in the external bridge.

If V_{GS}, on any active gate drive output, goes below the gate drive undervoltage warning, V_{GSUV}, the general fault flag will be active and the corresponding gate drive undervoltage bit, HU or LU, will be set in the diagnostic register. No other action will be taken. When V_{GS} rises above V_{GSUV} by more than the hysteresis voltage, $V_{GSUVHys}$, the general fault flags go inactive. The fault bits remain in the diagnostic register until cleared.

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MOSFET FAULT STATE: SHORT TO SUPPLY

A short from the load connections to the battery or VBB connection is detected by monitoring the voltage across the low-side MOSFET using the S terminal and the LSS terminal. This drain-source voltage is then compared to the low-side Drain-Source Threshold Voltage, V_{DSTL}. If the blanking timer is active, the output from the VDS overvoltage comparator will be ignored for t_{VDQ}. While the low-side VDS fault is detected, the VDS fault bit, LO, will be set in the diagnostic register and the low-side MOSFET will be disabled. When ESF is set to 1, both MOSFETs will be disabled.

MOSFET FAULT STATE: SHORT TO GROUND

A short from the load connection to ground is detected by monitoring the voltage across the low-side MOSFET using the S terminal and the voltage at VBRG. This drain-source voltage is then compared to the high-side Drain-Source Threshold Voltage, V_{DSTH}. If the blanking timer is active, the output from the VDS overvoltage comparator will be ignored for t_{VDQ}. While the low-side VDS fault is detected, the VDS fault bit, HO, will be set in the diagnostic register and the high-side MOSFET will be disabled. When ESF is set to 1, both MOSFETs will be disabled.

Fault Action

The action taken when one of the diagnostic functions indicates a fault is listed in Table 5.

When a fault is detected, a corresponding fault state is considered to exist. In some cases, the fault state only exists during the time the fault is detected. In other cases, when the fault is only detected for a short time, the fault state is latched (stored) until reset. The faults that are latched are indicated in Table 5. Latched fault states are always reset when RESETn is taken low, a power-on-reset state is present or when the associated fault bit is read through the serial interface. Any fault bits that have been set in the status or diagnostic register are only reset when a power-on-reset state is present or when the associated fault bit is read through the serial interface. RESETn low will not reset the fault bits in the status or diagnostic registers.

The fault conditions power-on-reset and VREG undervoltage are considered critical to the safe operation of the A4927 and the system. If these faults are detected, then the gate drive outputs are automatically driven low and both MOSFETs in the bridge held in the off state. This state will remain until the fault is removed.

For the logic terminal overvoltage and overtemperature fault conditions, the action taken depends on the status of the ESF bit. If a fault is detected on any of these two diagnostics and ESF = 1, then all the gate drive outputs will be driven low and all MOSFETs in the bridge held in the off state. This state will remain until the fault is removed. If ESF = 0, then the gate drive outputs will not be affected.

If a VDS fault or bootstrap undervoltage fault is detected, then the action taken will also depend on the status of the ESF bit, but these faults are handled as a special case. If a fault is detected on any of these two diagnostics and ESF = 1, then both gate drive outputs will be driven low and both MOSFETs in the bridge will be held in the off state. When ESF = 1, this fault state will be latched and remain until reset. If a VDS fault or bootstrap undervoltage fault is detected and ESF = 0, then only the gate drive output to the MOSFET where the fault was detected will be driven low and the MOSFET will be held in the off state. When ESF = 0, the VDS fault or bootstrap undervoltage fault state will be latched but will be reset the next time the MOSFET is commanded to switch on. For all other faults, the gate drive outputs will remain enabled.

Fault Masks

Individual diagnostics—except power-on reset, serial transmission error, and overtemperature—can be disabled by setting the corresponding bit in the mask register. Power-on-reset cannot be disabled because the diagnostics and the output control depend on the logic regulator to operate correctly. If a bit is set to one in the mask register, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated and no fault flags or diagnostic bits will be set. See Mask Register definition for bit allocation. Care must be taken when diagnostics are disabled to avoid potentially damaging conditions.

Table 5: Fault Actions

Fault Description	Disable Outputs		Fault State Latched
	ESF = 0	ESF = 1	
No Fault	No	No	-
Power-on-Reset	Yes [1]	Yes [1]	No
VREG undervoltage	Yes [1]	Yes [1]	No
VREG overvoltage	No	No	No
VBB overvoltage	No	No	No
Overtemperature	No	Yes [1]	No
Temperature warning	No	No	No
Serial transmission error	No	No	No
Bootstrap undervoltage	Yes [2]	Yes [1]	Yes
Overcurrent	No	No	No
VDS overvoltage	Yes [2]	Yes [1]	Yes
VGS undervoltage	No	No	No

[1] Both gate drives low, both MOSFETs off.
[2] Gate drive to the affected MOSFET low, only the affected MOSFET off.

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SERIAL INTERFACE

Table 6: Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: Config 0	0	0	0	0	WR					DT5	DT4	DT3	DT2	DT1	DT0	P
						0	0	0	0	1	0	0	0	0	0	
1: Config 1	0	0	0	1	WR	OCT3	OCT2	OCT1	OCT0	VT5	VT4	VT3	VT2	VT1	VT0	P
						1	0	0	1	0	1	1	0	0	0	
2: Config 2	0	0	1	0	WR		VDQ									P
						0	0	0	0	0	0	0	0	0	0	
3: Config 3	0	0	1	1	WR					TVD5	TVD4	TVD3	TVD2	TVD1	TVD0	P
						0	0	0	0	0	1	0	0	0	0	
4: Config 4	0	1	0	0	WR				VRG							P
						0	0	0	1	0	0	0	0	0	0	
5: Config 5	0	1	0	1	WR			SAO3	SAO2	SAO1	SAO0		SAG2	SAG1	SAG0	P
						0	0	1	1	1	1	0	1	0	1	
6: Config 6	0	1	1	0	WR			TR3	TR2	TR1	TR0	TF3	TF2	TF1	TF0	P
						0	0	0	0	0	1	0	0	0	1	
7: Config 7	0	1	1	1	WR			IR13	IR12	IR11	IR10	IF13	IF12	IF11	IF10	P
						0	0	0	0	0	0	0	0	0	0	
8: Config 8	1	0	0	0	WR			IR23	IR22	IR21	IR20	IF23	IF22	IF21	IF20	P
						0	0	0	0	0	0	0	0	0	0	
10: Mask 0	1	0	1	0	WR			VBS	TW					HU	LU	P
						0	0	0	0	0	0	0	0	0	0	
11: Mask 1	1	0	1	1	WR	VRO	VRU	VSO						HO	LO	P
						0	0	0	0	0	0	0	0	0	0	
12: Diag 0	1	1	0	0	0									HU	LU	P
						0	0	0	0	0	0	0	0	0	0	
13: Diag 1	1	1	0	1	0	VRO	VRU							HO	LO	P
						0	0	0	0	0	0	0	0	0	0	
14: Diag 2	1	1	1	0	0	VSO				VBS				OC		P
						0	0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Continued on the next page...

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Table 6:Serial Register Definition (continued)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15: Control	1	1	1	1	WR			DBM	ESF					HSR	LSR	P
						0	0	0	1	0	0	0	0	0	0	
Status	FF	POR	SE		OT	TW	VS			VR		OC	VBS	GSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

A three-wire synchronous serial interface, compatible with SPI, is used to control the features of the A4927. The SDO terminal can be used, during a serial transfer, to provide diagnostic feedback and readback of the register contents.

The A4927 can be operated without the serial interface using the default settings and the logic control inputs; however, application specific configurations are only possible by setting the appropriate register bits through the serial interface. In addition to setting the configuration bits, the serial interface can also be used to control the bridge MOSFETs directly.

The serial interface timing requirements are specified in the Electrical Characteristics table, and illustrated in Figure 4. Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. STRn is normally held high, and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple slave units to use common SDI and SCK connections. Each slave then requires an independent STRn connection. The SDO output assumes a high-impedance state when STRn is high, allowing a common data readback connection.

When 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the registers are reset depending on the type of transfer.

If there are more than 16 rising edges on SCK or if STRn goes high and there are fewer than 16 rising edges on SCK—either being described as a framing error—the write will be cancelled without latching data to the register. The Status register will not be reset.

The first four bits, D[15:12], in a serial word, are the register address bits giving the possibility of 16 register addresses. The fifth bit, WR (D[11]), is the write/read bit. When WR is 1, the following 10 bits, D[10:1], clocked in from the SDI terminal, are written to the addressed register. When WR is 0, then no data is written to the serial registers and the contents of the addressed register are clocked out on the SDO terminal.

The last bit in any serial transfer, D[0], is a parity bit (P) that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transfer should always be an odd number. This ensures that there is always at least one bit set to 1 and one bit set to 0 and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

In addition to the addressable registers, a read-only status register is output on SDO for all register addresses when WR is set to 1. For all serial transfers, the five bits output on SDO will always be the first five bits from the status register. Register data is output on the SDO terminal msb first while STRn is low and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF bit from the status register, is output as soon as STRn goes low.

Registers 12, 13, and 14 contain diagnostic fault indicators and are read only. If the WR bit for these registers is set to 1, then the data input through SDI is ignored and the contents of the status register is clocked out on the SDO terminal then reset as for a normal write. No other action is taken. If the WR bit for these registers is set to 0, then the data input through SDI is ignored and the contents of the addressed register is clocked out on the SDO terminal and the addressed register is reset.

If a framing or parity error is detected, the SE bit is set in the Status register to indicate a data transfer error. This fault condition can be cleared by a subsequent valid serial write or by a power-on-reset.

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Configuration Registers

Nine registers are used to configure the operating parameters of the A4927.

Config 0: Bridge timing settings:

- DT[5:0], a 6-bit integer to set the dead time, t_{DEAD}, in 50 ns increments.

Config 1: Bridge monitor setting:

- OCT[3:0], a 4-bit integer to set the overcurrent threshold voltage, V_{OCT}, in 300 mV increments.
- VT[5:0], a 6-bit integer to set the drain-source threshold voltage, V_{DST}, in 50 mV increments.

Config 2: Bridge monitor setting:

- OCQ, selects the overcurrent qualifier mode, blank or debounce.
- VDQ, selects the VDS qualifier mode, blank or debounce.

Config 3: Bridge monitor setting:

- TVD[5:0], a 6-bit integer to set the VDS fault verification time, t_{VDQ}, in 100 ns increments.

Config 4: Regulator configuration:

- VRG, selects the regulator and gate drive voltage.

Config 5: Sense amplifier setting:

- SAO[3:0], a 4-bit integer to set the sense amplifier offset up between 0 and 2.5 V.
- SAG[2:0], a 3-bit integer to set the sense amplifier gain between 10 and 50 V/V.

Config 6: Gate drive time setting:

- TR[3:0], a 4-bit integer to set the high-side and low-side I_1 time in 50 ns increments.
- TF[3:0], a 4-bit integer to set the high-side and low-side I_1 time in 50 ns increments.

Config 7: Gate drive current setting:

- IR1[3:0] , a 4-bit integer to set the MOSFET turn-on I_1 Current in 4.5 mA increments.
- IF1[3:0] , a 4-bit integer to set the MOSFET turn-off I_1 Current in 5.3 mA increments.

Config 8: Gate drive current setting:

- IR2[3:0] , a 4-bit integer to set the MOSFET turn-on I_2 Current in 4.5 mA increments.
- IF2[3:0] , a 4-bit integer to set the MOSFET turn-off I_2 Current in 5.3 mA increments.

Diagnostic Registers

In addition to the read-only status register, five registers provide detailed diagnostic management and reporting. Two mask register allow individual diagnostics to be disabled and three read-only diagnostic registers provide fault bits for individual diagnostic tests and monitors. If a bit is set to one in the mask register, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated and no fault flags or diagnostic bits will be set. These bits in the diagnostic registers are reset on completion of a successful read of the register.

Mask 0:

Individual bits to disable bootstrap (VBS), temperature warning (TW), and the VGS undervoltage diagnostic monitors (HU and LU).

Mask 1:

Individual bits to disable the voltage regulator (VRO, VRU and VSO) and the VDS overvoltage diagnostic monitors (HO and LO).

Diagnostic 0 (read only):

Individual bits indicating faults detected in VGS diagnostic monitors (HU and LU).

Diagnostic 1 (read only):

Individual bits indicating faults detected in voltage regulator (VRO and VRU) and VDS overvoltage diagnostic monitors (HO and LO).

Diagnostic 2 (read only):

Individual bits indicating faults detected in the VBB supply voltage and overcurrent (VBS and OC).

Control Register

The Control register contains one control bit for each MOSFET and some system function settings:

- DBM, disabled bootstrap management function.
- ESF, defines the action taken when a short is detected. See diagnostics section for details of fault actions.
- HSR and LSR, MOSFET Control bits.

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Status Register

There is one status register in addition to the 16 addressable registers. When any register transfer takes place, the first five bits output on SDO are always the most significant five bits of the status register regardless of whether the addressed register is being read or written. (see serial timing diagram).

The content of the remaining eleven bits will depend on the state of the WR bit input on SDI. When WR is 1, the addressed register will be written and the remaining eleven bits output on SDO will be the least significant ten bits of the status register followed by a parity bit. When WR is 0, the addressed register will be read and the remaining eleven bits will be the contents of the addressed register followed by a parity bit.

The read-only status register provides a summary of the chip status by indicating if any diagnostic monitors have detected a fault. The most significant three bits of the status register (FF, POR, and SE) indicate critical system faults. Bits OT and TW provide indicators for specific individual monitors and the remaining bits are derived from the contents of the three diagnostic registers. The contents and mapping to the diagnostic registers are listed in Table 7.

Table 7: Status Register Mapping

Status Register Bit	Diagnostic	Related Diagnostic Register Bits
FF	Status Flag	None
POR	Power-on-reset	None
SE	Serial Error	None
OT	Overtemperature	None
TW	Temperature warning	None
VS	VBB Monitor	VSO
VR	VREG monitor	VRU, VRO
OC	Overcurrent	OC
VBS	Bootstrap UV	VBS
GSU	VGS UV	HU, LU
DSO	VDS OV	HO, LO

UV = Undervoltage, OV = Overvoltage

The read-only status register provides a summary of the chip status by indicating if any diagnostic monitors have detected a fault. The most significant three bits of the status register (FF, POR, and SE) indicate critical system faults. Bits OT and TW provide indicators for specific individual monitors and the remaining bits are derived from the contents of the three diagnostic registers. The contents and mapping to the diagnostic registers is listed in Table 7.

The first most significant bit in the register is the diagnostic status flag, FF. This is high if any bits in the status register are set. When STRn goes low to start a serial write, the SDO outputs the diagnostic status flag. This allows the main controller to poll the A4927 through the serial interface to determine if a fault has been detected. If no faults have been detected, then the serial transfer may be terminated without generating a serial read fault by ensuring that SCK remains high while STRn is low. When STRn goes high, the transfer will be terminated and SDO will go into its high-impedance state.

The second most significant bit is the POR bit. At power-up or after a power-on-reset, the FF bit and the POR bit are set, indicating to the external controller that a power-on-reset has taken place. All other diagnostic bits are reset and all other registers are returned to their default state. Note that a power-on-reset only occurs when the output of the internal logic regulator rises above its undervoltage threshold. Power-on-reset is not affected by the state of the VBB supply or the VREG regulator output. In general, the VR and VRU bits will also be set following a power-on-reset as the regulators will not have reached their respective rising undervoltage thresholds until after the register reset is completed.

The third bit in the status register is the SE bit, which indicates that the previous serial transfer was not completed successfully.

Bits OT and TW are the fault bits for the two temperature monitors. If one or more of these faults are no longer present, then the corresponding fault bits will be reset following a successful read of the status register. Resetting only affects latched fault bits for faults that are no longer present. For any static faults that are still present, for example overtemperature, the fault flag will remain set after the reset.

The remaining bits, VS, VR, OC, VBS, GSU, and DSO are all derived from the contents of the diagnostic registers. These bits are only cleared when the corresponding contents of the diagnostic are read and reset, they cannot be reset by reading the status register. A fault indicated on any of the related diagnostic register bits will set the corresponding status bit to 1. The related diagnostic register must then be read to determine the exact fault and clear the fault state if the fault condition has cleared.

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SERIAL REGISTER REFERENCE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: Config 0	0	0	0	0	WR					DT5	DT4	DT3	DT2	DT1	DT0	P
						0	0	0	0	1	0	0	0	0	0	
1: Config 1	0	0	0	1	WR	OCT3	OCT2	OCT1	OCT0	VT5	VT4	VT3	VT2	VT1	VT0	P
						1	0	0	1	0	1	1	0	0	0	
2: Config 2	0	0	1	0	WR	OCQ	VDQ									P
						0	0	0	0	0	0	0	0	0	0	
3: Config 3	0	0	1	1	WR					TVD5	TVD4	TVD3	TVD2	TVD1	TVD0	P
						0	0	0	0	0	1	0	0	0	0	
4: Config 4	0	1	0	0	WR				VRG							P
						0	0	0	1	0	0	0	0	0	0	

Config 0

DT[5:0] Dead time.

$t_{DEAD} = n \times 50$ ns

where n is a positive integer defined by DT[5:0],
e.g. for the power-on-reset condition
DT[5:0] = [10 0000] then t_{DEAD} = 1.6 µs.
The range of t_{DEAD} is 100 ns to 3.15 µs.
Selecting a value of 1 or 2 will set the dead time to 100 ns. A value of zero disables the dead time.

Config 1

OCT[3:0] Overcurrent threshold.

$V_{OCT} = (n + 1) \times 300$ mV

where n is a positive integer defined by OCT[3:0]
e.g. for the power-on-reset condition
OCT[3:0] = [1001] then V_{OCT} = 3 V.
The range of V_{OCT} is 0.3 to 4.8 V.

VT[5:0] VDS overvoltage threshold.

$V_{DST} = n \times 50$ mV

where n is a positive integer defined by VT[5:0],
e.g. for the power-on-reset condition
VT[5:0] = [01 1000] then V_{DST} = 1.2 V.
The range of V_{DST} is 0 to 3.15 V.

Config 2

OCQ Overcurrent time qualifier mode.

OCQ	Qualifier	Default
0	Debounce	D
1	Blank	

VDQ VDS Fault qualifier mode.

VDQ	VDS Fault Qualifier	Default
0	Debounce	D
1	Blank	

Config 3

TVD[5:0] VDS verification time.

$t_{VDQ} = n \times 100$ ns

where n is a positive integer defined by TVD[5:0],
e.g. for the power-on-reset condition.
TVD[5:0] = [01 0000] then t_{VDQ} = 1.6 µs.
The range of t_{VDQ} is 0 to 6.3 µs.

Config 4

VRG V_{REG} Voltage Level.

VRG	VREG Voltage	Default
0	8 V	
1	11 V	D

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SERIAL REGISTER REFERENCE (continued)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
5:Config 5	0	1	0	1	WR			SAO3	SAO2	SAO1	SAO0		SAG2	SAG1	SAG0	P
						0	0	1	1	1	1	0	1	0	1	

Config 2

SAO[3:0] Sense Amp Offset.

Where SAO is a positive integer defined by SAO[3:0].

SAO	Offset	Default
0	0 mV	
1	0 mV	
2	100 mV	
3	100 mV	
4	200 mV	
5	300 mV	
6	400 mV	
7	500 mV	
8	750 mV	
9	1.0 V	
10	1.25 V	
11	1.5 V	
12	1.75 V	
13	2.0 V	
14	2.25 V	
15	2.5 V	D

SAG[2:0] Sense Amp Offset.

Where SAG is a positive integer defined by SAG[2:0].

SAG	Gain	Default
0	10	
1	15	
2	20	
3	25	
4	30	
5	35	D
6	40	
7	50	

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SERIAL REGISTER REFERENCE (continued)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6: Config 6	0	1	1	0	WR			TR3	TR2	TR1	TR0	TF3	TF2	TF1	TF0	P
						0	0	0	0	0	1	0	0	0	1	
7: Config 7	0	1	1	1	WR			IR13	IR12	IR11	IR10	IF13	IF12	IF11	IF10	P
						0	0	0	0	0	0	0	0	0	0	
8: Config 8	1	0	0	0	WR			IR23	IR22	IR21	IR20	IF23	IF22	IF21	IF20	P
						0	0	0	0	0	0	0	0	0	0	

Config 6

TR[3:0] MOSFET turn-on t_1 time.

$t_1 = (n + 1) \times 50$ ns

where n is a positive integer defined by TR[3:0],
e.g. if TR[3:0] = [0001] then t_1 = 100 ns.
The range of t_1 is 50 to 800 ns.

TF[3:0] MOSFET turn-off t_1 time.

$t_1 = (n + 1) \times 50$ ns

where n is a positive integer defined by TF[3:0],
e.g. for the power-on-reset condition
TF[3:0] = [0001] then t_1 = 100 ns.
The range of t_1 is 50 to 800 ns.

Config 7

IR1[3:0] MOSFET turn-on I_1 Current.

$I_1 = n \times -4.5$ mA

where n is a positive integer defined by IR1[3:0],
e.g. if IR1[3:0] = [1000] then I_1 = –36 mA
The range of I1 is –4.5 mA to –67.5 mA.
Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

IF1[3:0] MOSFET turn-off I_1 Current.

$I_1 = n \times 5.3$ mA

where n is a positive integer defined by IF1[3:0],
e.g. if IF1[3:0] = [1000] then I_1 = 42.4 mA.
The range of I_1 is 5.3 to 79.5 mA.
Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

Config 8

IR2[3:0] MOSFET turn-on I_2 Current.

$I_2 = n \times -4.5$ mA

where n is a positive integer defined by IR2[3:0],
e.g. if IR2[3:0] = [1000] then I_2 = –36 mA.
The range of I_2 is –4.5 to –67.5 mA.
Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

IF2[3:0] MOSFET turn-off I_2 Current.

$I_2 = n \times 5.3$ mA

where n is a positive integer defined by IF2[3:0],
e.g. if IF2[3:0] = [1000] then I_2 = 42.4 mA.
The range of I_2 is 5.3 to 79.5 mA.
Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

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SERIAL REGISTER REFERENCE (continued)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10: Mask 0	1	0	1	0	WR			VBS	TW					HU	LU	P
						0	0	0	0	0	0	0	0	0	0	
11: Mask 1	1	0	1	1	WR	VRO	VRU	VSO						HO	LO	P
						0	0	0	0	0	0	0	0	0	0	

Mask 0

VBS Bootstrap Undervoltage

TW Temperature Warning

HU High-Side VGS Undervoltage

LU Low-Side VGS Undervoltage

xxx	Fault Mask	Default
0	Fault detection permitted	D
1	Fault detection disabled	

Mask 1

VRO VREG Overvoltage

VRU VREG Undervoltage

VSO VBB Overvoltage

HO High-Side VDS Overvoltage

LO Low-Side VDS Overvoltage

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SERIAL REGISTER REFERENCE (continued)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
12: Diag 0	1	1	0	0	0									HU	LU	P
						0	0	0	0	0	0	0	0	0	0	
13: Diag 1	1	1	0	1	0	VRO	VRU							HO	LO	P
						0	0	0	0	0	0	0	0	0	0	
14: Diag 2	1	1	1	0	0	VSO				VBS				OC		P
						0	0	0	0	0	0	0	0	0	0	
Status	FF	POR	SE		OT	TW	VS			VR		OC	VBS	GSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

Diag 0 (read only)

HU High-Side VGS Undervoltage

LU Low-Side VGS Undervoltage

Diag 1 (read only)

VRO VREG Overvoltage

VRU VREG Undervoltage

HO High-Side VDS Overvoltage

LO Low-Side VDS Overvoltage

Diag 2 (read only)

VSO VBB Overvoltage

VBS Bootstrap Undervoltage

OC Overcurrent on sense amp

xxx	Status
0	No fault detected
1	Fault detected

Status (read only)

FF Diagnostic Register Flag

POR Power-On-Reset

SE Serial Error

OT Overtemperature

TW High Temperature Warning

VS VBB Fault

VR VREG Out of Range

OC Overcurrent

VBS Bootstrap Undervoltage

GSU VGS Undervoltage

DSO VDS Overvoltage

xxx	Status
0	No fault detected
1	Fault detected

Status Register Bit Mapping

Status Register Bit	Related Diagnostic Register Bits
FF	None
POR	None
SE	None
OT	None
TW	None
VS	VSO
VR	VRU, VRO
OC	OC
VBS	VBS
GSU	HU, LU
DSO	HO, LO

U = Undervoltage, O = Overvoltage

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SERIAL REGISTER REFERENCE (continued)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15: Control	1	1	1	1	WR			DBM	ESF					HSR	LSR	P
						0	0	0	1	0	0	0	0	0	0	

Control

DBM

DBM	Bootstrap manager	Default
0	Active	D
1	Disabled	

ESF Enable Stop on Fail.

ESF	Recirculation	Default
0	No stop on fail. Report fault.	
1	Stop on fail. Report fault.	D

HSR High-side gate drive

LSR Low-side gate drive

See Table 2 and Table 3 for control logic operation.

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APPLICATION INFORMATION

Dead-Time Selection

The choice of power MOSFET and external series gate resistance determines the selection of the dead time. The dead time, t_{DEAD}, should be made long enough to ensure that one MOSFET has stopped conducting before the complementary MOSFET starts conducting. This should also account for the tolerance and variation of the MOSFET gate capacitance, the series gate resistance and the on-resistance of the driver in the A4927.

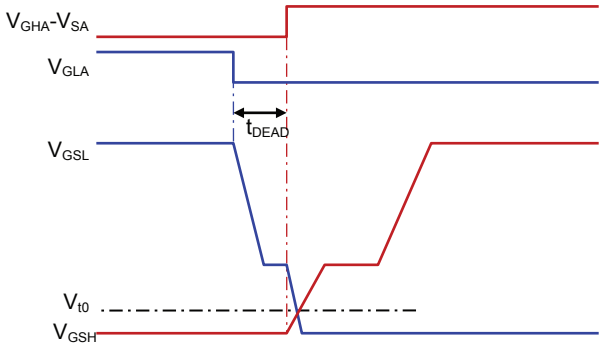

Figure 8: Minimum Dead Time

Figure 8 shows the typical switching characteristics of a pair of complementary MOSFETs. Ideally, one MOSFET should start to turn on just after the other has completely turned off. The point at which a MOSFET starts to conduct is the threshold voltage V_{t0}. The dead time should be long enough to ensure that the gate-source voltage of the MOSFET that is switching off is just below V_{t0} before the gate-source voltage of the MOSFET that is switching on rises to V_{t0}. This will be the minimum theoretical dead time, but in practice the dead time will have to be longer than this to accommodate variations in MOSFET and driver parameters for process variations and overtemperature.

Bootstrap Capacitor Selection

The A4927 requires a bootstrap capacitor C. To simplify this description of the bootstrap capacitor selection criteria, generic naming is used here. So, for example, C_{BOOT}, Q_{BOOT}, and V_{BOOT} refer to the bootstrap capacitor, and Q_{GATE} refers to any of the two associated MOSFETs. C_{BOOT} must be correctly selected to ensure proper operation of the device—too large and time will be wasted charging the capacitor, resulting in a limit on the maximum duty cycle and PWM frequency; too small and there can be a large voltage drop at the time the charge is transferred from C_{BOOT} to the MOSFET gate.

To keep the voltage drop due to charge sharing small, the charge in the bootstrap capacitor, Q_{BOOT}, should be much larger than Q_{GATE}, the charge required by the gate:

$$Q_{BOOT} >> Q_{GATE}$$

A factor of 20 is a reasonable value, so

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20$$

or

$$C_{BOOT} = \frac{Q_{GATE} \times 20}{V_{BOOT}}$$

where V_{BOOT} is the voltage across the bootstrap capacitor.

The voltage drop, ΔV, across the bootstrap capacitor as the MOSFET is being turned on, can be approximated by:

$$\Delta V = \frac{Q_{GATE}}{C_{BOOT}}$$

so for a factor of 20, ΔV will be 5% of V_{BOOT}.

The maximum voltage across the bootstrap capacitor under normal operating conditions is V_{REG} (max). However in some circumstances the voltage may transiently reach a maximum of 18 V, which is the clamp voltage of the Zener diode between the C terminal and the S terminal. In most applications with a good ceramic capacitor, the working voltage can be limited to 16 V.

Bootstrap Charging

It is good practice to ensure the high-side bootstrap capacitor is completely charged before a high-side PWM cycle is requested. The time required to charge the capacitor, t_{CHARGE}, in µs, is approximated by:

$$t_{CHARGE} = \frac{C_{BOOT} \times \Delta V}{100}$$

where C_{BOOT} is the value of the bootstrap capacitor in nF and ΔV is the required voltage of the bootstrap capacitor. At power up and when the drivers have been disabled for a long time, the bootstrap capacitor can be completely discharged. In this case, ΔV can be considered to be the full high-side drive voltage, 12 V. Otherwise, ΔV is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the S terminal is pulled low and current flows from the capacitor connected to the VREG terminal through the internal bootstrap diode circuit to C_{BOOT}.

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VREG Capacitor Selection

The internal reference, V_{REG}, supplies current for the low-side gate-drive circuits and the charging current for the bootstrap capacitors. When a low-side MOSFET is turned on, the gate-drive circuit will provide the high transient current to the gate that is necessary to turn the MOSFET on quickly. This current, which can be several hundred milliamperes, cannot be provided directly by the limited output of the VREG regulator but must be supplied by an external capacitor, C_{REG}, connected between the VREG terminal and GND

The turn-on current for the high-side MOSFET is similar in value but is mainly supplied by the bootstrap capacitor. However, the bootstrap capacitor must then be recharged from C_{REG} through the VREG terminal. Unfortunately, the bootstrap recharge can occur a very short time after the low-side turn on occurs. This means that the value of C_{REG} between VREG and GND should be high enough to minimize the transient voltage drop on VREG for the combination of a low-side MOSFET turn on and a bootstrap capacitor recharge. For block commutation control (trapezoidal drive), where only one high side and one low side are switching during each PWM period, a minimum value of 20 × C_{BOOT} is reasonable. For sinusoidal control schemes, a minimum value of 40 × C_{BOOT} is recommended. As the maximum working voltage of C_{REG} will never exceed V_{REG}, the part's voltage rating can be as low as 15 V. However, it is recommended that a capacitor rated to at least twice the maximum working voltage should be used to reduce any impact operating voltage may have on capacitance value. For best performance, C_{REG} should be ceramic rather than electrolytic. C_{REG} should be mounted as close to the VREG terminal as possible.

Current Sense Amplifier Configuration

Amplifier gain, A_V, and output offset zero point voltage, V_{OOS}, may be set to a range of values by the SAG[2:0] and SAO[3:0] variables respectively as defined in the Current Sense Amplifiers section above. It is important that both values are selected to ensure the absolute voltage at the CSO output, V_{CSO}, remains within the amplifier's dynamic range, V_{CSOUT}, and the dynamic range of any downstream signal processing circuitry. Allowance must be made for both positive and negative current flows within the sense resistor.

With reference to Figure 1, the relationship between phase current I_{PH}, sense resistor value, R_S, and differential amplifier input voltage, V_{ID} is given by:

$$V_{ID} = V_{CSP} - V_{CSM} = I_{PH} \times R_S$$

The current sense amplifier's output voltage on CSxO with respect to the programmed value of output offset on OOS is:

$$V_{CSD} = (V_{CSP} - V_{CSM}) \times A_V$$

The absolute voltage on CSxO with respect to ground is therefore:

$$V_{CSO} = [(V_{CSP} - V_{CSM}) \times A_V] + V_{OOS}$$

If, for example, the following parameter values are assumed:

- R_S = 1 mΩ
- I_{PH} = –20A to +40A
- A_V = 20 (SAG[2:0] = 0b010)
- V_{OOS} = 1 V (SAO[3:0] = 0b1001)

V_{ID} ranges between –20 mV and +40 mV and V_{CSO} between 0.6 V and 1.8 V. V_{CSO} remains within the amplifier dynamic range, V_{CSOUT}, of 0.3 V to 4.8 V. However, if A_V is increased to 50, V_{CSO} attempts to drive to 0 V and 3.0 V, the amplifier dynamic range limits are not complied with, and the amplifier output saturates at its negative limit. This situation could be remedied by reducing A_V to 30 (0.4 V < V_{CSO} < 2.2 V) or increasing V_{OOS} to 1.5 V (0.5 V < V_{CSO} < 3.5 V).

Current Sense Amplifier Output Signals

As defined in Figure 1, the current sense amplifier output signals on the CSO pins are internally referenced to the voltage on the OOS pin. Consequently, the signal voltages on CSO should be measured differentially with respect to OOS (V_{CSD}). Alternatively, the voltages on both CSO (V_{CSO}) and OOS (V_{OOS}) may be measured consecutively with respect to ground and the values subtracted to give the required output signal voltages as V_{CSD} = V_{CSO} – V_{OOS}.

The Input Offset Voltage, V_{IOS}, and the associated drift, ΔV_{IOS}, multiplied by the selected amplifier gain, A_V, represent the offset and offset drift limits that apply to V_{CS}D. The Output Offset Error, E_{VO}, and Output Offset Drift, V_{OOSD}, limits apply directly to V_{OOS}. E_{VO} and V_{OOSD} do not affect current sense output accuracy.

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INPUT/OUTPUT STRUCTURES

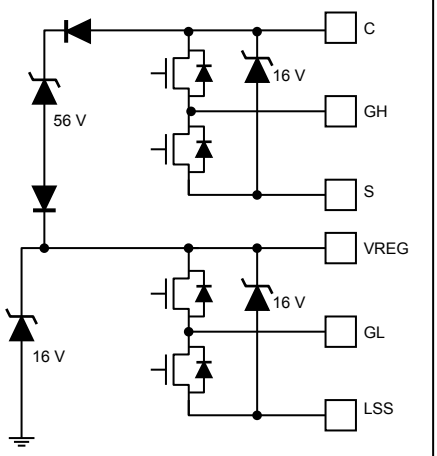

Figure 9a: Gate Drive Outputs

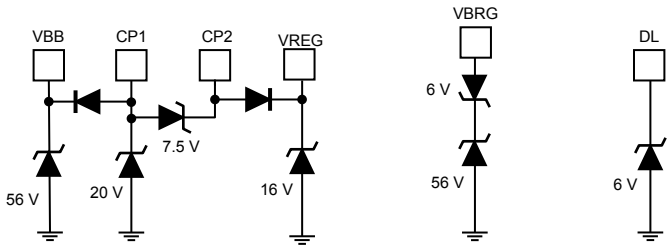

Figure 9b: Supplies

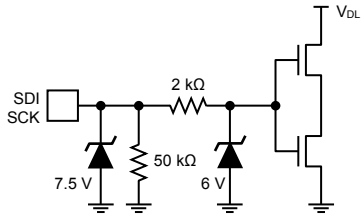

Figure 9c: SDI, SCK Inputs

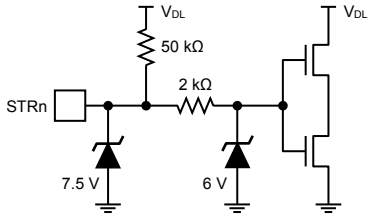

Figure 9d: STRn Inputs

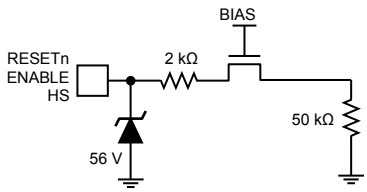

Figure 9e: RESETn, ENABLE, HS Inputs

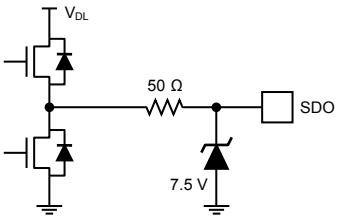

Figure 9f: SDO Output

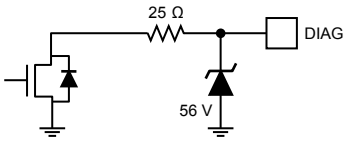

Figure 9g: DIAG Output

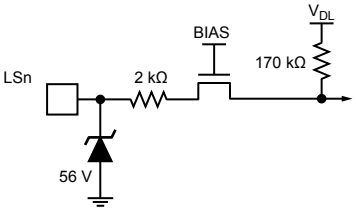

Figure 9h: LSn Input

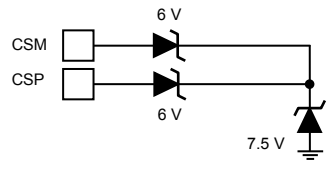

Figure 9i: CSM, CSP Inputs

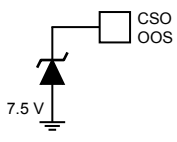

Figure 9j: CSO, OOS Outputs

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LAYOUT RECOMMENDATIONS

Careful consideration must be given to PCB layout when designing high-frequency, fast-switching, high-current circuits:

- The exposed thermal pad should be connected to the GND terminal.
- Minimize stray inductance by using short, wide copper tracks at the drain and source terminals of all power MOSFETs. This includes load lead connections, the input power bus.This will minimize voltages induced by fast switching of large load currents.
- Consider the addition of small (100 nF) ceramic decoupling capacitor across the source and drain of the power MOSFETs to limit fast transient voltage spikes caused by track inductance.
- Keep the gate discharge return connections S and LSS as short as possible. Any inductance on these tracks will cause negative transitions on the corresponding A4927 terminals, which may exceed the absolute maximum ratings. If this is likely, consider the use of clamping diodes to limit the negative excursion on these terminals with respect to the GND terminal.
- Supply decoupling, typically a 100 nF ceramic capacitor, should be connected between VBB and GND as close to the A4927 terminals as possible.
- Supply decoupling should be connected between VREG and GND as close to the A4927 terminals as possible.
- Check the peak voltage excursion of the transients on the LSS terminals with reference to the GND terminal using a close-grounded (“tip & barrel”) probe. If the voltage at any LSS terminal exceeds the absolute maximum in the datasheet, add additional clamping and/or capacitance between the LSS terminal and the GND terminal.
- Gate charge drive paths and gate discharge return paths may carry a large transient current pulse. Therefore, the traces from GH, GL, S, and LSS should be as short as possible to reduce the trace inductance.
- Provide an independent connection between the LSS terminal to the source of the low-side MOSFET in the power bridge. Connection of the LSS terminal directly to the GND terminal is not recommended as this may inject noise into sensitive functions such as the various voltage monitors.
- A low-cost diode can be placed in the connection to VBB to provide reverse battery protection. In reverse battery conditions, it is possible to use the body diodes of the power MOSFETs to clamp the reverse voltage to approximately 4 V. In this case, the additional diode in the VBB connection will prevent damage to the A4927 and the VBRG input will survive the reverse voltage.

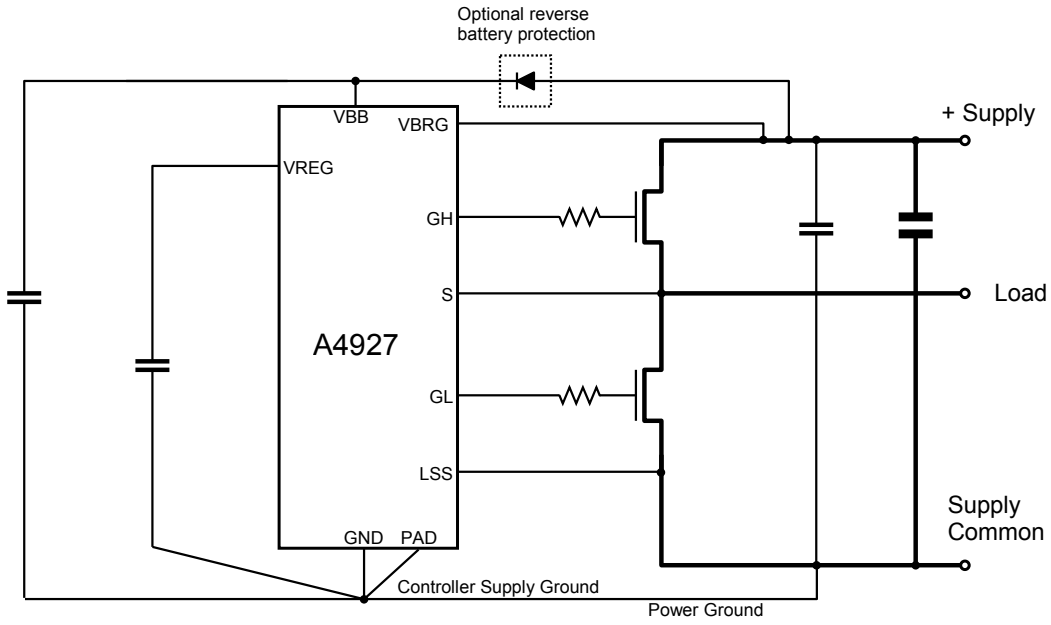

Figure 10: Supply Routing Suggestions

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153ADT)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

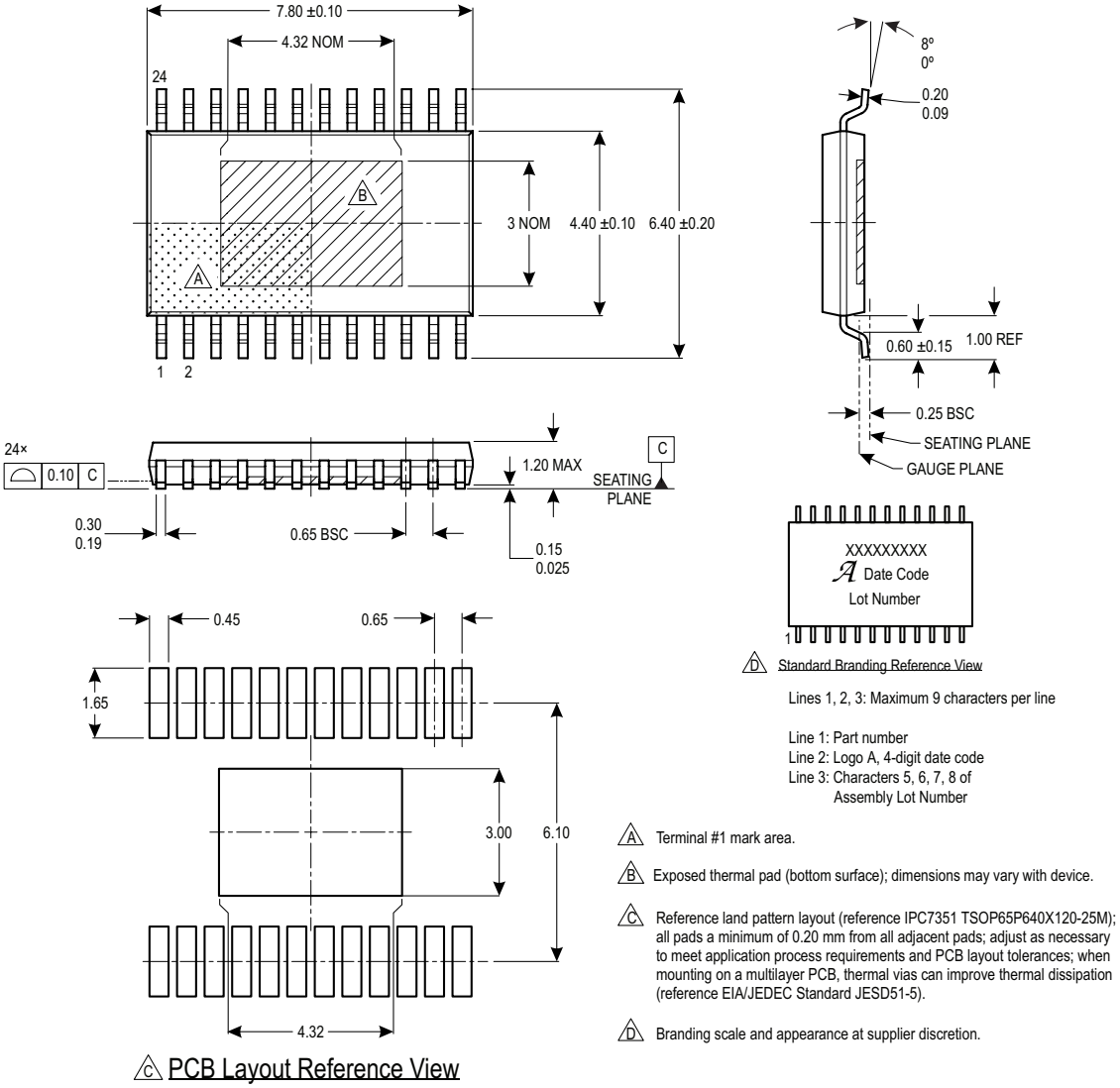

Figure 11: Package LP, 24-Lead TSSOP with Exposed Pad

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Revision History

Number	Date	Description
–	April 11, 2017	Initial release
1	April 24, 2017	Added DIAG Output section and updated Status and Diagnostic Registers section (page 20).
2	February 11, 2019	Minor editorial updates
3	February 28, 2020	Minor editorial updates
4	February 23, 2022	Updated package drawing (page 39)
5	March 13, 2024	Updated product status to Last-Time Buy

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