ARG81401

Adjustable Frequency Buck or Buck-Boost Pre-Regulator with 2 LDOs, Window Watchdog Timer, and NPOR

Discontinued Product

These parts are no longer in production The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: September 30, 2024

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, refer to the A4409KLPTR-T.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

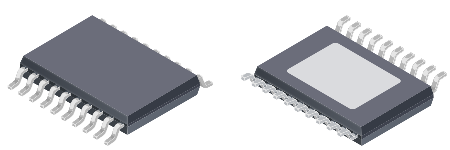
ARG81401

Adjustable Frequency Buck or Buck-Boost Pre-Regulator with 2 LDOs, Window Watchdog Timer, and NPOR

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- V_{IN} operating range from 3 to 36 V, with 40 V maximum
- Buck or buck-boost pre-regulator (VREG)
- Adjustable PWM switching frequency: 250 kHz to 2.4 MHz
- PWM frequency can be synchronized to external clock
- Two internal LDO regulators with foldback short-circuit protection
- Power-on reset (NPOR) with fixed delay of 22.5 ms
- Programmable window watchdog timer with a fixed activation delay of 30 ms
- Active low, watchdog timer enable/disable pin (WD_{ENn})
- Dual bandgaps for increased reliability:
  - □ BG1 for VREG, 3V3, and VCP reference
  - □ BG2 for V5 reference, and VREG, 3V3, and VCP fault detection
- Ignition-enable input (ENBAT)
- Frequency dithering helps reduce EMI/EMC
- Undervoltage protection for all output rails
- Pin-to-pin and pin-to-ground tolerant at every pin
- Thermal shutdown protection
- −40°C to 150°C junction temperature range

PACKAGE: 20-Pin eTSSOP (suffix LP)



Not to scale

DESCRIPTION

The ARG81401 is a power management IC that uses a buck or buck-boost pre-regulator to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage, complete with control, diagnostics, and protections. The output of the pre-regulator supplies a 5 V, 300 mA LDO and a 3.3 V, 200 mA LDO. Designed to supply CAN or microprocessor power supplies in high-temperature environments, the ARG81401 is ideal for underhood applications.

Enable-input to the ARG81401 is compatible to a high-voltage battery level (ENBAT).

Diagnostic outputs from the ARG81401 include a power-on-reset output (NPOR) with a fixed 22.5 ms typical delay. Dual bandgaps, one for regulation and one for fault checking, improve long-term reliability of a system designed around the ARG81401.

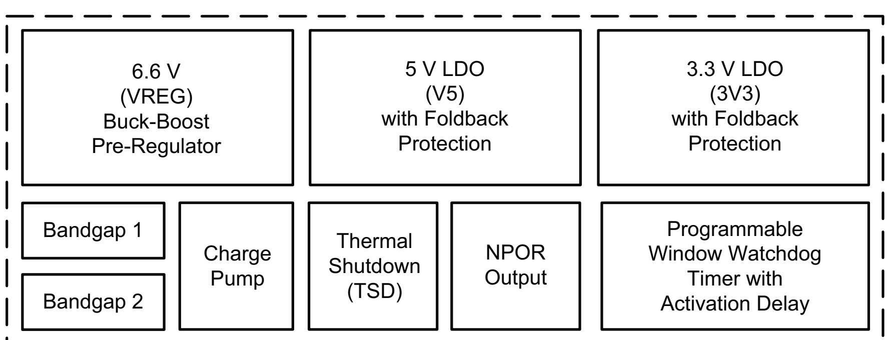
The ARG81401 contains a window watchdog timer that can be programmed to accept a wide range of clock frequencies (WD_{ADJ}). The watchdog timer has a fixed 30 ms activation delay to accommodate processor startup. The watchdog timer has an enable/disable pin (active low, WD_{ENn}) to facilitate initial factory programming or field reflash programming.

Continued on next page...

APPLICATIONS

Provides System Power for (µC/DSP, CAN, sensors, etc.) in Automototive Control Modules, such as:

- Electronic Power Steering (EPS)
- Transmission Control Units (TCU)
- Advanced Braking Systems (ABS)
- Emissions Control Modules
- Other automotive applications



ARG81401 Simplified Block Diagram

DESCRIPTION (continued)

Protection features include dual control loop for pre-regulator rail. In case of a shorted output, all linear regulators feature foldback overcurrent protection. The switching regulator includes pulse-by-pulse current limit, hiccup mode short-circuit protection, LX short-circuit protection, missing asynchronous diode protection, and thermal shutdown.

The ARG81401 is supplied in a low-profile (1.2 mm maximum height), 20-lead eTSSOP package (suffix "LP") with exposed thermal pad.

SELECTION GUIDE

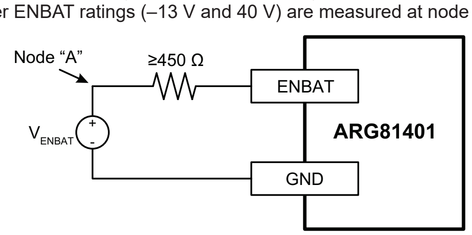
Part Number	Package	Packing [1]	Lead Frame
ARG81401KLPATR	20-pin eTSSOP with thermal pad	4000 pieces per 13-in. reel	100% Matte Tin

[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
VIN pin	V_{IN}		−0.3 to 40	V
ENBAT pin	V_{ENBAT}		−0.3 to 8	V
		With current limiting resistor [3]	−13 to 40	V
	I_{ENBAT}		±75	mA
LX pin	V_{LX}		−0.3 to V_{IN} + 0.3	V
		t < 250 ns	−1.5	V
		t < 50 ns	V_{IN} + 3	V
VCP, CP1, and CP2 pins	V_{VCP}, V_{CPx}		−0.3 to 50	V
All other pins			−0.3 to 7.5	V
Junction Temperature	T_J		−40 to 150	°C
Storage Temperature Range	T_S		−55 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
[3] The higher ENBAT ratings (–13 V and 40 V) are measured at node "A" in the following circuit configuration:



THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [4]	Value	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JC}$	eTSSOP-20 (LP) Package	32	°C/W

[4] Additional thermal information available on the Allegro website.

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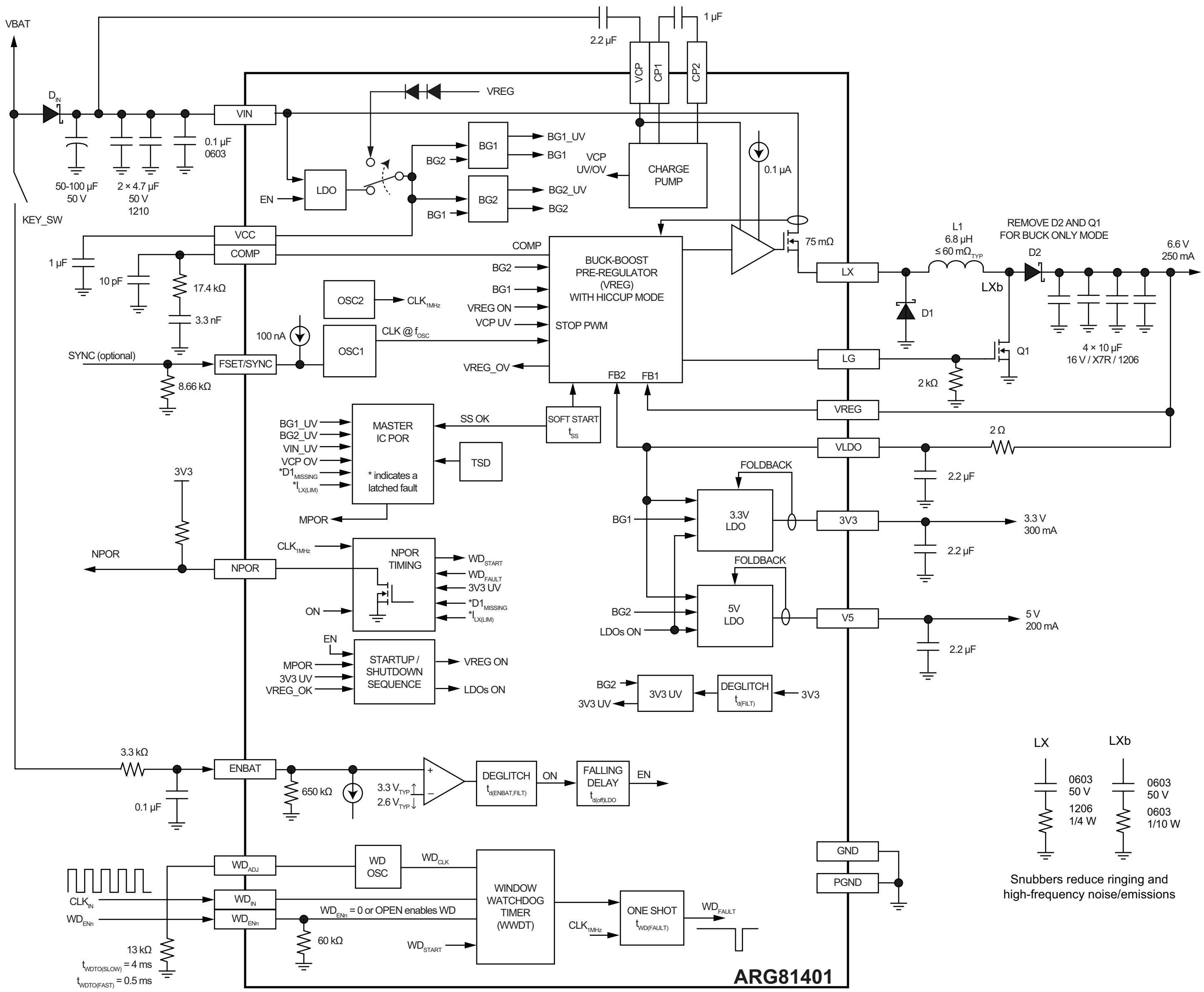

Functional Block Diagram / Typical Schematic

Buck-Boost Mode (f_{OSC} = 2 MHz)

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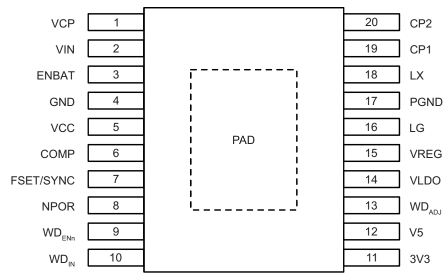
PINOUT DIAGRAM AND TERMINAL LIST



Package LP, 20-Pin eTSSOP Pinout Diagram

Terminal List

Number	Name	Function
1	VCP	Charge pump reservoir capacitor
2	VIN	Input voltage
3	ENBAT	Ignition-enable input from the key/switch through a 1 kΩ resistor
4	GND	Ground
5	VCC	Internal voltage regulator bypass capacitor pin
6	COMP	Error amplifier compensation network pin for the buck-boost pre-regulator
7	FSET/ SYNC	Frequency setting and synchronization input
8	NPOR	Active low, open-drain regulator fault detection output
9	WD_{ENn}	Watchdog enable pin: Open/Low – WD is enabled, High – WD is disabled
10	WD_{IN}	Watchdog refresh input (rising edge triggered) from a microcontroller or DSP
11	3V3	3.3 V, 300 mA regulator output
12	V5	5 V, 200 mA regulator output
13	WD_{ADJ}	The watchdog window time is programmed by connecting R_{ADJ} from this pin to ground
14	VLDO	Input for the LDOs
15	VREG	Feeback pin for VREG output, connect to VREG converter output capacitors
16	LG	Boost gate drive output for the buck-boost pre-regulator
17	PGND	Power ground
18	LX	Switching node for the buck-boost pre-regulator
19	CP1	Charge pump capacitor connection
20	CP2	Charge pump capacitor connection
–	PAD	

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ELECTRICAL CHARACTERISTICS – GENERAL SPECIFICATIONS [1]: Valid at 3 V ≤ V_{IN} ≤ 36 V in buck-boost mode and V_{IN} having first reached $V_{IN(START)}$, –40°C ≤ T_J ≤ 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Operating Input Voltage	V_{IN}	After V_{IN} > $V_{IN(START)}$, V_{ENBAT} ≥ 4 V, buck-boost pre-regulator	3	13.5	36	V
		After V_{IN} > $V_{IN(START)}$, V_{ENBAT} ≥ 4 V, buck pre-regulator	5.5	13.5	36	V
VIN UVLO Start	$V_{IN(START)}$	V_{IN} rising	–	–	5	V
VIN UVLO Stop	$V_{IN(STOP)}$	V_{IN} falling, when in buck-boost mode	–	–	2.9	V
Supply Quiescent Current [1]	I_Q	V_{IN} = 13.5 V, V_{ENBAT} ≥ 4 V, no load on VREG	–	10	–	mA
	$I_{Q(SLEEP)}$	V_{IN} = 13.5 V, V_{ENBAT} ≤ 2 V, no load on VREG	–	–	10	μA
PWM SWITCHING FREQUENCY AND DITHERING						
Switching Frequency	f_{OSC}	R_{FSET} = 8.66 kΩ	1.8	2	2.2	MHz
		R_{FSET} = 57.6 kΩ	343	400	457	kHz
Frequency Divide By 2 Start [2]	$V_{IN(FREQ/2,START)}$	V_{IN} rising, frequency = $f_{OSC}/2$	18	19	20	V
Frequency Divide By 2 Stop [2]	$V_{IN(FREQ/2,STOP)}$	V_{IN} falling, frequency = $f_{OSC}/2$	17	18	19	V
Frequency Dithering	Δf_{OSC}	As a percent of f_{OSC}	–	±12	–	%
VIN Dithering START Threshold	$V_{IN(DITHER,ON)}$	Low range, V_{IN} rising	9	9.5	10	V
		High range, V_{IN} falling	17	18	19	V
VIN Dithering STOP Threshold	$V_{IN(DITHER,OFF)}$	Low range, V_{IN} falling	8.5	9	9.5	V
		High range, V_{IN} rising	18	19	20	V
VIN Dithering Hysteresis	$V_{IN(DITHER,HYS)}$		–	500	–	mV
CHARGE PUMP (VCP)						
Output Voltage	ΔV_{VCP}	V_{VCP} – V_{IN}	4.1	6.6	–	V
Switching Frequency	$f_{SW(CP)}$		–	65	–	kHz
VCC OUTPUT						
Output Voltage	V_{VCC}	V_{VREG} = 6.6 V	–	4.6	–	V
THERMAL PROTECTION						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	160	170	180	°C
Thermal Shutdown Hysteresis [2]	T_{HYS}		–	20	–	°C

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS – BUCK AND BUCK-BOOST PRE-REGULATOR SPECIFICATIONS [1]: Valid at 3 V ≤ V_{IN} ≤ 36 V in buck-boost mode and V_{IN} having first reached $V_{IN(START)}$, –40°C ≤ T_J ≤ 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE SPECIFICATIONS						
Pre-Regulator Output Voltage – VREG Regulating	V_{VREG}	V_{IN} = 13.5 V, ENBAT = 1, 0.1 A ≤ I_{VREG} ≤ 1 A	6.47	6.6	6.7	V
Pre-Regulator Output Voltage – VLDO Regulating	$V_{VLDO(REG)}$	VREG pin open, measured at VLDO pin, V_{IN} = 13.5 V, ENBAT = 1, 0.1 A ≤ I_{VREG} ≤ 1 A	5.88	6	6.12	V
PULSE WIDTH MODULATION (PWM)						
PWM Ramp Offset	$V_{PWMOFFSET}$	V_{COMP} for 0% duty cycle	–	400	–	mV
LX Rising Slew Rate [2]	$SR_{LX(RISE)}$	V_{IN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A	–	1.7	–	V/ns
LX Falling Slew Rate [2]	$SR_{LX(FALL)}$	V_{IN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A	–	1.5	–	V/ns
Buck Minimum On-Time [2]	$t_{ON(BUCK,MIN)}$		–	85	160	ns
Buck Minimum Off-Time	$t_{OFF(BUCK,MIN)}$		–	0	–	ns
Buck Maximum Duty Cycle	$D_{BUCK(MAX)}$		–	100	–	%
Boost Minimum On-Time	$t_{ON(BOOST,MIN)}$		–	60	120	ns
Boost Maximum Duty Cycle	$D_{BOOST(MAX)}$	V_{IN} = 3.5 V	–	70	–	%
COMP to LX Current Gain	$g_{m(POWER)}$		–	4.5	–	A/V
Slope Compensation [2]	S_E	f_{OSC} = 2 MHz	3.84	4.8	5.76	A/μs
		f_{OSC} = 400 kHz	0.76	0.96	1.16	A/μs
INTERNAL MOSFET						
MOSFET On Resistance	$R_{DS(on)}$	V_{IN} = 13.5 V, T_J = –40°C [2], I_{DS} = 0.1 A	–	60	75	mΩ
		V_{IN} = 13.5 V, T_J = 25°C [2], I_{DS} = 0.1 A	–	80	100	mΩ
		V_{IN} = 13.5 V, T_J = 150°C, I_{DS} = 0.1 A	–	140	170	mΩ
MOSFET Leakage	$I_{FET(LEAK)}$	V_{ENBAT} ≤ 2 V, V_{LX} = 0 V, V_{IN} = 13.5 V, −40°C ≤ T_J ≤ 85°C [2]	–	–	10	μA
		V_{ENBAT} ≤ 2 V, V_{LX} = 0 V, V_{IN} = 13.5 V, −40°C ≤ T_J ≤ 125°C [2]	–	–	100	μA
		V_{ENBAT} ≤ 2 V, V_{LX} = 0 V, V_{IN} = 13.5 V, −40°C ≤ T_J ≤ 150°C	–	50	150	μA
ERROR AMPLIFIER						
Open Loop Voltage Gain	A_{VOL}		–	65	–	dB
Transconductance	$g_{m(EA)}$		550	750	950	μA/V
Output Current	$I_{O(EA)}$		–	±75	–	μA
Maximum Output Voltage	$V_{O(EA,MAX)}$		1.3	1.7	2.1	V
Minimum Output Voltage	$V_{O(EA,MIN)}$		–	–	200	mV
COMP Pull-Down Resistance	R_{COMP}	HICCUP = 1 or FAULT = 1 or IC disabled	–	1	–	kΩ

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ELECTRICAL CHARACTERISTICS – BUCK AND BUCK-BOOST PRE-REGULATOR SPECIFICATIONS (continued) [1]: Valid at 3 V ≤ V_{IN} ≤ 36 V in buck-boost mode and V_{IN} having first reached $V_{IN(START)}$, –40°C ≤ T_J ≤ 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
BOOST MOSFET (LG) GATE DRIVER						
LG High Output Voltage	$V_{LG(ON)}$	V_{IN} = 7 V, V_{VREG} = 6.35 V	4.6	–	6.35	V
LG Low Output Voltage	$V_{LG(OFF)}$	V_{IN} = 13.5 V, V_{VREG} = 6.85 V	–	0.2	0.4	V
LG Source Current [1]	$I_{LG(ON)}$	V_{IN} = 7 V, V_{VREG} = 6.35 V, V_{LG} = 1 V	–	–500	–	mA
LG Sink Current [1]	$I_{LG(OFF)}$	V_{IN} = 13.5 V, V_{VREG} = 6.85 V, V_{LG} = 1 V	–	500	–	mA
LG Leakage Current [2]	$I_{LG(LEAK)}$	V_{IN} = 13.5 V, V_{VREG} = 6.6 V, V_{LG} = 3 V	–	–	10	μA
SOFT START						
SS Ramp Time	$t_{SS(ramp)}$		–	1	–	ms
SS PWM Frequency Foldback	$f_{SW(SS)}$	0 V ≤ V_{VREG} ≤ 3.3 V, V_{COMP} = $V_{O(EA,MAX)}$	–	$f_{OSC}/8$	–	–
		0 V ≤ V_{VREG} ≤ 3.3 V	–	$f_{OSC}/2$	–	–
		V_{VREG} > 3.3 V	–	f_{OSC}	–	–
HICCUP MODE						
Hiccup OCP PWM Counts	$t_{HIC(OCP)}$	V_{VREG} < 2.4 V (typical), V_{COMP} = $V_{O(EA,MAX)}$	–	15	–	PWM cycles
		V_{VREG} > 2.4 V (typical), V_{COMP} = $V_{O(EA,MAX)}$	–	60	–	PWM cycles
Hiccup Mode Recovery Time	$t_{rec(HIC)}$	LX switching stops to LX switching starts, during VREG overcurrent	–	2	–	ms
CURRENT PROTECTIONS						
Pulse-by-Pulse Current Limit	I_{LIM}		3.6	4.1	4.6	A
LX Short-Circuit Current Limit	$I_{LIM(LX)}$		6	7	–	A
MISSING ASYNCHRONOUS DIODE (D1) PROTECTION						
Detection Level	$V_{D(OPEN)}$		−1.5	−1.3	−0.9	V
Time Filtering [2]	$t_{D(OPEN)}$		50	–	250	ns

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ELECTRICAL CHARACTERISTICS – LINEAR REGULATOR (LDO) SPECIFICATIONS [1]: Valid at 3 V ≤ V_{IN} ≤ 36 V in buck-boost mode and V_{IN} having first reached $V_{IN(START)}$, –40°C ≤ T_J ≤ 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
V5 LINEAR REGULATOR						
V5 Accuracy and Load Regulation	V_{V5}	10 mA ≤ I_{V5} ≤ 200 mA, V_{VREG} = 5.4 V	4.9	5	5.1	V
V5 Dropout	$V_{V5(DROPOUT)}$	I_{V5} = 200 mA, V_{VLDO} = 4.91 V	4.75	–	–	V
V5 Output Capacitance Range [2]	$C_{V5(OUT)}$		1	–	22	µF
V5 OVERCURRENT PROTECTION						
V5 Current Limit [1]	$I_{V5(LIM)}$	V_{V5} = 5 V	−230	−325	–	mA
V5 Foldback Current [1]	$I_{V5(FB)}$	V_{V5} = 0 V	−80	−120	−160	mA
V5 STARTUP						
V5 Startup Time [2]	$t_{V5(START)}$	C_{V5} ≤ 2.9 µF, load = 25 Ω ±5% (200 mA)	–	0.24	1	ms
3V3 LINEAR REGULATOR						
3V3 Accuracy and Load Regulation	V_{3V3}	10 mA ≤ I_{3V3} ≤ 300 mA, V_{VREG} = 5.4 V	3.23	3.3	3.37	V
3V3 Output Capacitance Range [2]	$C_{3V3(OUT)}$		1	–	22	µF
3V3 OVERCURRENT PROTECTION						
3V3 Current Limit [1]	$I_{3V3(LIM)}$	V_{3V3} = 3.3 V	−345	−485	–	mA
3V3 Foldback Current [1]	$I_{3V3(FB)}$	V_{3V3} = 0 V	−120	−165	−210	mA
3V3 STARTUP						
3V3 Startup Time [2]	$t_{3V3(START)}$	C_{3V3} ≤ 2.9 µF, load = 15 Ω ±5% (220 mA)	–	0.24	1	ms

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ELECTRICAL CHARACTERISTICS – CONTROL INPUTS [1]: Valid at 3 V ≤ V_{IN} ≤ 36 V in buck-boost mode and V_{IN} having first reached $V_{IN(START)}$, –40°C ≤ T_J ≤ 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
IGNITION-ENABLE (ENBAT) INPUT						
ENBAT Thresholds	$V_{ENBAT(H)}$	V_{ENBAT} rising	2.8	3.2	3.5	V
	$V_{ENBAT(L)}$	V_{ENBAT} falling	2.1	2.5	2.8	V
ENBAT Hysteresis	$V_{ENBAT(HYS)}$	$V_{ENBAT(H)} – V_{ENBAT(L)}$	–	700	–	mV
ENBAT Bias Current [1]	$I_{IB(ENBAT)}$	T_J = 25°C [2], V_{ENBAT} = 3.51 V	–	28	45	μA
		T_J = 150°C, V_{ENBAT} = 3.51 V	–	35	60	μA
ENBAT Resistance	R_{ENBAT}		–	650	–	kΩ
ENBAT DEGLITCH						
Enable Filter/Deglitch Time	$t_{d(ENBAT,FILT)}$		10	15	20	μs
ENBAT SHUTDOWN DELAY						
LDO Shutdown Delay	$t_{d(off)LDO}$	Measure $t_{d(off)LDO}$ from the falling edge of ENBAT to the time when all LDOs begin to decay	15	50	100	μs
FSET/SYNC INPUT						
FSET/SYNC Pin Voltage	$V_{FSET/SYNC}$	No external SYNC signal	–	800	–	mV
FSET/SYNC Open Circuit (Undercurrent) Detection Time	$t_{FSET/SYNC(UC)}$	PWM switching frequency becomes 900 kHz upon detection	–	3	–	μs
FSET/SYNC Short-Circuit (Overcurrent) Detection Time	$t_{FSET/SYNC(OC)}$	PWM switching frequency becomes 900 kHz disabled upon detection	–	3	–	μs
Sync. High Threshold	$V_{SYNC(H)}$	V_{SYNC} rising	–	–	2	V
Sync. Low Threshold	$V_{SYNC(L)}$	V_{SYNC} falling	0.5	–	–	V
Sync. Input Duty Cycle	D_{SYNC}		–	–	80	%
Sync. Input Pulse Width	$t_{PW(SYNC)}$		200	–	–	ns
Sync. Input Transition Times [2]	$t_{T(SYNC)}$		–	10	15	ns

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ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS [1]: Valid at 3 V ≤ V_{IN} ≤ 36 V in buck-boost mode and V_{IN} having first reached $V_{IN(START)}$, –40°C ≤ T_J ≤ 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NPOR UNDERVOLTAGE PROTECTION THRESHOLDS						
3V3 Undervoltage Thresholds	$V_{3V3(UV,H)}$	V_{3V3} rising	–	3.1	–	V
	$V_{3V3(UV,L)}$	V_{3V3} falling	2.97	3.07	3.17	V
3V3 Undervoltage Hysteresis	$V_{3V3(UV,HYS)}$	$V_{3V3(UV,H)} – V_{3V3(UV,L)}$	–	30	–	mV
NPOR TURN-ON AND TURN-OFF DELAYS						
NPOR Turn-On Delay	$t_{d(on)NPOR}$		18	22.5	27	ms
NPOR Turn-Off Propagation Delay	$t_{d(off)NPOR}$	ENBAT low to NPOR low, measured after ENBAT deglitch time $t_{d(ENBAT,FILT)}$	–	–	3	μs
NPOR OUTPUT VOLTAGES						
NPOR Output Low Voltage	$V_{NPOR(L)}$	ENBAT high, V_{IN} ≥ 2.5 V, I_{NPOR} = 4 mA	–	150	400	mV
		ENBAT high, V_{IN} = 1.5 V, I_{NPOR} = 2 mA	–	–	800	mV
NPOR Leakage Current [1]	$I_{NPOR(LEAK)}$	V_{NPOR} = 3.3 V	–	–	2	μA
NPOR UNDERVOLTAGE FILTERING/DEGLITCH						
NPOR Undervoltage Filter/Deglitch Times	$t_{d(NPOR,FILT)}$	Applies to undervoltage of the 3V3 voltage	10	15	20	μs

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ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS (continued) [1]: Valid at 3 V ≤ V_{IN} ≤ 36 V in buck-boost mode and V_{IN} having first reached $V_{IN(START)}$, –40°C ≤ T_J ≤ 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VREG, VCP, AND BG THRESHOLDS						
VREG Overvoltage Threshold	$V_{VREG(OV,H)}$	V_{VREG} rising, PWM disabled	6.8	6.93	7.18	V
VREG Overvoltage Hysteresis	$V_{VREG(OV,HYS)}$		–	100	–	mV
VREG Undervoltage Thresholds	$V_{VREG(UV,H)}$	V_{VREG} rising	4.16	4.41	4.64	V
	$V_{VREG(UV,L)}$	V_{VREG} falling	–	4.3	–	V
VREG Undervoltage Hysteresis	$V_{VREG(UV,HYS)}$	$V_{VREG(UV,H)} – V_{VREG(UV,L)}$	–	100	–	mV
VCP Overvoltage Threshold	$V_{VCP(OV,H)}$	V_{VCP} rising, PWM disabled	11	12.5	14	V
VCP Undervoltage Thresholds	$V_{VCP(UV,H)}$	V_{VCP} rising, PWM enabled	3	3.2	3.4	V
	$V_{VCP(UV,L)}$	V_{VCP} falling, PWM disabled	–	2.7	–	V
VCP Undervoltage Hysteresis	$V_{VCP(UV,HYS)}$	$V_{VCP(UV,H)} – V_{VCP(UV,L)}$	–	500	–	mV
BG1 and BG2 Undervoltage Thresholds [2]	$V_{BGx(UV)}$	BG1 or BG2 rising	1	1.05	1.1	V
UNDERVOLTAGE AND OVERVOLTAGE FILTERING/DEGLITCH						
Undervoltage Filter/Deglitch Time	$t_{d(UV,FILT)}$		10	15	20	µs
Overvoltage Response Time [2]	$t_{d(OV,FILT)}$		–	1	–	µs

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS – WINDOW WATCHDOG TIMER (WWDT) [1]: Valid at 3 V ≤ V_{IN} ≤ 36 V in buck-boost mode and V_{IN} having first reached $V_{IN(START)}$, –40°C ≤ T_J ≤ 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
WD ENABLE INPUT (WD_{ENn})						
WD_{ENn} Voltage Thresholds	$V_{WDENn(L)}$	V_{WDENn} falling, WWDT enabled	0.8	–	–	V
	$V_{WDENn(H)}$	V_{WDENn} rising, WWDT disabled	–	–	2	V
WD_{ENn} Input Resistance	R_{WDENn}		–	60	–	kΩ
WD_{IN} VOLTAGE THRESHOLDS AND CURRENT						
WD_{IN} Input Voltage Thresholds	$V_{WDIN(L)}$	V_{WDIN} falling, WD_{ADJ} pulled low by R_{ADJ}	0.8	–	–	V
	$V_{WDIN(H)}$	V_{WDIN} rising, WD_{ADJ} charging	–	–	2	V
WD_{IN} Input Current [1]	I_{WDIN}	V_{WDIN} = 5 V	−10	±1	10	μA
WD_{IN} TIMING SPECIFICATIONS						
WD_{IN} Frequency	f_{WDIN}		–	–	750	Hz
WD_{IN} Duty Cycle	D_{WDIN}		20	50	80	%
Watchdog Activation Delay	$t_{WD(START)}$		24	30	36	ms
WD PROGRAMMING						
WD Timeout FAST Range [2]	$t_{WDTO(FAST)}$		0.5	–	12.5	ms
WD Timeout SLOW Range [2]	$t_{WDTO(SLOW)}$		4	–	100	ms
WD Timeout, FAST Clock	$t_{WDTO(FASTCLK)}$	R_{ADJ} = 13 kΩ	0.4	0.5	0.6	ms
		R_{ADJ} = 324 kΩ	10	12.5	15	ms
WD Timeout, SLOW Clock	$t_{WDTO(SLOWCLK)}$	R_{ADJ} = 13 kΩ	3.2	4	4.8	ms
		R_{ADJ} = 324 kΩ	80	100	120	ms
WD ONE-SHOT TIME						
WD Pulse Time After WD Fault	$t_{WD(FAULT)}$		1.6	2	2.4	ms

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.

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Table 1: Startup and Shutdown Logic (signal names consistent with Functional Block Diagram)

ARG81401 Status Signals				Supply Control (0=OFF, 1=ON)		ARG81401 MODE
ENBAT	MPOR	VREG UV	3V3_UV	VREG ON	LDOs ON	
X	1	X	X	0	0	RESET
0	0	1	1	0	0	OFF
1	0	1	1	1	0	STARTUP
1	0	0	1	1	0	↓
1	0	0	1	1	1	↓
1	0	0	0	1	1	RUN
0	0	0	0	1	1	50 µs DELAY
0	0	0	0	1	0	SHUTDOWN
0	0	0	1	1	0	↓
0	0	0	1	0	0	↓
0	0	1	1	0	0	OFF

TIME

X = DON'T CARE

MPOR = BG1_UV or BG2_UV or VIN_UV or TSD or VCP_UV or VCP_OV or $D1_{MISSING}$ (latched) + $I_{LIM(LX)}$ (latched)

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Table 2: Summary of Fault Mode Operation

FAULT TYPE and CONDITION	ARG81401 RESPONSE TO FAULT	NPOR	LATCHED FAULT?	RESET METHOD or CORRECTION
3V3 undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	Low	NO	Decrease the load
3V3 overcurrent	Foldback current limit will reduce the output voltage	Transitions low if 3V3 < $V_{3V3(UV,L)}$	NO	Decrease the load
V5 undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	Not affected	NO	Decrease the load
V5 overcurrent	Foldback current limit will reduce the output voltage	Not affected	NO	Decrease the load
VREG pin open circuit	VLDO pin will take over regulation, power dissipation in IC will increase	Not affected	NO	Connect the VREG pin
VREG shorted to ground, V_{VREG} < 2.4 V, $V_{COMP} \neq E_{AVO(MAX)}$	Continue to PWM but turn off LX when the high-side MOSFET current exceeds I_{LIM}	Depends on 3V3	NO	Remove the short circuit
VREG overcurrent, V_{VREG} < 2.4 V, $V_{COMP} = E_{AVO(MAX)}$	Enters hiccup mode after 15 OCP faults	Depends on 3V3	NO	Decrease the load
VREG overcurrent, V_{VREG} > 2.4 V, $V_{COMP} = E_{AVO(MAX)}$	Enters hiccup mode after 60 OCP faults	Depends on 3V3	NO	Decrease the load
VREG asynchronous diode (D1) missing	Results in an MPOR after 1 detection, so all regulators are off	Low	YES	Place D1 then cycle ENBAT or VIN
Asynchronous diode (D1) short circuited or LX shorted to ground	Results in an MPOR after the high-side MOSFET current exceeds $I_{LIM,LX}$, so all regulators are off	Low	YES	Remove the short then cycle ENBAT or VIN
FSET/SYNC pin open circuit	Oscillator frequency becomes default frequency 900 kHz	Not affected	NO	Connect the FSET/SYNC pin
FSET/SYNC pin shorted to ground	Oscillator frequency becomes default frequency 900 kHz	Not affected	NO	Remove the short circuit
Charge pump (VCP) overvoltage	Results in an MPOR, so all regulators are shut off	Depends on 3V3	NO	Check VCP/CP1/CP2 pins and components, then cycle ENBAT or VIN
Charge pump (VCP) undervoltage	Results in an MPOR, so all regulators are shut off	Depends on 3V3	NO	Check VCP/CP1/CP2 pins and components
VCP pin open circuit	Results in VCP_UV and an MPOR, so all regulators are shut off	Depends on 3V3	NO	Connect the VCP pin
VCP pin shorted to ground	Results in high current from the charge pump and (intentional) fusing of an internal trace. Also results in an MPOR, so all regulators are shut off	Depends on 3V3	NO	Remove the short circuit and replace the ARG81401
COMP shorted high	$VREG_{OV,H}$ will trip, so all regulators are shut off	Depends on 3V3	YES	Remove the high level from the COMP pin then cycle ENBAT or VIN
CP1 or CP2 pin open circuit	Results in VCP_UV and an MPOR, so all regulators are shut off	Depends on 3V3	NO	Connect the CP1 or CP2 pins
CP1 pin shorted to ground	Results in VCP_UV and an MPOR, so all regulators are shut off	Depends on 3V3	NO	Remove the short circuit

Continued on next page...

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Table 2: Summary of Fault Mode Operation (continued)

FAULT TYPE and CONDITION	ARG81401 RESPONSE TO FAULT	NPOR	LATCHED FAULT?	RESET METHOD or CORRECTION
CP2 pin shorted to ground	Results in high current from the charge pump and (intentional) fusing of an internal trace. Also results in an MPOR, so all regulators are shut off.	Depends on 3V3	NO	Remove the short circuit and replace the ARG81401
BG1 or BG2 undervoltage	Results in an MPOR, so all regulators are shut off	Depends on 3V3	NO	Raise VIN or wait for BGs to power up
BG1 or BG2 overvoltage	If BG1 is too high, 3V3 will appear to be overvoltage, because BG2 is good. If BG2 is too high, 3V3 will appear to be undervoltage, because BG1 is good.	Low	NO	Replace the ARG81401
VIN undervoltage	Results in an MPOR, so all regulators are shut off	Depends on 3V3	NO	Raise VIN
Thermal shutdown	Results in an MPOR, so all regulators are shut off	Depends on 3V3	NO	Let the ARG81401 cool
WD_{ADJ} pin shorted to ground or open circuit	A WD_{ADJ} fault only affects the NPOR output. The remainder of the ARG81401 operates normally.	Low	NO	Remove the short circuit or connect the pin

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TIMING DIAGRAMS
(not to scale)

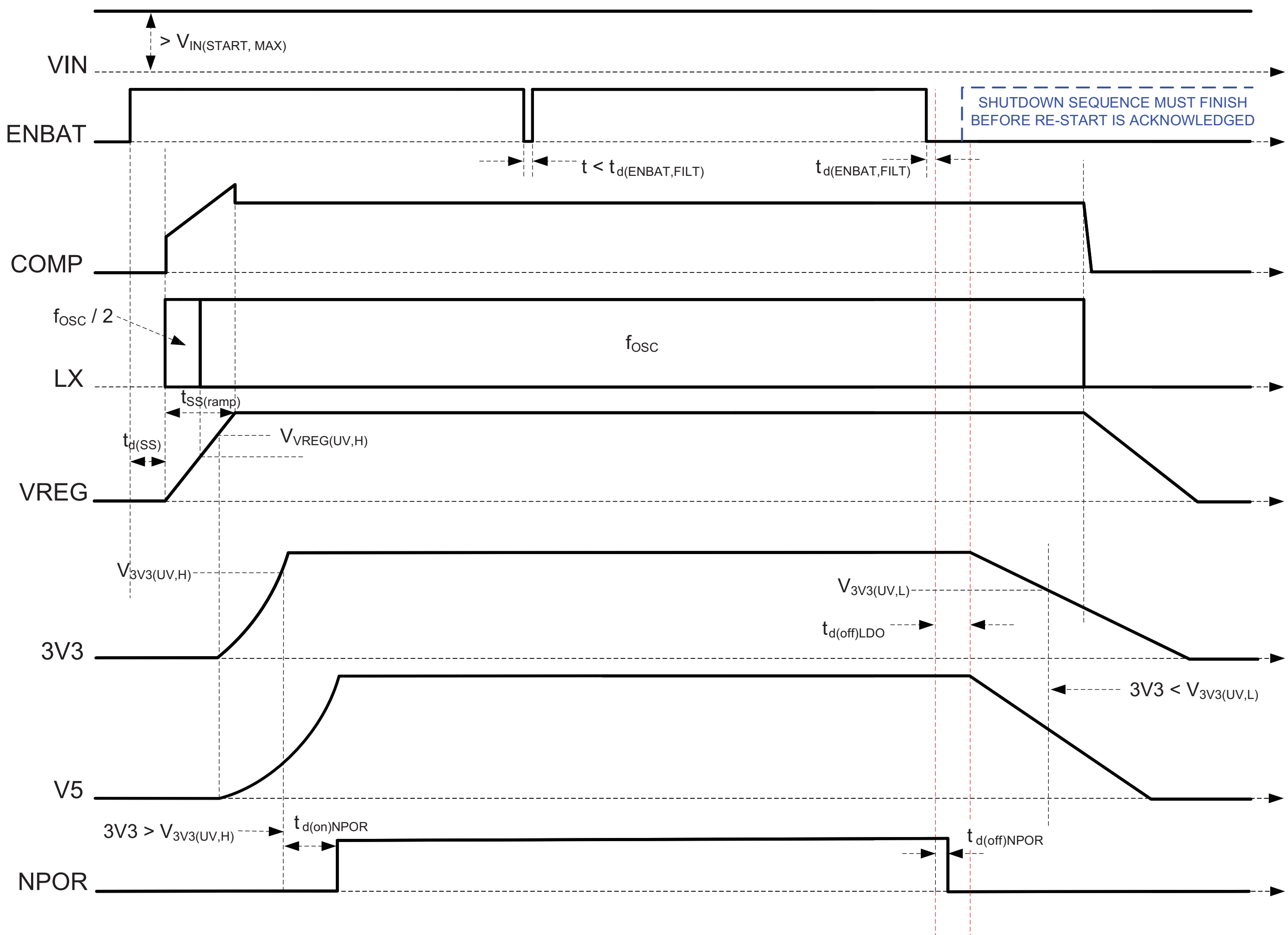

Figure 1: Startup and Shutdown Sequence

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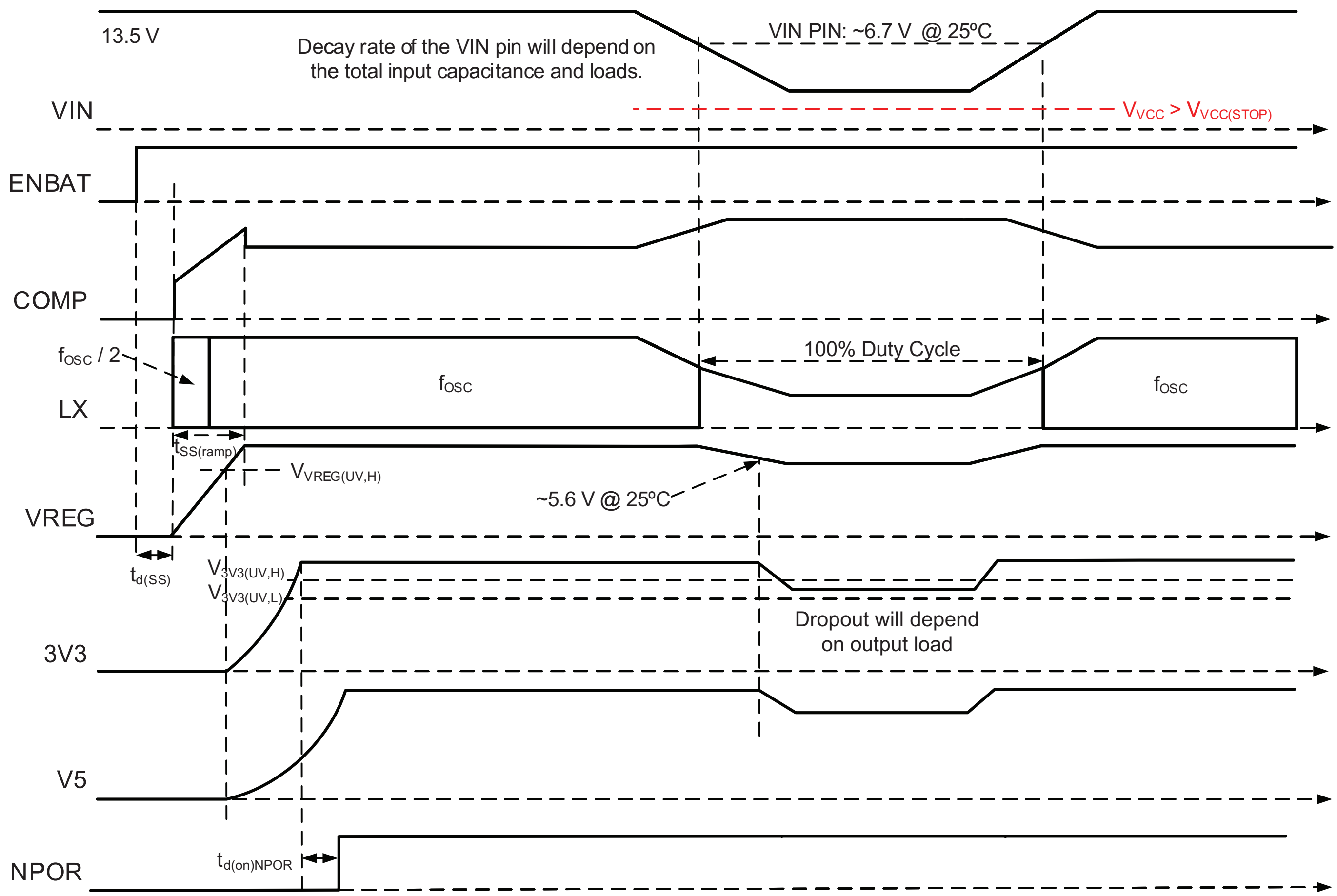

Figure 2: Input Undervoltage Timing, when VIN > $V_{IN(STOP)}$

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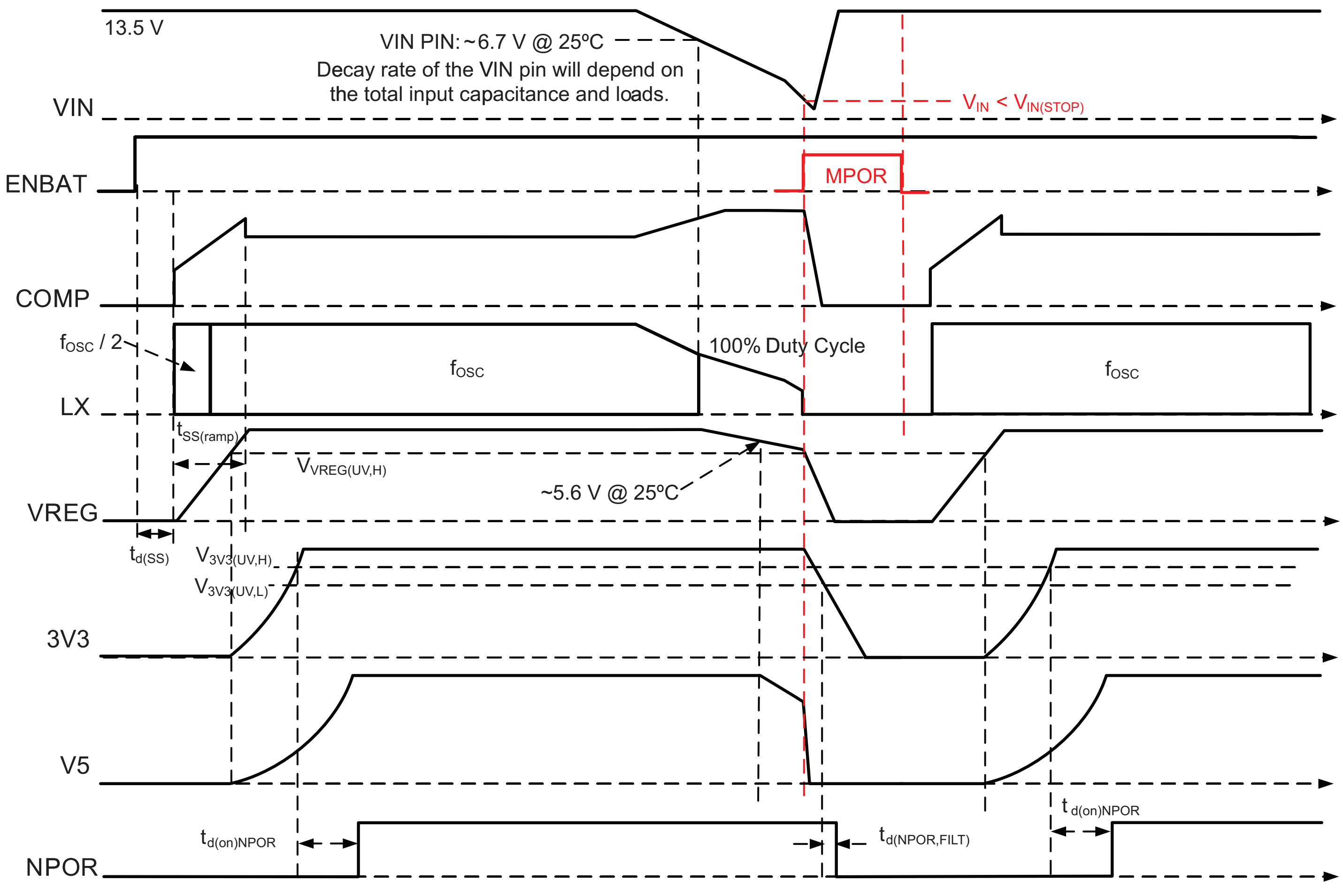

Figure 3: Input Undervoltage Timing, when VIN < $V_{IN(STOP)}$

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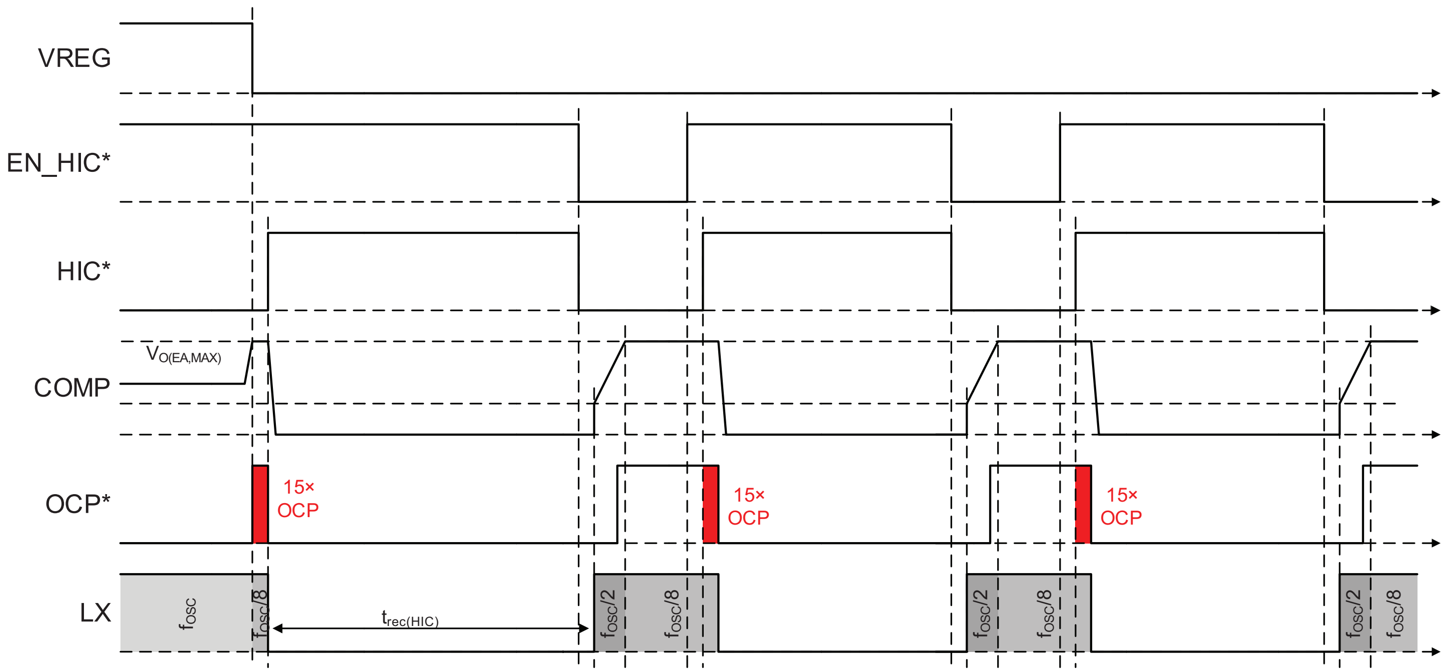

Figure 4: VREG Short Circuit to Ground Hiccup Operation

*** Signal is internal to ARG81401**

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DESIGN AND COMPONENT SELECTION

Setting Up the Pre-Regulator

This section describes component selection for the ARG81401 pre-regulator, including charge-pump circuit, inductor, diodes, boost MOSFET, and input and output capacitors. This section also covers loop compensation.

Charge Pump Capacitors

The charge pump requires two capacitors: a 2.2 µF capacitor connected from pin VCP to pin VIN, and a 1 µF capacitor connected between pins CP1 and CP2. These capacitors should be high quality ceramic capacitors, such as X7R, with a voltage rating of at least 50 V.

PWM Switching Frequency

When the PWM switching frequency is chosen, the designer should be aware of the minimum controllable on-time, $t_{ON(MIN)}$, of the ARG81401. If the system's required on-time is less than the ARG81401's minimum controllable on-time, then switch-node jitter will occur and the output voltage will have increased ripple or oscillations.

The PWM switching frequency should be calculated using equation 1, where $t_{ON(BUCK,MIN)}$ is the minimum controllable on-time of the ARG81401 (160 ns typical), and $V_{IN(MAX)}$ is the maximum required operational input voltage (not the peak surge voltage).

$$f_{OSC} < \frac{6.6\text{ V}}{t_{ON(BUCK,MIN)} \times V_{IN(MAX)}} \tag{1}$$

If the ARG81401's synchronization function is used, then the base oscillator frequency should be chosen such that jitter will not result at the maximum synchronized switching frequency according to equation 1.

R_{FSET} can be estimated using equation 2 below.

$$R_{FSET} = \frac{1}{0.0455 \times f_{OSC}} - 1.98\ (\text{k}\Omega) \tag{2}$$

where f_{OSC} is in MHz.

Pre-Regulator Output Inductor (L1)

For peak current mode control, it is well known that the system will become unstable when the duty cycle is above 50% without adequate slope compensation (S_E). However, the slope compensation in the ARG81401 is a fixed value based on the oscillator frequency (f_{OSC}). Therefore, it is important to calculate an inductor value so the falling slope of the inductor current (S_F) will work well with the ARG81401's slope compensation.

Equation 3 can be used to calculate a range of values for the output inductor for buck or buck-boost.

$$\frac{(VREG + V_F)}{S_E} \leq L1 \leq \frac{2 \times (VREG + V_F)}{S_E} \tag{3}$$

where V_F is the asynchronous diode forward voltage, f_{OSC} is the programmed oscillator frequency in kHz, and S_E slope compensation can be calculated from equation 4 and is in amperes per microsecond (A/µs). The resultant inductor value will be in microhenries (µH).

$$S_E = 0.0024 \times f_{OSC} \tag{4}$$

If equation 3 yields an inductor value that is not a standard value, then the next closest available value should be used. The final inductor value should allow for 10%-20% of initial tolerance and 20%-30% of inductor saturation.

The inductor should not saturate given the peak operating current during overload. Equation 5 calculates the current. In equation 5, $V_{IN(MAX)}$ is the maximum continuous input voltage, such as 16 V, and V_F is the asynchronous diodes forward voltage.

$$I_{PEAK} = 4.6\text{ A} - \frac{S_E \times (VREG + V_F)}{0.9 \times f_{OSC} \times (V_{IN(MAX)} + V_F)} \tag{5}$$

After an inductor is chosen, it should be tested during output overload and short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator is not damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

Inductor ripple current can be calculated using equation 6 for buck mode and equation 7 for buck-boost mode.

$$\Delta I_{L1} = \frac{(V_{IN} - VREG) \times VREG}{f_{SW} \times L1 \times V_{IN}} \tag{6}$$

$$\Delta I_{B/B} = \frac{V_{IN} \times D_{BOOST}}{f_{SW} \times L1} \tag{7}$$

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Pre-Regulator Output Capacitors

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage, and they store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{OUT}) is a function of the output capacitors parameters: C_O, ESR_{CO}, ESL_{CO}.

$$\Delta V_{OUT} = \Delta I_{L1} \times ESR_{CO} + \frac{V_{IN} - VREG}{L1} \times ESL_{CO} + \frac{\Delta I_{L1}}{8 \times f_{SW} \times C_O} \tag{8}$$

The type of output capacitors will determine which terms of equation 8 are dominant. For ceramic output capacitors, the ESR_{CO} and ESL_{CO} are virtually zero, so the output voltage ripple will be dominated by the third term of equation 8.

$$\Delta VREG = \frac{\Delta I_{L1}}{8 \times f_{SW} \times C_O} \tag{9}$$

To reduce the voltage ripple of a design using ceramic output capacitors, simply increase the total capacitance, reduce the inductor current ripple (i.e. increase the inductor value), or increase the switching frequency.

The transient response of the regulator depends on the number and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (di/dt), the output voltage will change by the amount

$$\Delta VREG = \Delta I_{LOAD} \times ESR_{CO} + \frac{di}{dt} ESL_{CO} \tag{10}$$

After the load transient occurs, the output voltage will deviate from its nominal value for a short time. This time will depend on the system bandwidth, the output inductor value, and output capacitance. Eventually, the error amplifier will bring the output voltage back to its nominal value.

The speed at which the error amplifier will bring the output voltage back to its setpoint will depend mainly on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, it may be more difficult to obtain acceptable gain and phase margins in a a higher bandwidth system. Selection of the compensation components (R_Z, C_Z, C_P) are discussed in more detail in the Compensation Components section of this datasheet.

Ceramic Input Capacitors

The ceramic input capacitor or capacitors must limit the voltage ripple at the VIN pin to a relatively low voltage during maximum load. Equation 11 can be used to calculate the minimum input capacitance,

$$C_{IN} \geq \frac{I_{VREG(MAX)} \times 0.25}{0.9 \times f_{SW} \times 50\ \text{mV}} \tag{11}$$

where $I_{VREG(MAX)}$ is the maximum current from the pre-regulator,

$$I_{VREG(MAX)} \equiv I_{LINEAR} + I_{AUX} + 20\ \text{mA} \tag{12}$$

where I_{LINEAR} is the sum of all internal linear regulators output currents, and I_{AUX} is any extra current drawn from the VREG output to power other devices external to the ARG81401.

A good design should consider the dc-bias effect on a ceramic capacitor— as the applied voltage approaches the rated value, the capacitance value decreases. An X7R type capacitor should be the primary choice due to its stability with both dc bias and temperature variation. For all ceramic capacitors, the dc-bias effect is even more pronounced on smaller case sizes, so a good design will use the largest affordable case size.

Also for improved noise performance, it is recommended to add smaller-sized capacitors close to the ARG81401 VIN pin and the D1 anode. Use a 0.1 µF, 0603 capacitor.

Buck-Boost Asynchronous Diode (D1)

The highest peak current in the asynchronous diode (D1) occurs during overload and is limited by the ARG81401. Equation 5 can be used to calculate this current.

The highest average current in the asynchronous diode occurs when V_{IN} is at its maximum, D_{BOOST} = 0%, and D_{BUCK} = minimum (10%),

$$I_{AVG} = 0.9 \times I_{VREG(MAX)} \tag{13}$$

where $I_{VREG(MAX)}$ is calculated using equation 12.

Boost MOSFET (Q1)

The RMS current in the boost MOSFET (Q1) occurs when V_{IN} is at its minimum and both the buck and boost operate at their maximum duty cycles (approximately 64% and 58%, respectively),

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$$I_{Q1(RMS)} = \sqrt{D_{BOOST} \times \left[\left(I_{PEAK} - \frac{\Delta I_{B/B}}{2}\right)^2 + \frac{\Delta I_{B/B}}{12}\right]} \quad (14)$$

where I_{PEAK} and $\Delta I_{B/B}$ are derived using equations 5 and 7, respectively.

Boost Diode (D2)

In buck mode, this diode will simply conduct the output current. However, in buck-boost mode, the peak currents in this diode may increase significantly. The ARG81401 limits the peak current to the value calculated using equation 5. The average current is simply the output current.

Pre-Regulator Compensation Components (R_Z, C_Z, C_P)

Although the ARG81401 can operate in buck-boost mode at low input voltages, it can still be considered a buck converter when looking at the control loop. The following equations can be used to calculate the compensation components.

First, the target crossover frequency for the final system must be selected. Although the ARG81401 can switch at over 2 MHz, the crossover will be governed by the required phase margin. Since a type II compensation scheme is used, there are limits to the amount of phase that can be added. Therefore, a crossover frequency, f_C, of around 40 kHz is selected. The total system phase will drop off at higher crossover frequencies. The R_Z selection is based on the gain required at the crossover frequency, and can be calculated by the following simplified equation:

$$R_Z = \frac{13.36 \times \pi \times f_C \times C_O}{g_{m(POWER)} \times g_{m(EA)}} \quad (15)$$

The series capacitor, C_Z, along with the resistor, R_Z, set the location of the compensation zero. This zero should be placed no lower than ¼ of the crossover frequency and should be kept to minimum value. Equation 18 can be used to estimate this capacitor value.

$$C_Z > \frac{4}{2\pi \times R_Z \times f_C} \quad (16)$$

Determine if the second compensation capacitor (C_P) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency or the following relationship is valid:

$$\frac{1}{2\pi \times C_O \times ESR_{CO}} < \frac{f_{SW}}{2} \quad (17)$$

If this is the case, then add the second compensation capacitor (C_P) to set the pole f_{P3} at the location of the ESR zero. Determine the C_P value by the equation:

$$C_P = \frac{C_{OUT} \times ESR}{R_Z} \quad (18)$$

Finally, take a look at the combined bode plot of both the control-to-output and the compensated error amp— see the red curves shown in Figure 5. Careful examination of this plot shows that the magnitude and phase of the entire system are simply the sum of the error amp response (blue) and the control-to-output response (green). As shown in Figure 5, the bandwidth of this system (f_C) is 25.2 kHz, the phase margin is 52.5 degrees, and the gain margin is 22 dB. These values are theoretical; actual measured values may be different. Some fine-tuning of the final compensation components may be necessary in the lab.

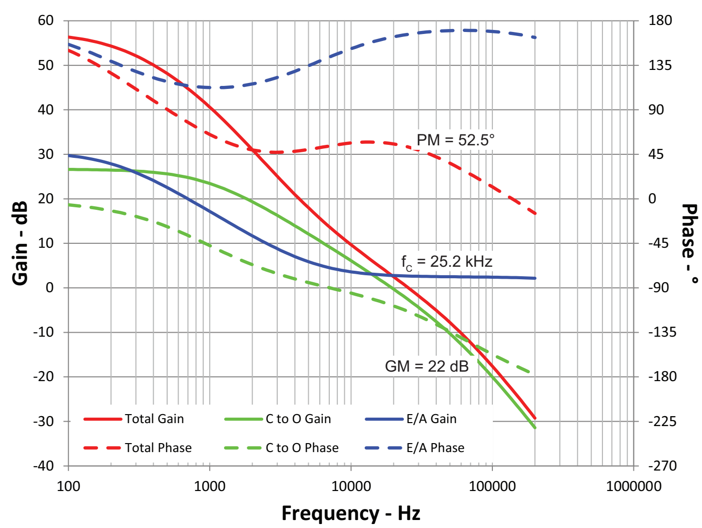

Figure 5: Bode plot of the complete system (red curve) R_Z = 6.19 kΩ, C_Z = 4.7 nF, C_P = 10 pF L_O = 33 µH, C_O = 4 × 10 µF ceramic

Linear Regulators

The two linear regulators only require a ceramic capacitor to ensure stable operation. The capacitor can be any value between 1 µF and 22 µF. A 2.2 µF or 4.7 µF capacitor per regulator is recommended.

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Internal Bias (VCC)

The internal bias voltage should be decoupled at the VCC pin using a 1 µF, 25 V X7R ceramic capacitor. It is not recommended to use this pin as a source.

Signal Pins (NPOR, ENBAT)

The NPOR signal is an open drain output and requires an external pull-up resistor. It is recommended to pull NPOR up to the 3V3 rail, so when the ARG81401 is disabled, NPOR will not be high.

The ENBAT is a high-voltage input pin. It does require a current-limiting resistor when connected to voltages greater than 8 V. There are limitations on this resistor value based on ENBAT sink current, ENBAT enable threshold, and input voltage operating conditions. Minimum ENBAT resistor is 450 Ω. If ENBAT must ensure ARG81401 is enabled down to the minimum operating voltage, then a resistor less than 3.37 kΩ is recommended.

Watchdog (WD_{ENn}, WD_{IN}, WD_{ADJ})

The ARG81401 window watchdog circuit monitors an external clock applied to the WD_{IN} pin. This clock should be generated by the microcontroller or DSP. The time between rising edges of the clock must fall within an acceptable "window" or a watchdog fault will be generated. A watchdog fault will set NPOR for $t_{WD(FAULT)}$ (typically 2 ms). A watchdog fault will occur if the time between rising edges is either too short (a FAST fault) or too long (a SLOW fault).

The watchdog time "window" is programmable via the WD_{ADJ} pin according to the following equations:

$$R_{ADJ} = 3.24 \times t_{WDTO(SLOW)}$$
$$t_{WDTO(FAST)} = t_{WDTO(SLOW)} / 8$$

where $t_{WDTO(SLOW)}$ is the nominal watchdog timeout (in ms) and R_{ADJ} is the required external resistor value (in kΩ) from the WD_{ADJ} pin to ground. Typical watchdog operation under FAST and SLOW fault conditions are shown in Figure 7 and Figure 8. The watchdog is enabled if two conditions are met:

1. the WD_{ENn} pin is a logic low, and
2. all regulators (3V3 and V5) have been above their undervoltage thresholds for at least 30 ms_{TYP} ($t_{WD(START)}$).

After startup, if no clock edges are detected at WD_{IN} for at least $t_{WD(START)} + t_{WDTO(SLOW)}$, the ARG81401 will set NPOR low for $t_{WD(FAULT)}$ and reset its counters. This process will repeat until the system recovers and clock edges are applied to WD_{IN}.

A timing diagram for the "missing clock" situation is shown in Figure 9. Figure 10 shows the WD_{FAULT} signal during a fast clock fault.

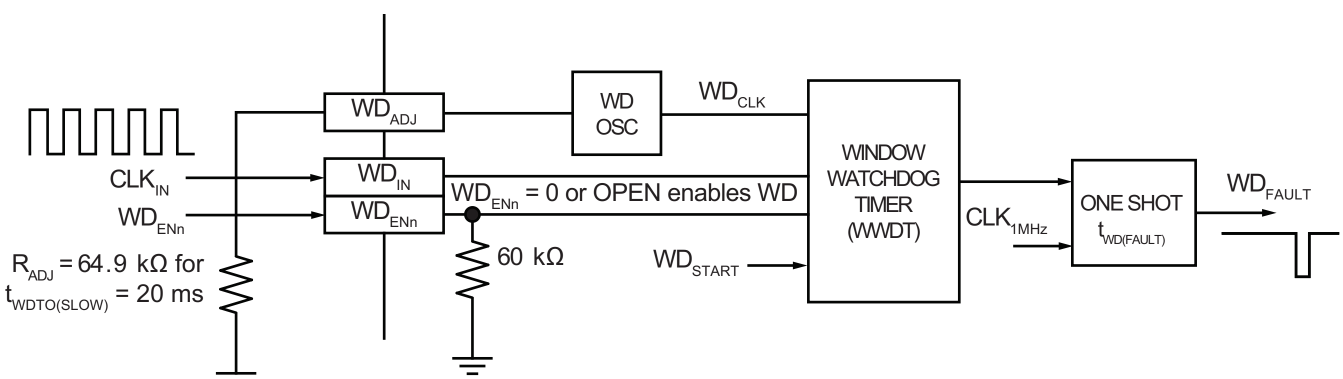

Figure 6: Watchdog Block Diagram

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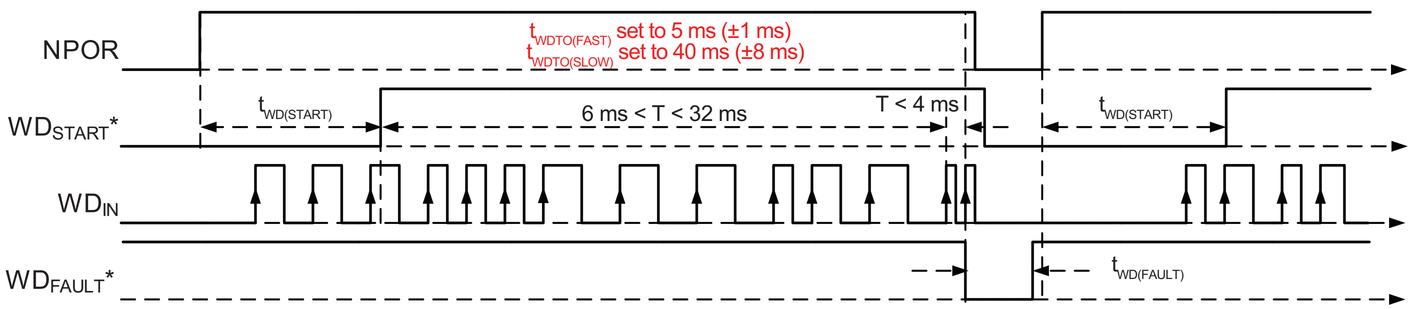

Figure 7: Window Watchdog Timer FAST Fault, T = WD_{IN} period
*** Signal is internal to ARG81401**

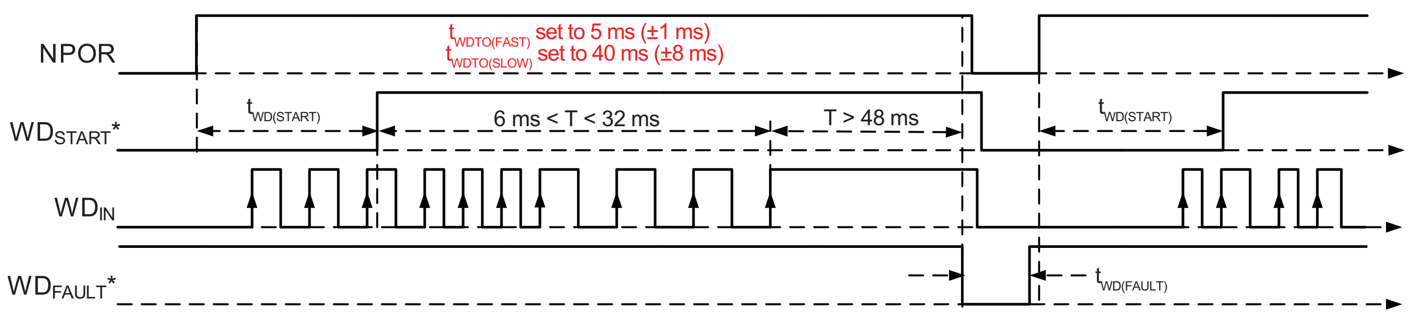

Figure 8: Window Watchdog Timer SLOW Fault, T = WD_{IN} period
*** signal is internal to ARG81401**

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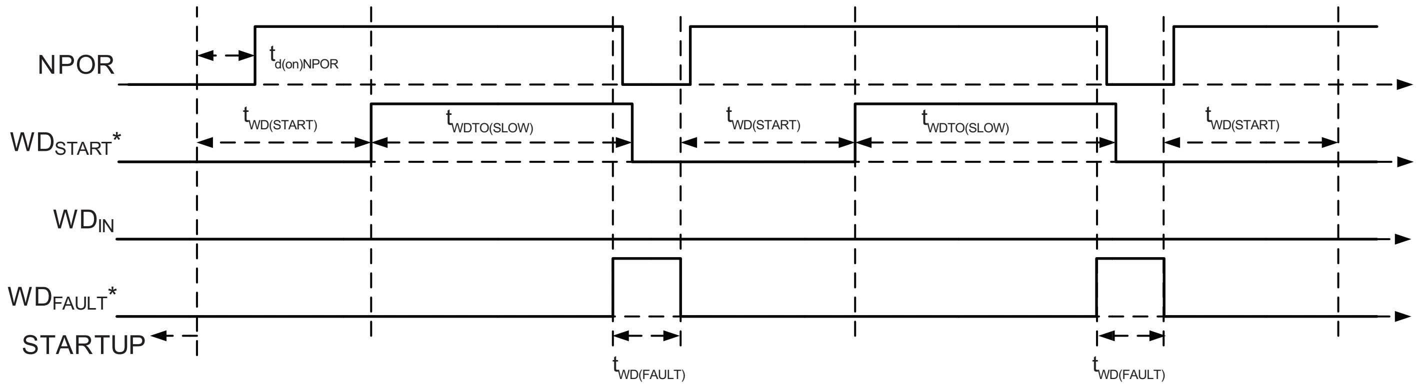

Figure 9: Window Watchdog Timer operation during slow clock fault, WD_{IN} stuck low or high
*** signal is internal to ARG81401**

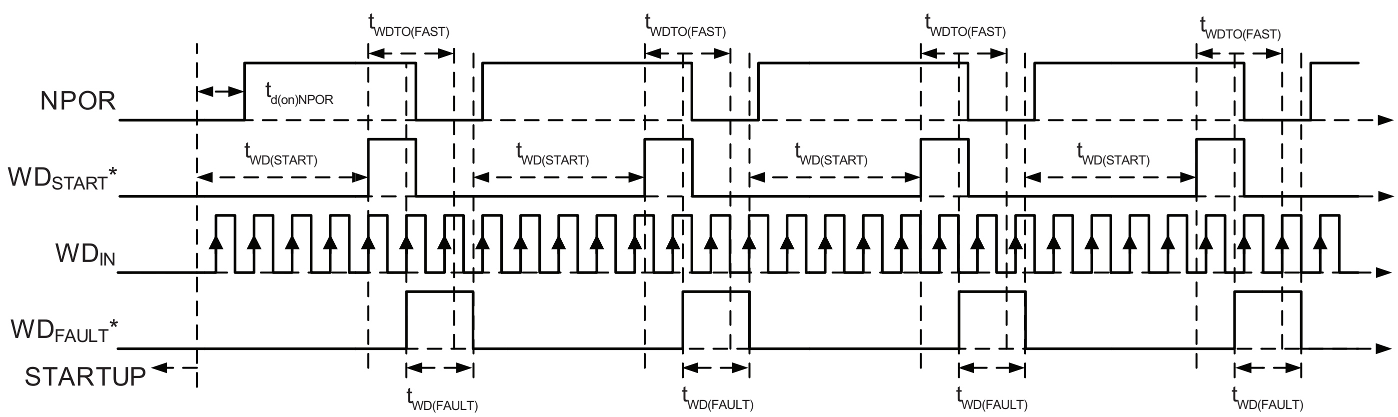

Figure 10: Window Watchdog Timer operation during fast clock fault
*** signal is internal to ARG81401**

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PCB LAYOUT GUIDELINES

Good layout of the power components and high di/dt loops is critical to proper operation of the ARG81401. It also helps to reduce EMI generation.

The first loop to consider is the buck regulator input loop. This consists of the input capacitors C3, C4, and C5, pins 2 and 18 of the ARG81401, and the diode D2. Figure 11 shows this loop in red.

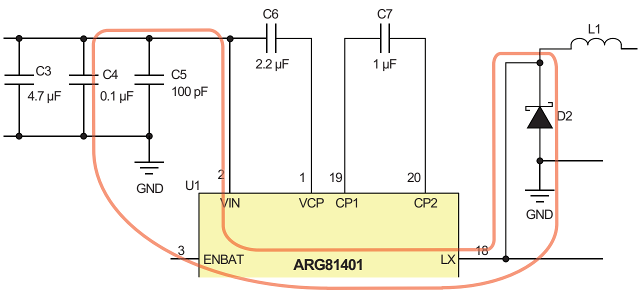

Figure 11: Buck High di/dt Loop

An example of how these components may be placed is shown below. Ensure that these components and connecting traces are on the same side of the PCB. Also ensure the enclosed area within the loop is as small as possible. The switch node trace connected to LX should be as short and as wide as possible to ensure the lowest possible impedance.

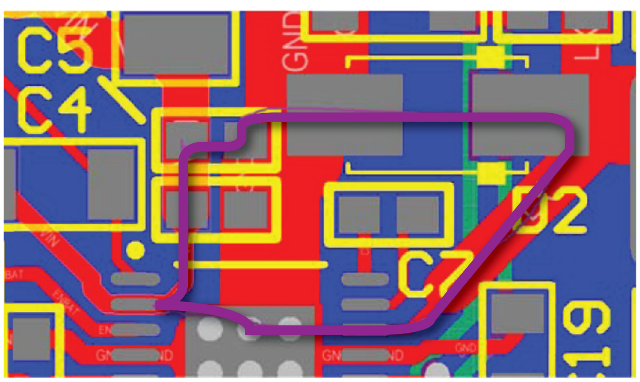

Figure 12

If the ARG81401 is configured as a buck-boost, then the boost output loop needs to be considered. This is made up of the boost MOSFET Q1, boost diode D7, and output capacitors C30 and C8. The boost switch node (L1, Q1 drain, and D7 anode) should be as short and as wide as possible to ensure the lowest possible impedance.

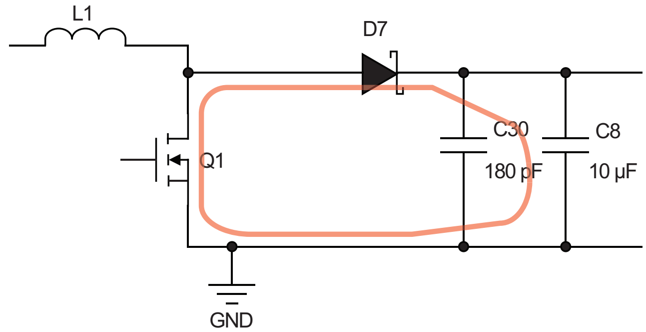

Figure 13: Boost Output Loop

Layout below shows the boost high di/dt loop.

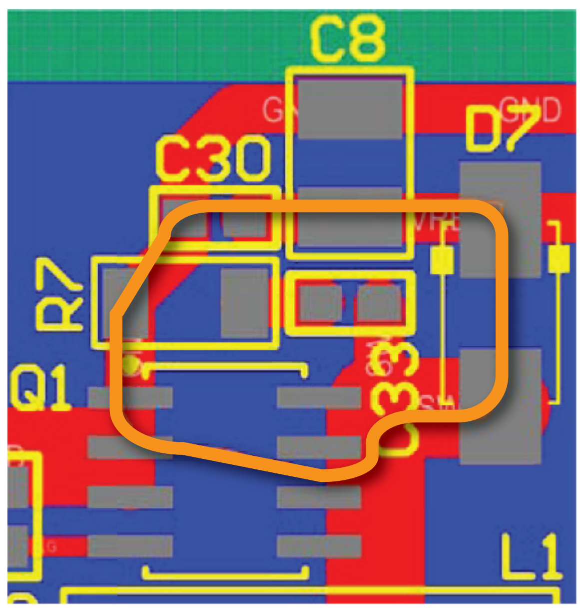

Figure 14: Boost High di/dt Loop

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Also if configured for buck-boost mode, then care must be taken with the gate drive trace. The turn-on pulse is from C17 through ARG81401 pin 16 to Q1 gate and source back to C17. The turn-off pulse is from Q1 gate to ARG81401 pin 16 back to Q1 source through the ground.

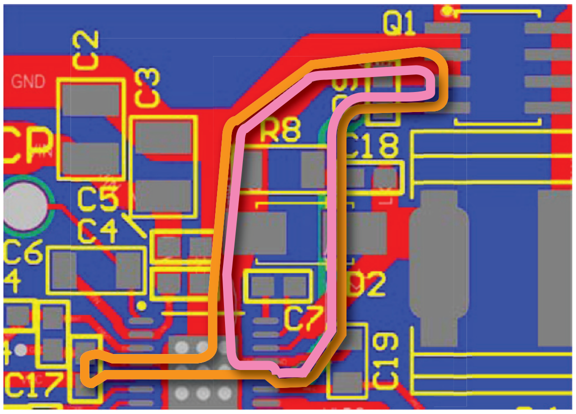

Figure 15

Other sensitive nodes to keep small are the FSET/SYNC to R3, the COMP pin to C15 and C16, and WD_{ADJ} pin to R_{ADJ}.

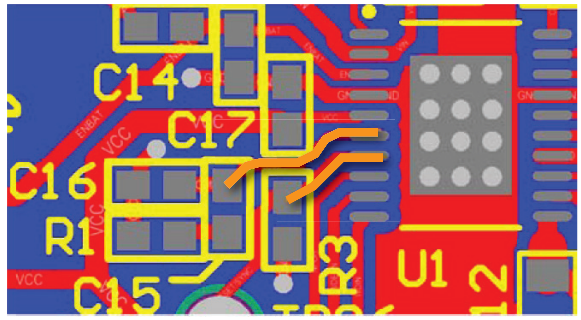

Figure 16

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PIN ESD STRUCTURES

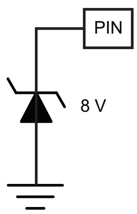

Figure 17: VCC, COMP, FSET/SYNC, NPOR, WD_{ENn}, WD_{IN}, 3V3, V5, WD_{ADJ}, VLDO, VREG, LG

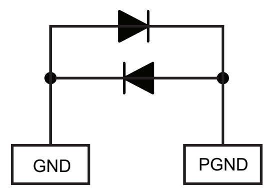

Figure 18: GND, PGND

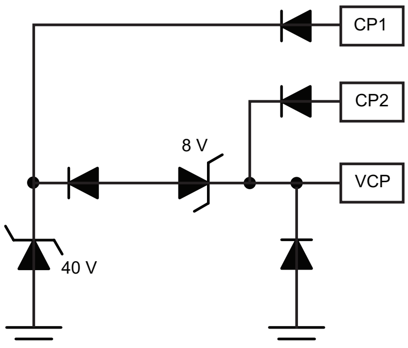

Figure 19: VCP, CP1, CP2

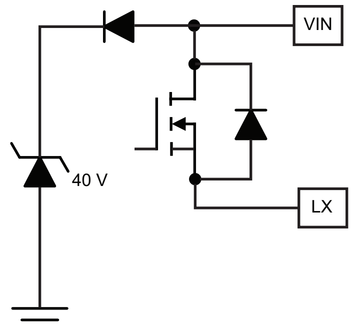

Figure 20: VIN, LX

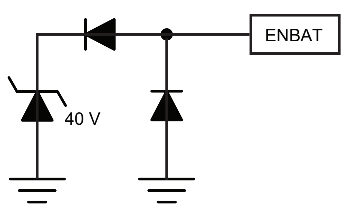

Figure 21: ENBAT

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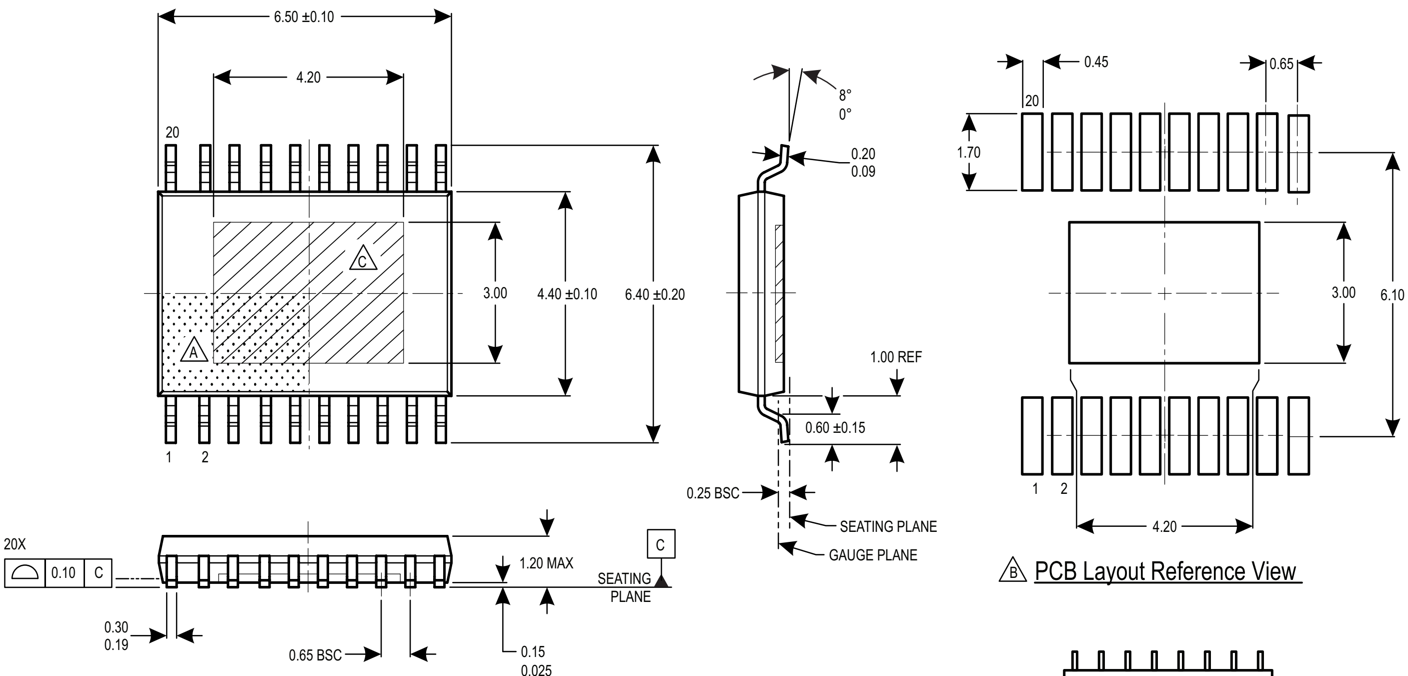
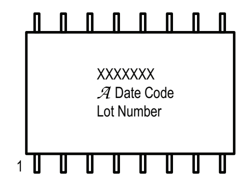
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153ACT; Allegro DWG-0000379, Rev. 3)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





D Standard Branding Reference View

Line 1, 2, 3 = 8 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-21M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface)

D Branding scale and appearance at supplier discretion

Figure 22: Package LP, 20-Pin eTSSOP

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Revision History

Number	Date	Description
–	June 21, 2017	Initial release
1	June 25, 2018	Minor editorial updates
2	July 3, 2019	Minor editorial updates
3	March 19, 2021	Updated Equation 4 (page 21)
4	April 6, 2022	Updated package drawing (page 30)
5	March 14, 2024	Updated product status to Last-Time Buy
6	September 12, 2024	Updated product status to Discontinued

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