ARG81800

40 V, 500 mA / 1.0 A Synchronous Buck Regulators with Ultralow Quiescent Current, $SYNC_{IN}$, CLK_{OUT}, and PGOOD

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Input operating voltage range: 3.5 to 36 V
  - □ Withstands surge voltages to 40 V for load dump
- Low-Power (LP) mode—draws just 8 µA from V_{IN} while maintaining 3.3 or 5.0 V_{OUT}
- AUTO mode allows automatic transition between PWM and LP mode based on load current
- Programmable PWM frequency (f_{SW}): 250 kHz to 2.4 MHz
- PWM frequency dithering and controlled switch node slew rate reduce EMI/EMC signature
- CLK_{OUT} allows interleaving and dithering of "downstream" regulators using their synchronization inputs
- Interleaving minimizes input filter capacitor requirement and improves EMI/EMC performance
- Synchronization of PWM frequency to external clock on $SYNC_{IN}$ pin
- Adjustable output voltage: ±1.5% accuracy over operating temperature range (–40°C to 150°C)
- Maximized duty cycle at low V_{IN} improves dropout
- Soft recovery from dropout condition
- Adjustable soft-start time controls inrush current to accommodate a wide range of output capacitances
- External compensation provides flexibility to tune the system for maximum stability or fast transient response

Continued on next page...

APPLICATIONS

- Infotainment
- Navigation Systems
- Instrument Clusters
- Audio Systems
- ADAS Applications
- Battery Powered Systems
- Industrial Systems
- Network and Telecom
- Home Audio
- HVAC Systems

DESCRIPTION

The ARG81800 includes all the control and protection circuitry to produce a PWM regulator with ±1.5% output voltage accuracy, with ultralow quiescent current to enable "keepalive" supply operation with minimal current draw from the supply during very light load regulation. There are two versions of the ARG81800 available, 500 mA and 1 A, so the physical size of the power components can be optimized for lower current systems, thus reducing PCB area and saving cost. PWM switching frequency can be programmed over a wide range to balance efficiency, component sizing, and EMC performance. If V_{IN} decays and the duty cycle reaches its maximum, the ARG81800 will automatically fold back its PWM frequency to extend the duty cycle and maintain V_{OUT}.

The ARG81800 employs Low-Power (LP) mode to maintain the output voltage at no load or very light load conditions while drawing only micro-amps from V_{IN}. The ARG81800 includes a PWM/AUTO control pin so the system can dynamically force either PWM or AUTO mode by setting this pin high or low, respectively.

If the $SYNC_{IN}$ pin is driven by an external clock, the ARG81800 will be forced into PWM mode and synchronize to the incoming clock. The ARG81800 adds frequency dithering to the $SYNC_{IN}$ clock to reduce EMI/EMC. The ARG81800 provides a CLK_{OUT} pin so "downstream" regulators can be easily interleaved and dithered via their synchronization inputs.

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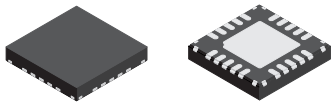
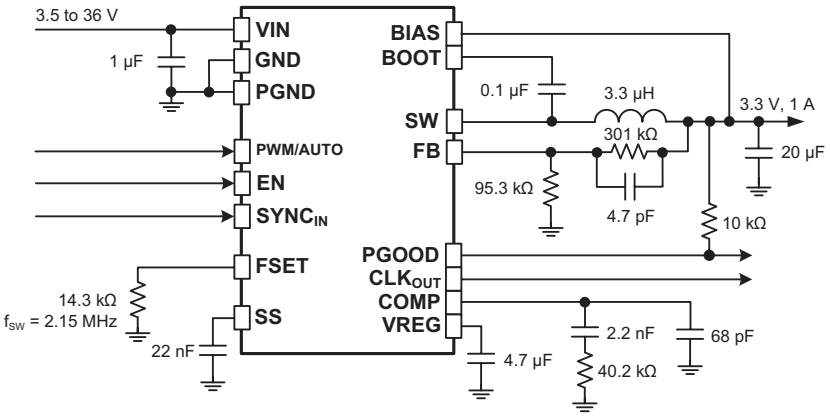


20-pin, 4 mm × 4 mm, QFN (ES) with wettable flank

Not to scale



Typical Application Diagram

FEATURES AND BENEFITS

- Enable input can command ultralow 1 µA shutdown current
- Open-drain PGOOD output with rising delay
- Pre-bias startup allows quick restart and avoids reset
- Overvoltage, pulse-by-pulse current limit, hiccup mode short circuit, and thermal protections
- Robust FMEA: pin open/short and component faults

DESCRIPTION

The ARG81800 has external compensation, so it can be tuned to satisfy a wide range of system goals with many different external components over a wide range of PWM frequencies. The ARG81800 includes adjustable soft start to minimize inrush current. The ARG81800 monitors the feedback voltage to provide an open-drain power good signal. The Enable input can command an ultra-low current shutdown mode with V_{OUT} = 0 V.

Extensive protection features of the ARG81800 include pulse-by-pulse current limit, hiccup mode short circuit protection, BOOT open/short voltage protection, V_{IN} undervoltage lockout, V_{OUT} overvoltage protection, and thermal shutdown. The ARG81800 is supplied in a low profile 20-pin wettable flank QFN package (suffix "ES") with exposed power pad.

SELECTION GUIDE

Part Number	DC Current	Package	Packing	Lead Frame
ARG81800KESJSR	1 A	20-pin wettable flank QFN package with thermal pad	6000 pieces per 13-inch reel	100% matte tin
ARG81800KESJSR-1	0.5 A			

*Contact Allegro for additional packing options

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
VIN, EN, SS, BIAS Pin Voltage			–0.3 to 40	V
SW Pin Voltage	V_{SW}	Continuous	–0.3 [2] to V_{IN} + 0.3	V
		V_{IN} ≤ 36 V, t < 50 ns	–1.0 to V_{IN} + 2	V
BOOT Pin Voltage	V_{BOOT}	Continuous	V_{SW} – 0.3 to V_{SW} + 5.5	V
		t < 1 ms	V_{SW} – 0.3 to V_{SW} + 7.0	V
All Other Pin Voltages			–0.3 to 5.5	V
Operating Junction Temperature	$T_{J(max)}$		–40 to 150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[1] Stresses beyond the ratings listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.

[2] This voltage is a function of temperature.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	37	°C/W

[3] Additional thermal information available on the Allegro website.

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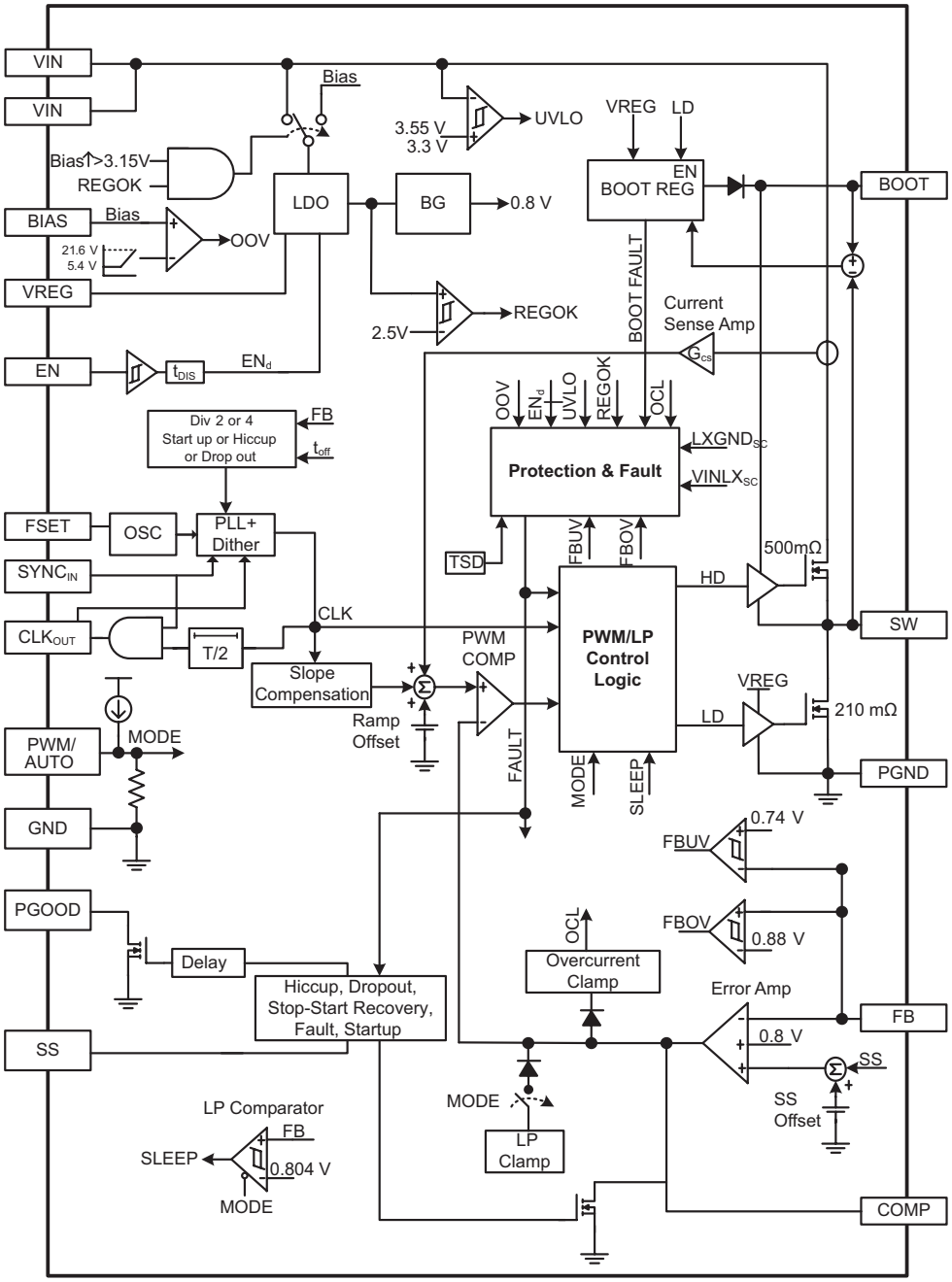

Functional Block Diagram

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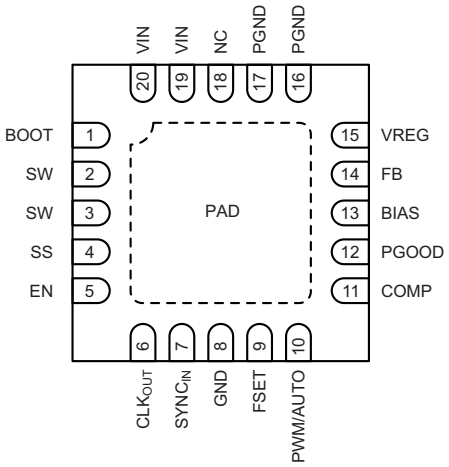
PINOUT DIAGRAM AND TERMINAL LIST



Package ES, 20-Pin QFN Pinout Diagram

Terminal List Table

Number	Name	Function
1	BOOT	This pin supplies the drive for the high-side N-channel MOSFET. Connect a 100 nF ceramic capacitor from BOOT to SW. Do not add any external resistor in series with the boot capacitor.
2, 3	SW	Regulator switch node output pins. Connect these pins to power inductor with a short and wide PCB trace.
4	SS	Soft start pin. Connect a capacitor, C_{SS}, from this pin to GND to set the start-up time. This capacitor also determines the hiccup period during overcurrent.
5	EN	This pin must be set high to enable the ARG81800. If this pin is low, the ARG81800 will enter a very low current shutdown or “SLEEP” state where V_{OUT} = 0 V. If the application does not require a logic level controlled enable, then this pin can be tied directly to V_{IN}. Also, if this pin is floated, it will be pulled low by an internal pull-down resistor, disabling the ARG81800.
6	CLK_{OUT}	Dual function pin: Clock output pin for “Master” operation. Frequency dithering is added to this pin when the ARG81800 is operating as a Master. For “Follower” operation, this pin must be connected to VREG so dithering will not be internally added to $SYNC_{IN}$; see Figure 1. The exact functionality of this pin is dependent on the status of the $SYNC_{IN}$ pin; see Table 1 and the description for $SYNC_{IN}$ for additional details.
7	$SYNC_{IN}$	Triple function pin: High/Low/ExtClock. Setting this pin high sets CLK_{OUT} to the internal oscillator frequency (f_{SW}) but with 180 degree phase shift. Setting this pin low disables the CLK_{OUT} pin. Applying an external clock (at f_{SYNC}) forces PWM mode, synchronizes the PWM switching frequency to the external clock plus dithering, and sets CLK_{OUT} to the same dithered frequency but with 180 degree phase shift. See Table 1 for details.
8	GND	Analog ground pin.
9	FSET	Frequency setting pin. A resistor, R_{FSET}, from this pin to GND sets the oscillator frequency, f_{SW}.
10	PWM/ AUTO	Mode selection pin. High/Low. Setting this pin high forces PWM mode. Setting this pin low allows AUTO changeover between PWM and LP mode based on the load current.
11	COMP	Output of the error amplifier and compensation node for the current mode control loop. Connect a series RC network from this pin to GND for loop compensation.
12	PGOOD	Power good output signal. PGOOD is an open-drain output that remains low until the output has achieved regulation for $t_{dPG(SU)}$. The PGOOD pull-up resistor can be connected to VREG, VOUT, or any external supply voltage less than 5.5 V. PGOOD will pull low if the output voltage (V_{OUT}) is out of range.
13	BIAS	Connect this pin to the output of the regulator. This pin supplies the internal circuitry when the voltage level is high enough.
14	FB	Feedback (negative) input to the error amplifier. Connect a resistor divider from the regulators output, V_{OUT}, to this pin to program the output voltage.
15	VREG	Internal voltage regulator bypass capacitor pin. Connect a 4.7 µF capacitor from this pin to PGND and place it very close to the ARG81800.
16, 17	PGND	Power ground pins for the lower MOSFET, gate driver, and BOOT charge circuit.
18	NC	No connection.
19, 20	VIN	Power input for the control circuits and the drain of the internal high-side N-channel MOSFET. Bypass VIN to PGND with an X7R or X8R ceramic capacitor. Place the capacitor as close to the VIN and PGND pins as possible. Additional capacitors may be required depending on the application to comply with EMC requirements.
–	PAD	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane of the PCB with at least 6 vias directly in the pad.

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ELECTRICAL CHARACTERISTICS: Valid at 3.5 V ≤ V_{IN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
INPUT VOLTAGE						
Input Voltage Range	V_{IN}	V_{IN} must first rise above $V_{INUV(ON)}$ (max)	3.5	–	36	V
VIN UVLO Start	$V_{INUV(ON)}$	V_{IN} rising	3.35	3.55	3.8	V
VIN UVLO Stop	$V_{INUV(OFF)}$	V_{IN} falling	3.1	3.3	3.5	V
VIN UVLO Hysteresis	$V_{INUV(HYS)}$		–	250	–	mV
INPUT SUPPLY CURRENT						
Input Shutdown Current [2]	$I_{IN(SD)}$	V_{IN} = 12 V, V_{EN} = 0, V_{SW} = V_{IN}, T_J = 25°C	–	1	2	µA
Input Current, PWM Mode [2]	$I_{IN(PWM)}$	V_{IN} = 12 V, V_{EN} = 2 V, no load, no switching	–	5	6.5	mA
3.3 V_{OUT} LP Input Current [3][4]	$I_{LP(3.3V)}$	V_{IN} = 12 V, I_{OUT} = 0 µA, T_J = 25°C	–	8	–	µA
		V_{IN} = 12 V, I_{OUT} = 50 µA, T_J = 25°C	–	33	–	µA
5.0 V_{OUT} LP Input Current [3][4]	$I_{LP(5.0V)}$	V_{IN} = 12 V, I_{OUT} = 0 µA, T_J = 25°C	–	8	–	µA
		V_{IN} = 12 V, I_{OUT} = 50 µA, T_J = 25°C	–	44	–	µA
REGULATION ACCURACY (FB PIN)						
Feedback Voltage Accuracy	V_{FB}	–40°C < T_J < 150°C, V_{IN} ≥ 3.5 V, V_{FB} = V_{COMP}	788	800	812	mV
SWITCHING FREQUENCY AND DITHERING (FSET PIN)						
PWM Switching Frequency	f_{SW}	R_{FSET} = 14.3 kΩ	1.93	2.15	2.37	MHz
		R_{FSET} = 34 kΩ	0.90	1.00	1.10	MHz
		R_{FSET} = 71.5 kΩ	450	500	550	kHz
		R_{FSET} = 86.6 kΩ	360	410	460	kHz
Dropout Switching Frequency	f_{DROP}		–	f_{SW}/4	–	–
PWM Frequency Dither Range	$f_{DITH(RNG)}$	CLK_{OUT} left open	–	±5	±6.5	% of f_{SW}
		CLK_{OUT} connected to VREG	–	0	–	% of f_{SW}
PWM Dither Modulation Frequency	$f_{DITH(MAG)}$		–	±0.5	–	% of f_{SW}
PULSE WIDTH MODULATION (PWM) TIMING AND CONTROL						
Minimum Controllable SW On-Time	$t_{ON(MIN)}$	V_{IN} = 12 V, I_{OUT} = 0.7 A, V_{BOOT} – V_{SW} = 4.5 V	–	60	85	ns
Minimum SW Off-Time	$t_{OFF(MIN)}$	V_{IN} =12 V, I_{OUT} = 0.7 A	–	85	110	ns
COMP to SW Current Gain	gm_{POWER1}	ARG81800	–	2.0	–	A/V
	gm_{POWER2}	ARG81800-1	–	1.0	–	A/V
Slope Compensation	S_{E1}	f_{SW} = 2.15 MHz, ARG81800	650	900	1100	mA/µs
	S_{E2}	f_{SW} = 2.15 MHz, ARG81800-1	325	450	550	mA/µs
	S_{E3}	f_{SW} = 252 kHz, ARG81800	75	100	125	mA/µs
	S_{E4}	f_{SW} = 252 kHz, ARG81800-1	35	50	65	mA/µs
PWM Ramp Offset	$V_{PWM(OFFS)}$		–	650	–	mV

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOW-POWER (LP) MODE						
LP Output Voltage Ripple [3][4]	$\Delta V_{OUT(LP)}$	LP Mode, 8 V < V_{IN} < 12 V	–	65	–	mV
Low I_Q Peak Current Threshold	$I_{PEAK(LP1)}$	ARG81800, No Load, V_{IN} = 12 V	320	400	500	mA
	$I_{PEAK(LP2)}$	ARG81800-1, No Load, V_{IN} = 12 V	160	212	270	mA
INTERNAL POWER SWITCHES						
High-Side MOSFET On-Resistance	$R_{DS(on)HS}$	T_J =25°C [3], V_{BOOT} – V_{SW} = 4.5 V, I_{DS} = 800 mA	–	500	600	mΩ
		T_J = 150°C, V_{BOOT} – V_{SW} = 4.5 V, I_{DS} = 800 mA	–	–	1075	mΩ
Low-Side MOSFET On-Resistance	$R_{DS(on)LS}$	T_J =25°C [3], V_{IN} ≥ 4.5 V, I_{DS} = 1 A	–	210	250	mΩ
		T_J =150°C, V_{IN} ≥ 4.5 V, I_{DS} = 1 A	–	–	450	mΩ
High-Side Leakage Current [5]	$I_{LKG(HS)}$	T_J = 25°C, V_{IN} = 12 V, V_{EN} = 0 V, V_{SW} = 0 V	–1.5	–	1.5	µA
Low-Side Leakage Current	$I_{LKG(HS)}$	T_J = 25°C, V_{IN} = 12 V, V_{EN} = 0 V, V_{SW} = 12 V	–1.5	–	1.5	µA
Gate Drive Non-Overlap Time [3]	t_{NO}		–	10	25	ns
Switch Node Rising Slew Rate	SR_{HS}	12 V < V_{IN} < 16 V [3]	–	5	–	V/ns
MOSFET CURRENT PROTECTION THRESHOLDS						
High-Side Current Limit	I_{LIMHS1}	t_{ON} = $t_{ON(MIN)}$, ARG81800	1.7	2.0	2.3	A
	I_{LIMHS2}	t_{ON} = $t_{ON(MIN)}$, ARG81800-1	0.85	1.0	1.15	A
Low-Side Current Limit	I_{LIMLSx}		–	50	–	% of I_{LIMHSx}
SYNCHRONIZATION INPUT ($SYNC_{IN}$ PIN)						
Synchronization Frequency Range	$f_{SW(SYNC)}$		0.25	–	2.5	MHz
$SYNC_{IN}$ Duty Cycle	DC_{SYNC}		20	50	70	%
$SYNC_{IN}$ Pulse Width	t_{PWSYNC}		80	–	–	ns
$SYNC_{IN}$ Voltage Thresholds	$V_{SYNC(HI)}$	$V_{SYNC(IN)}$ rising	–	1.35	1.5	V
	$V_{SYNC(LO)}$	$V_{SYNC(IN)}$ falling	0.8	1.2	–	V
$SYNC_{IN}$ Hysteresis	$V_{SYNC(HYS)}$	$V_{SYNC(HI)}$ – $V_{SYNC(LO)}$	–	150	–	mV
$SYNC_{IN}$ Pin Current	I_{SYNC}	$V_{SYNC(IN)}$ = 5 V	–	±1	–	µA
CLOCK OUTPUT (CLK_{OUT} PIN)						
$SYNC_{IN}$ to CLK_{OUT} Delay	$\Phi_{SYNC(CLK)}$	R_{FSET} = 14.3 kΩ, $V_{SYNC(HI)}$ = 3.3 V, Dither disabled	–	1/(2×f_{SW}) ± 70	–	ns
SW_{MASTER} to $SW_{FOLLOWER}$ Delay [3]	$\Phi_{SWM(SWF)}$	R_{FSET} = 14.3 kΩ, $V_{SYNC(HI)}$ = 3.3 V	–	1/(2×f_{SW}) ± 30	–	ns
CLK_{OUT} Output Voltages	$V_{CLK(OUT)H}$	V_{VREG} = 4.8 V	2.2	–	–	V
	$V_{CLK(OUT)L}$	V_{VREG} = 4.8 V	–	–	0.6	V

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ELECTRICAL CHARACTERISTICS (continued): Valid at 3.5 V ≤ V_{IN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ERROR AMPLIFIER						
Feedback Input Bias Current [2]	I_{FB}	V_{FB} = 800 mV	–40	–	–15	nA
Open-Loop Voltage Gain	A_{VOL}		–	65	–	dB
Transconductance	gm	V_{FB} > 400 mV	550	750	950	µA/V
		0 V < V_{FB} < 400 mV	275	375	550	µA/V
Output Current	I_{EA}		–	±75	–	µA
COMP Pull-Down Resistance	R_{COMP}	FAULT = 1 or HICCUP = 1	–	1	–	kΩ
SOFT START						
Startup (Source) Current	I_{SS}	HICCUP = FAULT = 0	−30	−20	−10	µA
Hiccup/Dropout (Sink) Current	I_{HIC}	HICCUP = 1 or Dropout Mode	1	2.2	5	µA
Soft Start Delay Time [3]	t_{dSS}	C_{SS} = 22 nF	–	440	–	µs
Soft Start Ramp Time [3]	t_{SS}	C_{SS} = 22 nF	–	880	–	µs
FAULT/HICCUP Reset Voltage	V_{SSRST}	V_{SS} falling due to HICCUP or FAULT	–	200	275	mV
Hiccup OCP (and LP) Counter Enable Threshold	$V_{HIC/LP(EN)}$	V_{SS} rising	–	2.3	–	V
Soft Start Frequency Foldback	$f_{SW(SS)}$	0 V < V_{FB} < 200 mV	–	f_{SW} / 4	–	–
		200 mV < V_{FB} < 400 mV	–	f_{SW} / 2	–	–
		400 mV < V_{FB}	–	f_{SW}	–	–
Maximum Voltage	$V_{SS(MAX)}$	V_{EN} = 0 V or FAULT without HICCUP	–	V_{VREG}	–	–
Pull-Down Resistance	$R_{SS(FLT)}$			2		kΩ
HICCUP MODE COUNTS						
High-Side Overcurrent Count	HIC_{OC}	After V_{SS} > $V_{HIC/LP(EN)}$	–	120	–	f_{SW} counts
SW Short-to-Ground Count	$HIC_{SW(GND)}$		–	2	–	f_{SW} counts
BOOT Short Circuit Count	$HIC_{BOOT(SC)}$		–	120	–	f_{SW} counts
BOOT Open Circuit Count [3]	$HIC_{BOOT(OC)}$		–	7	–	f_{SW} counts

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE PROTECTION THRESHOLDS (VFB, OV, UV)						
VFB OV PWM Threshold	$V_{FB(OV)}$	V_{FB} rising	850	880	900	mV
VFB OV PWM Hysteresis	$V_{FB(OV,HYS)}$	V_{FB} falling, relative to $V_{FB(OV)}$	–	−15	–	mV
VFB UV PWM Threshold	$V_{FB(UV)}$	V_{FB} falling	716	740	764	mV
VFB UV PWM Hysteresis	$V_{FB(UV,HYS)}$	V_{FB} rising, relative to $V_{FB(UV)}$	–	+15	–	mV
VFB UV LP Mode Threshold [3]	$V_{FB(UV,LP)}$	V_{FB} falling	665	700	735	mV
POWER GOOD OUTPUT (PGOOD PIN)						
PGOOD Startup (SU) Delay	$t_{dPG(SU)}$	Increasing V_{FB} due to startup	–	30	–	µs
PGOOD Undervoltage (UV) Delay	$t_{dPG(UV)}$	Decreasing VFB	–	30	–	µs
PGOOD Overvoltage (OV) Delay	$t_{dPG(OV)}$	After an overvoltage event	–	240	–	f_{SW} cycles
PGOOD Low Voltage	$V_{PG(L)}$	I_{PGOOD} = 5 mA	–	200	400	mV
PGOOD Leakage [1]	$I_{PG(LKG)}$	V_{PGOOD} = 5.5 V	–	–	2	µA
PWM/AUTO INPUT						
PWM/AUTO High Threshold	$V_{HI(PWM)}$	$V_{PWM/AUTO}$ rising	1.8	2.0	2.5	V
PWM/AUTO Float Voltage	$V_{FLOAT(PWM)}$	$V_{PWM/AUTO}$ floating	1.1	1.4	1.7	V
PWM/AUTO Low Threshold	$V_{LO(PWM)}$	$V_{PWM/AUTO}$ falling	0.6	0.8	1.0	V
PWM to LP Transition Delay [3]	$t_{dPWM(LP)}$	$V_{PWM/AUTO}$ = 0 V, V_{SS} > $V_{HIC/LP(EN)}$, PGOOD high	–	7.5	–	ms
ENABLE INPUT (EN PIN)						
Enable High Threshold	V_{ENHI}	V_{EN} rising	–	1.6	2.0	V
Enable Low Threshold	V_{ENLO}	V_{EN} falling	0.8	1.4	–	V
Enable Input Hysteresis	V_{ENHYS}	V_{ENHI} – V_{ENLO}	–	200	–	mV
Disable Delay	t_{DISDLY}	V_{EN} transitions low to when SW stops switching	–	120	–	f_{SW} cycles
Enable Pin Input Current	I_{EN}	V_{EN} = $V_{PWM/AUTO}$ = 5 V	–	12	–	µA

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
BOOT REGULATOR (BOOT PIN)						
BOOT Charging Frequency	f_{BOOT}		–	f_{SW}	–	–
BOOT Voltage	V_{BOOT}	V_{IN} = 12 V, V_{BOOT} – V_{SW}	–	4.8	5.3	V
INTERNAL REGULATOR (VREG PIN)						
BIAS Disconnected	V_{VREG1}	6 V < V_{VIN} < 36 V, V_{BIAS} = 0 V	4.5	4.8	5.1	V
BIAS Connected	V_{VREG2}	VBIAS = 3.3V	2.85	3.2	3.29	V
		6 V < V_{BIAS} < 20 V	4.5	4.8	5.1	V
BIAS Input Voltage Range	V_{BIAS}		3.3	–	36	V
THERMAL SHUTDOWN PROTECTION (TSD)						
TSD Rising Threshold [3]	T_{TSD}	T_J rising, PWM stops immediately and COMP and SS are pulled low	155	170	–	°C
TSD Hysteresis [3]	T_{SDHYS}	T_J falling, relative to T_{TSD}	–	20	–	°C

[1] Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[2] Thermally limited depending on input voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[3] Ensured by design and characterization, not production tested.
[4] Using recommended external components specified in Table 3.
[5] At V_{IN} = 36 V, I_{OUT} = 0 A, and T_J = 150°C, V_{OUT} rises to overvoltage threshold due to leakage.

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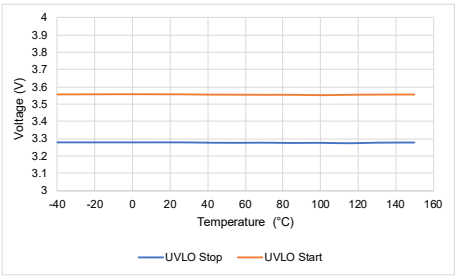
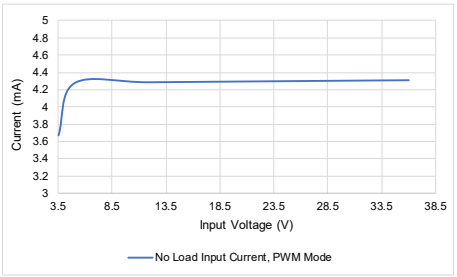
TYPICAL PERFORMANCE CHARACTERISTICS

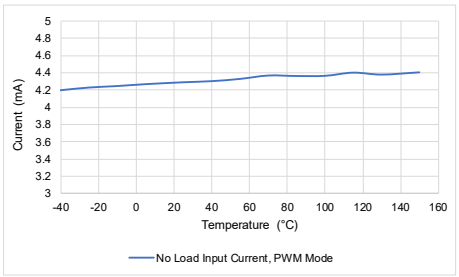
$V_{IN} = V_{EN} = 12$ V, $C_{BOOT} = 0.1$ µF, $C_{SS} = 22$ nF, unless otherwise noted $-40°C \le T_J \le 150°C$. Typical Values are at $T_A = 25°C$.
ARG81800, $V_{OUT} = 3.3$ V, $f_{SW} = 2.15$ MHz. See Table 3 for External Component Values.
ARG81800-1, $V_{OUT} = 5.0$V, $f_{SW} = 0.4$ MHz. See Table 3 for External Component Values.



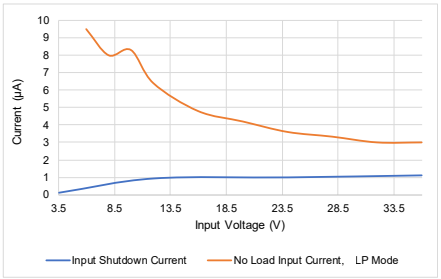
UVLO Start and Stop Thresholds vs. Temperature



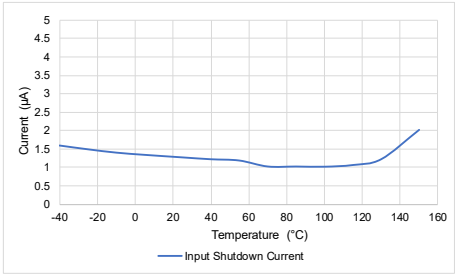
No-Load Input Current (PWM Mode) vs. Input Voltage



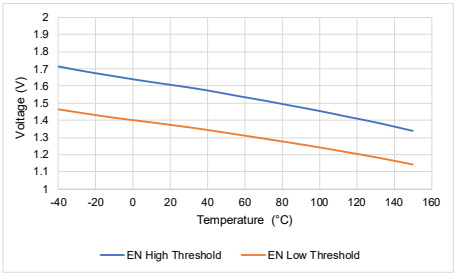
No-Load Input Current (PWM Mode) vs. Temperature



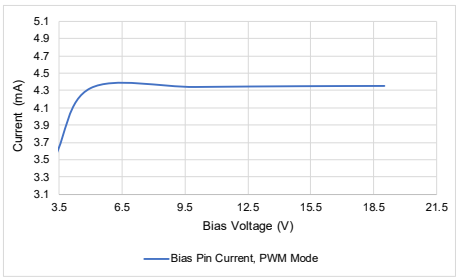
Input Current vs. Input Voltage



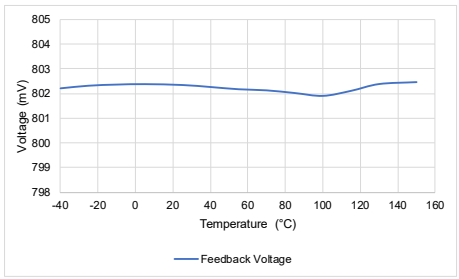
Input Shutdown Current vs. Temperature



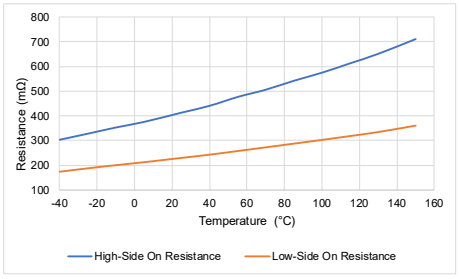
EN High and Low Thresholds vs. Temperature



Bias Pin Current vs. Output Voltage



Feedback Voltage vs. Temperature



On Resistance (High-Side and Low-Side) vs. Temperature

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TYPICAL PERFORMANCE CHARACTERISTICS

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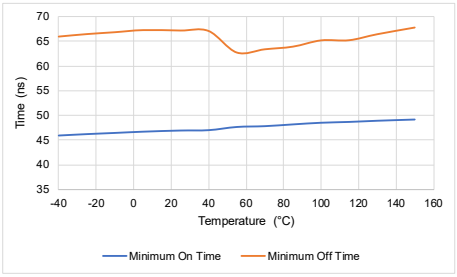
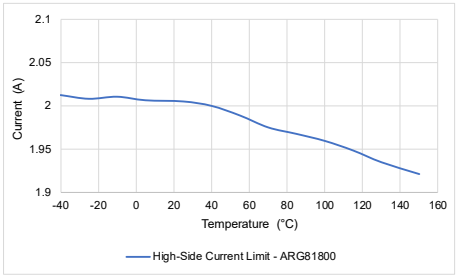
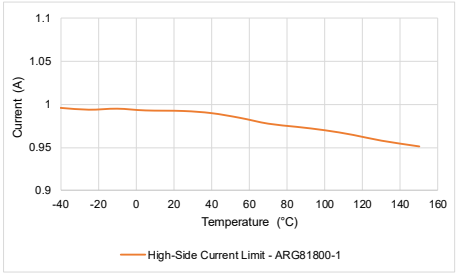


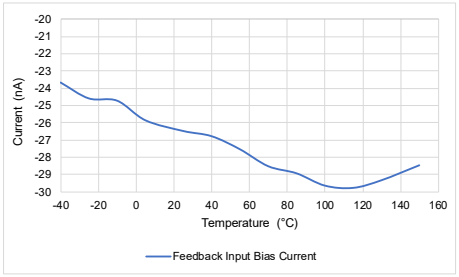
Minimum On and Off Time vs. Temperature



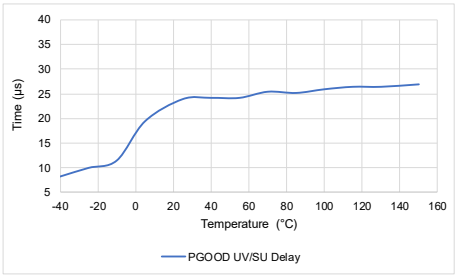
High-Side Current Limit vs. Temperature – ARG81800



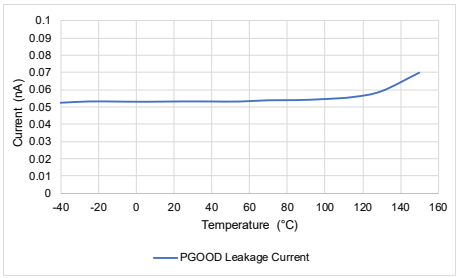
High-Side Current Limit vs. Temperature – ARG81800-1



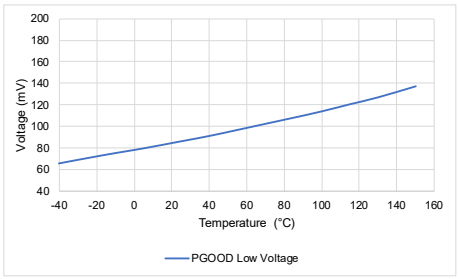
Feedback Input Bias Current vs. Temperature



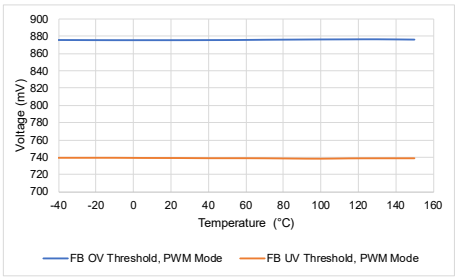
PGOOD Delay (UV and SU) vs. Temperature



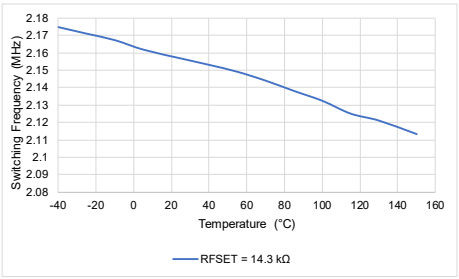
PGOOD Leakage Current vs. Temperature



PGOOD Low Voltage vs. Temperature



Feedback OV and UV Threshold vs. Temperature



Switching Frequency vs. Temperature

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TYPICAL PERFORMANCE CHARACTERISTICS

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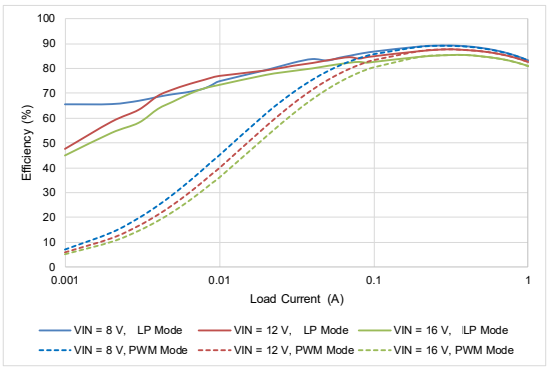
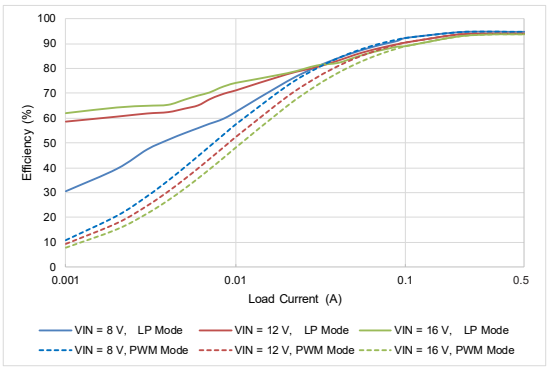
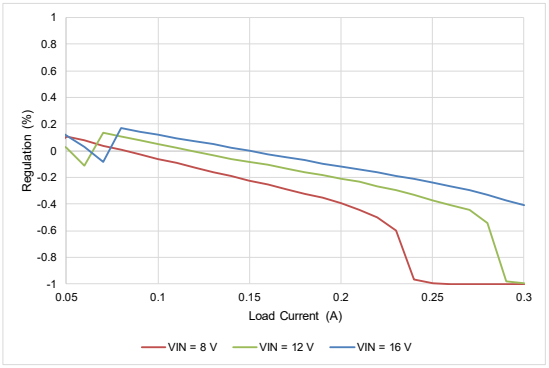
ARG81800-1, $V_{OUT} = 5.0$V, $f_{SW} = 0.4$ MHz. See Table 3 for External Component Values.



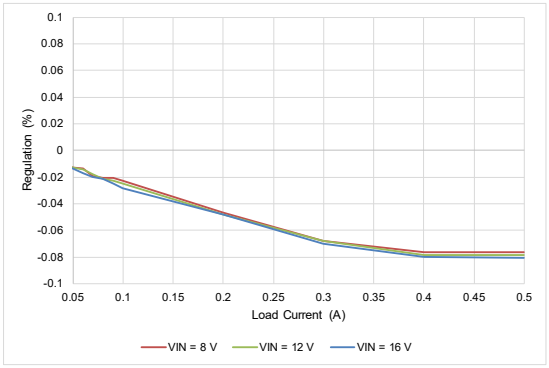
Efficency vs. Load Current
$V_{OUT} = 3.3$ V, $f_{SW} = 2.15$ MHz



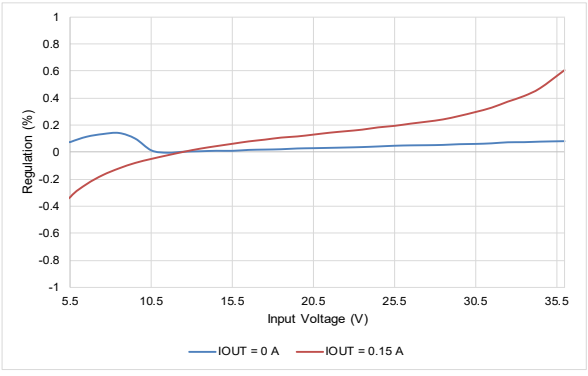
Efficency vs. Load Current
$V_{OUT} = 5.0$ V, $f_{SW} = 400$ kHz



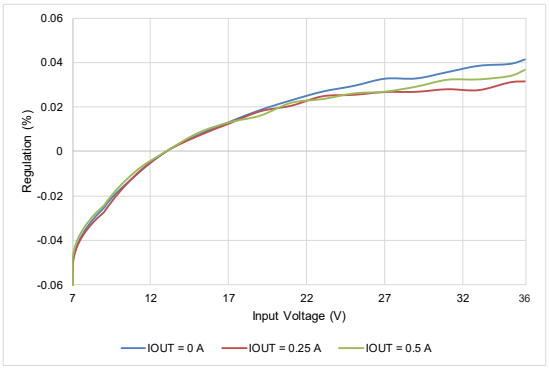
Load Regulation
$V_{OUT} = 3.3$ V, $f_{SW} = 2.15$ MHz, LP Mode



Load Regulation
$V_{OUT} = 5.0$ V, $f_{SW} = 400$ kHz, PWM Mode



Line Regulation
$V_{OUT} = 3.3$ V, $f_{SW} = 2.15$ MHz, LP Mode



Line Regulation
$V_{OUT} = 5.0$ V, $f_{SW} = 400$ kHz, PWM Mode

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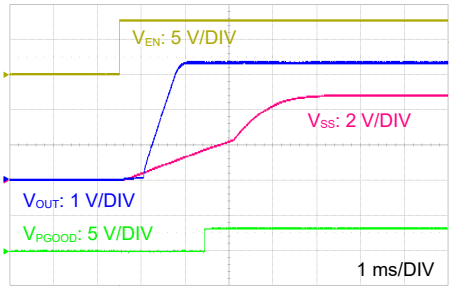
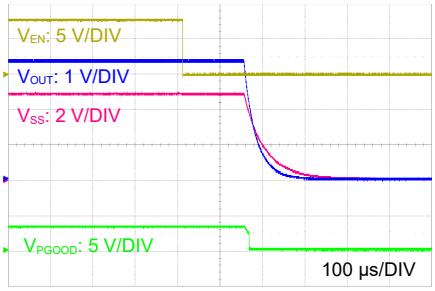
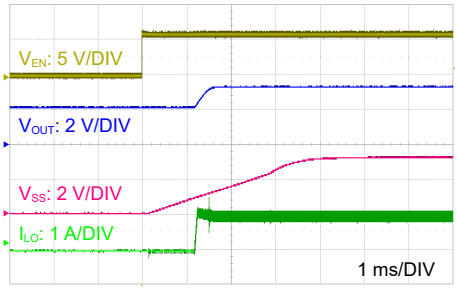


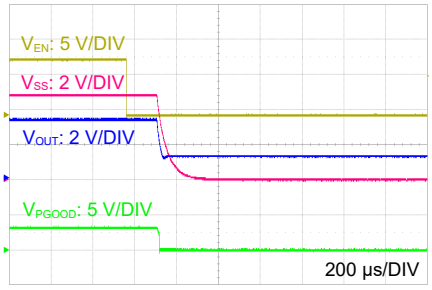
Start-up with EN rising
V_{OUT} = 3.3 V, I_{OUT} = 1.0 A, PWM Mode



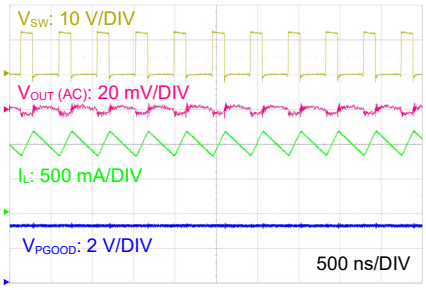
Shut-down with EN falling
V_{OUT} = 3.3 V, I_{OUT} = 1.0 A, PWM Mode



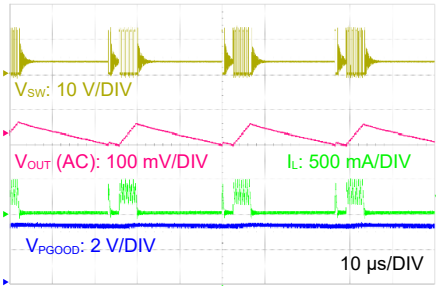
Pre-bias Start-up with EN rising
V_{OUT} = 3.3 V, I_{OUT} = 1.0 A, PWM Mode



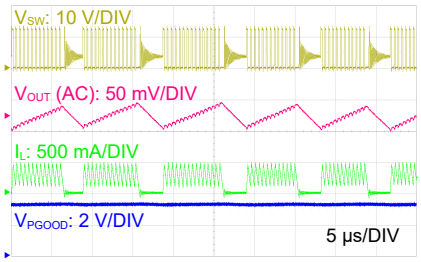
Pre-bias Shut-down with EN falling
V_{OUT} = 3.3 V, I_{OUT} = 1.0 A, PWM Mode



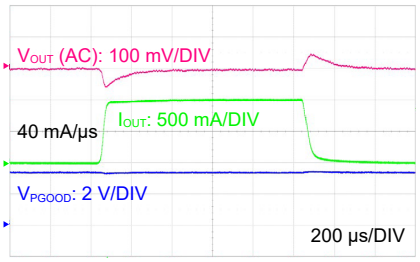
Steady-State Performance
V_{OUT} = 3.3 V, I_{OUT} = 1.0 A, PWM Mode



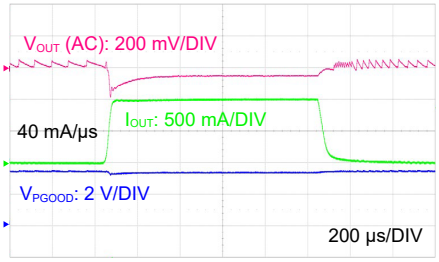
Steady-State Performance
V_{OUT} = 3.3 V, I_{OUT} = 10 mA, LP Mode



Steady-State Performance
V_{OUT} = 3.3 V, I_{OUT} = 100 mA, LP Mode



Load Transient Performance
V_{OUT} = 3.3 V, PWM Mode



Load Transient Performance
V_{OUT} = 3.3 V, LP Mode

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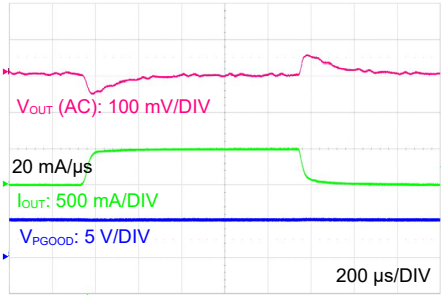
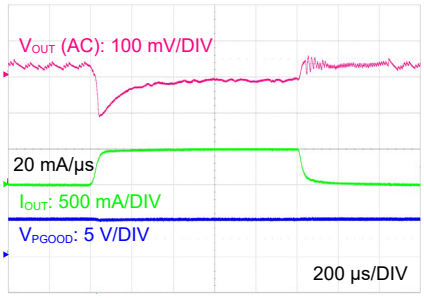
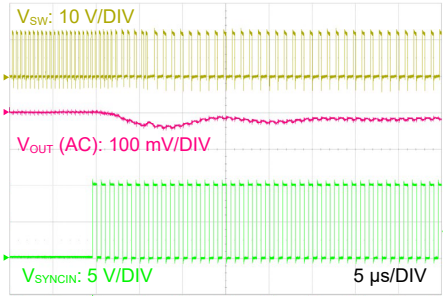


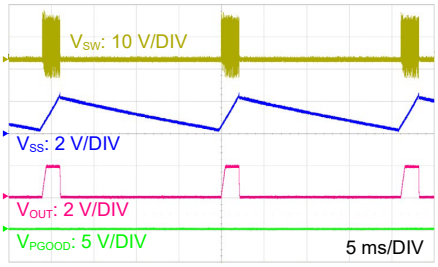
Load Transient Performance
V_{OUT} = 5.0 V, PWM Mode



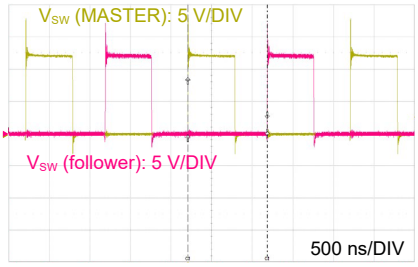
Load Transient Performance
V_{OUT} = 5.0 V, LP Mode



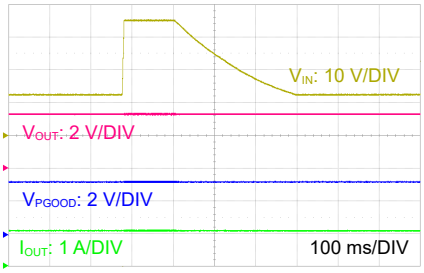
External Clock Synchronization
V_{OUT} = 3.3 V, f_{SW} = 2.15 MHz, f_{EXT} = 1 MHz



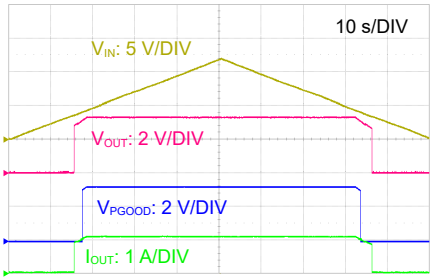
Output Short Protection
V_{OUT} = 3.3 V, PWM Mode



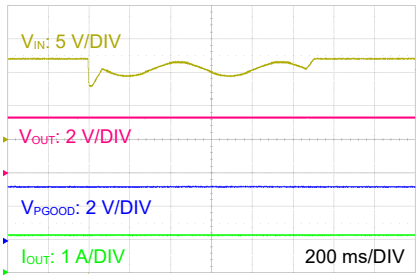
Interleaved Clock Generation
V_{OUT} = 5.0 V, f_{SW} = 500 kHz, PWM Mode



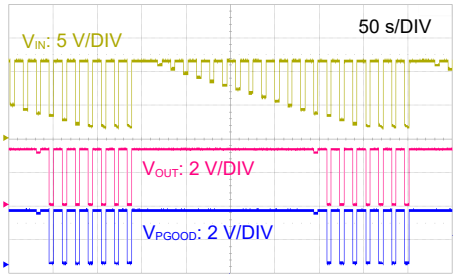
ISO 16750-2: Load Dump Pulse
V_{OUT} = 3.3 V, I_{OUT} = 1.0A, PWM Mode



V_{IN} Slow Ramp Up and Ramp Down
V_{OUT} = 3.3 V, I_{OUT} = 1.0 A, PWM Mode



ISO 16750-2: Level 1 Starting Profile
V_{OUT} = 3.3 V, I_{OUT} = 1.0 A, PWM Mode



ISO 16750-2: Reset Voltage Profile
V_{OUT} = 3.3 V, I_{OUT} = 1.0 A, PWM Mode

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FUNCTIONAL DESCRIPTION

Overview

The ARG81800 is a wide input voltage (3.5 to 36 V) synchronous PWM buck regulator that integrates low $R_{DS(on)}$ high-side and low-side N-channel MOSFETs. The ARG81800 employs peak current mode control to provide superior line and load regulation, cycle-by-cycle current limit, fast transient response, and simple compensation. The features of the ARG81800 include ultralow I_Q LP mode, extremely low minimum on-time, maximized duty cycle for low dropout operation, soft recovery from dropout condition, and pre-bias startup capability.

Protection features of the ARG81800 include VIN undervoltage lockout, cycle-by-cycle overcurrent protection, BOOT overvoltage and undervoltage protection, hiccup mode short circuit protection, overvoltage protection, and thermal shutdown. In addition, the ARG81800 provides open circuit, adjacent pin short circuit, and pin-to-ground short circuit protection.

Reference Voltage

The ARG81800 incorporates an internal precision reference that allows output voltages as low as 0.8 V. The accuracy of the internal reference is ±1.5% across –40°C to 150°C. The output voltage of the regulator is programmed with a resistor divider between VOUT and the FB pin of the ARG81800.

Internal VREG Regulator

VREG is used as the power supply for internal control circuitry and a low-side MOSFET driver. The ARG81800 consists of two internal low dropout regulators, VIN LDO and Bias LDO, to generate VREG voltage. VIN LDO is powered from input voltage to generate 4.8 V for VREG supply. Bias LDO uses the BIAS pin as a supply to generate VREG voltage. When voltage at the BIAS pin exceeds 3.0 V, VIN LDO is deactivated and Bias LDO generates the VREG voltage. Bias LDO can be made more efficient than VIN LDO by providing an external voltage at the BIAS pin that is less than the input voltage. If the output voltage of the ARG81800 is programmed to be greater than 3.1 V, it is recommended to supply the output voltage to the BIAS pin to improve the efficiency of the regulator.

Oscillator/Switching Frequency

The PWM switching frequency of the ARG81800 is adjustable from 250 kHz to 2.4 MHz by programming the internal clock frequency of the oscillator by connecting an FSET resistor from the FSET pin to GND. The internal clock has an accuracy of about ±10% over the operating temperature range. Usually, an FSET resistor with ±1% tolerance is recommended. A graph of switching frequency versus FSET resistor value is shown in the Design and Component Selection section. The ARG81800 will suspend operation if the FSET pin is shorted to GND or left open.

Synchronization ($SYNC_{IN}$) and Clock Output (CLK_{OUT})

The Phase-Locked Loop (PLL) in the ARG81800 allows its internal oscillator to be synchronized to an external clock applied on the $SYNC_{IN}$ pin. If the $SYNC_{IN}$ pin is driven by an external clock, the ARG81800 will be forced to operate in PWM mode, with synchronized switching frequency, overriding the mode selection on the PWM/AUTO pin. The external clock must also satisfy the pulse width, duty cycle, and rise/fall time requirements shown in the Electrical Characteristics table. If the $SYNC_{IN}$ pin is continuously pulled high, the ARG81800 outputs a 180-degree phase-shifted internal oscillator clock on the CLK_{OUT} pin, so “downstream” ARG81800 devices can be easily interleaved via their synchronization inputs. Figure 1 shows the usage of multiple ARG81800 devices in master-follower configuration. If the $SYNC_{IN}$ pin is continuously pulled low, the device disables the CLK_{OUT} pin.

Frequency Dither

In addition to EMI-aware PCB layout, extensive filtering, controlled switch node transitions, and shielding, switching frequency dithering is an effective way to mitigate EMI concerns in switching power supplies. Frequency dither helps to minimize peak emissions by spreading the emissions across a wide range of frequencies. The ARG81800 provides frequency dither by spreading the switching frequency ±5% using a triangular modulated wave of 0.5% switching frequency.

The ARG81800 is capable of adding dither to the external clock applied on the $SYNC_{IN}$ pin. This unique feature allows the minimizing of electromagnetic emissions even when the device is using external clock. Frequency dither scheme can be disabled by connecting the CLK_{OUT} pin to VREG pin. In master-follower configuration, the CLK_{OUT} pin of the follower device should be connected to VREG to avoid double-dithering.

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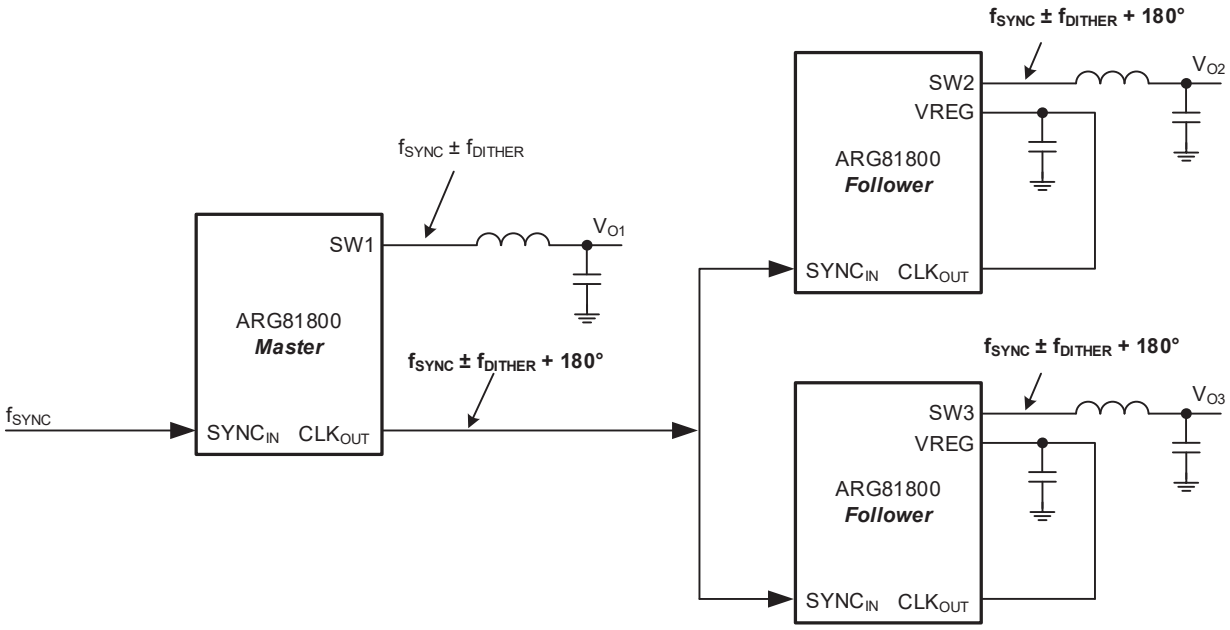

Figure 1: Master-Follower Configuration

Table 1: PWM Frequency, CLKOUT, and Dithering Settings

Device	$SYNC_{IN}$	PWM Frequency and Dithering			CLK_{OUT} Frequency and Dithering		
		SW Frequency	Magnitude of Dithering	Dither Modulation Frequency	Frequency	Magnitude of Dithering	Dither Modulation Frequency
ARG81800/ ARG81800-1	Low	f_{SW}	±0.05 × f_{SW}	0.005 × f_{SW}	Disabled/Off	None	None
	High	f_{SW}			f_{SW} + 180°	±0.05 × f_{SW}	0.005 × f_{SW}
	f_{SYNC}	f_{SYNC}	±0.05 × f_{SW}	0.005 × f_{SW}	f_{SYNC} + 180°	±0.05 × f_{SYNC}	0.005 × f_{SYNC}

Transconductance Error Amplifier

The transconductance error amplifier's primary function is to control the regulator's output voltage. The error amplifier is a three-terminal input device with two positive inputs and one negative input, as shown in Figure 2. The negative input is simply connected to the FB pin and is used to sense the feedback voltage for regulation. The error amplifier performs an "analog OR" selection between its positive inputs and operates according to the positive input with the lowest potential. The two positive inputs are used for soft-start and steady-state regulation. The error amplifier regulates to the soft-start pin voltage minus 400 mV during startup and to the internal reference (VREF) during normal operation.

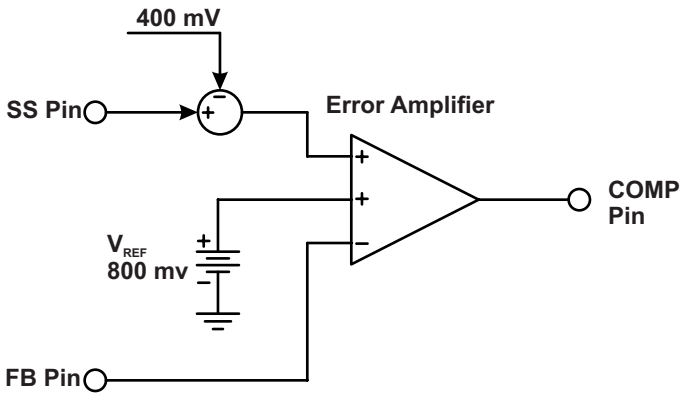

Figure 2: ARG81800 Error Amplifier

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Compensation Components

To stabilize the regulator, a series RC compensation network (R_Z and C_Z) must be connected from the output of the error amplifier (COMP pin) to GND as shown in the applications schematic. In most instances, an additional low-value capacitor (C_P) should be connected in parallel with the R_Z-C_Z compensation network to reduce the loop gain at very high frequencies. However, if the C_P capacitor is too large, the phase margin of the converter may be reduced. Calculation of R_Z, C_Z, and C_P is covered in the Component Selection section of this datasheet. If a fault occurs or the regulator is disabled, the COMP pin is pulled to GND via the approximately 1 kΩ internal resistor and PWM switching is inhibited.

Power MOSFETs

The ARG81800 includes a 500 mΩ, high-side N-channel MOSFET and a 210 mΩ, low-side N-channel MOSFET to provide synchronous rectification. When the ARG81800 is disabled via the EN input being low or a fault condition, its output stage is tri-stated by turning off both the upper and lower MOSFETs.

BOOT Regulator

The ARG81800 includes a BOOT regulator to supply the power for a high-side MOSFET gate driver. The voltage across the BOOT capacitor is typically 4.8 V. If the BOOT capacitor is missing, the device will detect a BOOT overvoltage. Similarly, if the BOOT capacitor is shorted, the ARG81800 will detect a BOOT undervoltage. Also, the BOOT regulator has a current limit to protect itself during a short-circuit condition.

Soft Start (Startup) and Inrush Current Control

The soft start function controls the inrush current at startup. The soft start pin (SS) is connected to GND via a capacitor. When the ARG81800 is enabled and all faults are cleared, the SS pin sources the charging current I_{SS} and the voltage on the soft start capacitor C_{SS} starts ramping upward from 0 V. When the voltage at the soft start pin exceeds the soft start offset voltage (SS Offset), typically 400 mV, the error amplifier will ramp up its output voltage above the PWM Ramp Offset. At this instant, the top and bottom MOSFETs will begin switching. There is a small delay (t_{dSS}) from the moment EN pin transitioning high to the moment soft start voltage reaching 400 mV to initiate PWM switching.

Immediately after the start of PWM switching, the error amplifier will regulate the voltage at the FB pin to the soft start pin voltage minus approximately 400 mV. During the active portion of soft start, the voltage at the SS pin will rise from 400 mV to 1.2 V (a difference of 800 mV), the voltage at the FB pin will rise from 0 V to 800 mV, and the regulator output voltage will rise from 0 V to the set voltage determined by the feedback resistor divider.

During startup, PWM switching frequency is reduced to 25% of f_{SW} while FB is below 200 mV. If FB voltage is above 200 mV but below 400 mV, the switching frequency is 50% of f_{SW}. At the same time, the transconductance of the error amplifier, gm, is reduced to half of nominal value when FB is below 400 mV. When FB is above 400 mV, the switching frequency will be f_{SW} and the error amplifier gain will be the nominal value. The reduced switching frequency and error amplifier gain are necessary to help improve output regulation and stability when V_{OUT} is very low. During low V_{OUT}, the PWM control loop requires on-time near the minimum controllable on-time and very low duty cycles that are not possible at the nominal switching frequency.

When the voltage at the soft start pin reaches approximately 1.2 V, the error amplifier will switch over and begin regulating the voltage at the FB pin to the fixed internal bandgap reference voltage of 800 mV. The voltage at the soft start pin will continue to rise to the internal LDO regulator output voltage. If the ARG81800 is disabled or a fault occurs, the internal fault latch is set and the capacitor at the SS pin is discharged to ground very quickly through a 2 kΩ pull-down resistor. The device will clear the internal fault latch when the voltage at the SS pin decays to approximately 200 mV. However, if the device enters hiccup mode, the capacitor at the SS pin is slowly discharged through a current sink, I_{HIC}. Therefore, the soft start capacitor C_{SS} not only controls the startup time but also the time between soft start attempts in hiccup mode.

Slope Compensation

The ARG81800 incorporates internal slope compensation that ensures stable operation at PWM duty cycles above 50% for a wide range of input/output voltages, switching frequencies, and inductor values. As shown in the functional block diagram, the slope compensation signal is added to the sum of the current sense and PWM Ramp Offset. The relationship between slope compensation and adjustable switching frequency is given by

Equation 1:

$$S_E = 12.84 / (37.037 / f_{SW} - 3)$$

where f_{SW} is switching frequency in MHz and S_E is slope compensation in A/µs. Internal slope compensation in ARG81800-1 is half of that (Equation 1) in ARG81800.

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Pre-Biased Startup

If the output of the buck regulator is pre-biased at a certain output voltage level, the ARG81800 will modify the normal startup routine to prevent discharging the output capacitors. As described in the Soft Start (Startup) and Inrush Current Control section, the error amplifier usually becomes active when the voltage at the soft start pin exceeds 400 mV. If the output is pre-biased, the voltage at the FB pin will be non-zero. The device will not start switching until the voltage at SS pin rises to approximately V_{FB} + 400 mV. From then on, the error amplifier becomes active, the voltage at the COMP pin rises, PWM switching starts, and V_{OUT} will ramp upward from the pre-bias level.

Dropout

The ARG81800 is designed to operate at extremely wide duty cycles to minimize any reduction in output voltage during dropout conditions (difference between input and output voltage drops to a minimum value) such as cold crank. During dropout, if the minimum off-time (85 ns typical) is reached for more than 5 consecutive switching cycles, the programmed switching frequency f_{SW} is reduced by a factor of 4 and the off-time is extended to 115 ns (typical). While operating with reduced frequency, if the device further reaches minimum off-time (115 ns typical) for more than 35 consecutive switching cycles, it continues to operate with reduced frequency. Otherwise, the device toggles back to the programmed switching frequency f_{SW}. In addition, during dropout operation, the soft start capacitor C_{SS} will discharge so that if the input voltage increases, the output voltage recovers with a slew rate set by the soft start ramp.

PGOOD Output

The ARG81800 provides a Power Good (PGOOD) status signal to indicate if the output voltage is within the regulation limits. Since the PGOOD output is an open-drain output, an external pull-up resistor must be used as shown in the applications schematic. PGOOD transitions high when the output voltage, sensed at the FB pin, is within regulation.

During start-up, PGOOD signal exhibits an additional delay of $t_{dPG(SU)}$ after FB pin voltage reaches the regulation voltage. This delay helps to filter out any glitches on the FB pin voltage.

The PGOOD output is pulled low if either an undervoltage or overvoltage condition occurs or the ARG81800 junction temperature exceeds thermal shutdown threshold (T_{SD}). The PGOOD overvoltage and undervoltage comparators incorporate a small amount of hysteresis ($V_{FB(OV,HYS)}$, $V_{FB(UV,HYS)}$) to prevent chattering and deglitch filtering ($t_{dPG(UV)}$, $t_{dPG(OV)}$) to eliminate false triggering. For other faults, PGOOD depends on the output voltage.

It is important that the correct status of PGOOD is reported during either the input supply ramp up or ramp down. During a supply ramp up, the PGOOD is designed to operate in the correct state from a very low input voltage. Also, during supply ramp down, the PGOOD is designed to operate in the correct state down to a very low input voltage.

Current Sense Amplifier

The ARG81800 incorporates a high-bandwidth current sense amplifier to monitor the current through the top MOSFET. This current signal is used to regulate the peak current when the top MOSFET is turned on. The current signal is also used by the protection circuitry for the cycle-by-cycle current limit and hiccup mode short circuit protection

Pulse-Width Modulation (PWM)

The ARG81800 employs fixed-frequency, peak current mode control to provide excellent load and line regulation, fast transient response, and simple compensation. A high-speed comparator and control logic is included in the ARG81800. The inverting input of the PWM comparator is connected to the output of the error amplifier. The non-inverting input is connected to the sum of the current sense signal, the slope compensation signal, and a DC PWM Ramp offset voltage (Ramp Offset).

At the beginning of each PWM cycle, the CLK signal sets the PWM flip flop, the bottom MOSFET is turned off, the top MOSFET is turned on, and the inductor current increases. When the voltage at the non-inverting of PWM comparator rises above the error amplifier output COMP, the PWM flip flop is reset, the top MOSFET is turned off, the bottom MOSFET is turned on, and the inductor current decreases. Since the PWM flip flop is reset, the dominant error amplifier may override the CLK signal in certain situations.

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Low-Power (LP) Mode

The ARG81800 operates in ultralow I_Q LP mode when PWM/AUTO pin is pulled to logic low. If the PWM/AUTO pin transitions from logic high to logic low while output is in regulation, the device waits for 7 clock cycles before entering the LP mode. This delay provides adequate filtering to ensure no noise transients forces the device to erroneously enter LP mode.

When LP mode is selected, the ARG81800 operates in continuous conduction PWM Mode until peak inductor current decreases to $I_{PEAK(LP)}$. When peak inductor current falls below $I_{PEAK(LP)}$, the LP comparator monitors FB node and regulates the output voltage in hysteretic manner. The reference for the LP comparator is calibrated approximately 0.5% above the PWM regulation point. The transition point from PWM to LP mode is defined by the input voltage, output voltage, and inductor value. The exact operation of the ARG81800 in LP mode is described below.

When voltage on the COMP pin falls to the voltage corresponding to the ultralow I_Q peak current threshold value, an internal clamp prevents the COMP voltage from falling further. This results in a momentary rise in the FB voltage beyond LP comparator upper threshold which causes the LP comparator to trip. Once the LP comparator trips, the device enters coast period during which MOSFET switching is terminated and the associated control circuitry is also shut down. This ensures a very low quiescent current is drawn from the input.

The coast period terminates once the FB voltage falls below the LP comparator lower threshold. The device will fully power-up approximately after a 2.5 µs delay and the high-side MOSFET is repeatedly turned on, operating at the PWM switching frequency until the voltage at the FB pin rises again above the LP comparator threshold. The rate of rise of output voltage is determined by the input voltage, output voltage, inductor value, output capacitance, and load.

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Protection Features

The ARG81800 was designed to satisfy the most demanding automotive and non-automotive applications. In this section, a description of each protection feature is described and Table 2 summarizes the protections and their operation.

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout (UVLO) comparator in the ARG81800 monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the start threshold ($V_{INUV(ON)}$, V_{IN} rising) or the stop threshold ($V_{INUV(OFF)}$, V_{IN} falling). The UVLO comparator incorporates some hysteresis ($V_{INUV(HYS)}$) to help prevent on-off cycling of the regulator due to resistive or inductive drops in the V_{IN} path during heavy loading or during startup.

PULSE-BY-PULSE PEAK CURRENT PROTECTION (PCP)

The ARG81800 monitors the current in the high-side MOSFET, and if the peak MOSFET current exceeds the pulse-by-pulse overcurrent limit I_{LIMHSx}, the upper MOSFET is turned off and the bottom MOSFET is turned on until the start of the next clock pulse from the oscillator. The device includes leading edge blanking to prevent false triggering of pulse-by-pulse current protection when the upper MOSFET is turned on.

Because of the addition of the slope compensation ramp to the sensed inductor current, the ARG81800 can deliver more current at minimum duty cycle and less current at maximum duty cycle. Figure 3 illustrates the relationship between the high-side MOSFET peak current limit and duty cycle. As shown, the peak current limit at minimum and maximum duty cycle remains fixed, but the relationship versus duty cycle is skewed with frequency due to the fixed minimum off-time. Given the relationship, it is best to use the $I_{HSPKMIND}$ and $I_{HSPKMAXD}$ current limits to calculate the current limit at any given duty cycle.

During synchronization, slope compensation scales in a similar fashion as with R_{FSET} although with slightly less accuracy. The exact current the buck regulators can support is heavily dependent on duty cycle (V_{IN}, V_{OUT}), ambient temperature, thermal resistance of the PCB, airflow, component selection, and nearby heat sources.

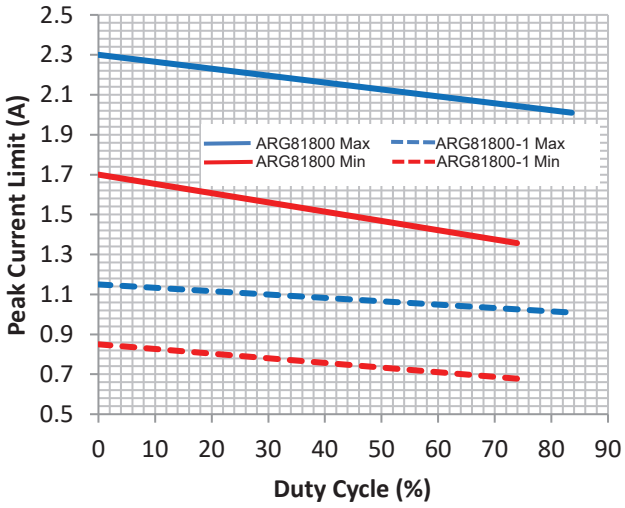

Figure 3: Peak Current Limit vs. Duty Cycle

OVERCURRENT PROTECTION (OCP) AND HICCUP MODE

An OCP counter and hiccup mode circuit protect the buck regulator when the output of the regulator is shorted to ground or when the load is too high. When the soft-start ramp is active ($t < t_{ss}$), the OCP hiccup counter is disabled. The following two conditions must be met for the OCP counter to be enabled and begin counting:

- SS pin voltage, $V_{SS} > V_{HIC/LP(EN)}$ (2.3 V), and
- Comp pin voltage, V_{COMP} clamped at its maximum voltage (OCP = 1)

As long as these two conditions are met, the OCP counter remains enabled and will count pulses from the overcurrent comparator. If the COMP voltage decreases (OCP = 0), the OCP counter is cleared. Otherwise, if the OCP counter reaches HIC_{OCP} clock counts (120), PWM switching ceases, a hiccup latch is set, and the COMP pin is quickly pulled down by a relatively low resistance (1 kΩ). The hiccup latch also enables a small current sink connected to the SS pin (I_{HIC}). This causes the voltage at the soft start pin to slowly ramp downward. When the voltage at the soft start pin decays to a low enough level (V_{SSRST}, 200 mV), the hiccup latch is cleared, and the current sink is turned off. At

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this instant, the SS pin will begin to source current (I_{SS}) and the voltage at the SS pin will ramp upward. This marks the beginning of a new, normal soft start cycle as described earlier. When the voltage at the soft start pin exceeds the error amp voltage by approximately 400 mV, the error amplifier will force the voltage at the COMP pin to quickly slew upward and PWM switching will resume.

If the short circuit/overload at the regulator output persists, another hiccup cycle will occur. Hiccups will repeat until the short circuit/overload is removed or the converter is disabled. If the short circuit/overload is removed, the device will soft start normally and the output voltage will automatically recover to the desired level. Thus, hiccup mode is a very effective protection for the short-circuit/overload condition. It avoids false trigger during short duration short-circuit/overload. On the other hand, for the extended short-circuit/overload duration, the reduced average power dissipation with hiccup mode of operation helps in lowering the temperature rise of the device and enhancing the system reliability.

Note that OCP is the only fault that results in hiccup mode being ignored while V_{SS} < 2.3 V.

BOOT CAPACITOR PROTECTION

The ARG81800 monitors the voltage across the BOOT capacitor to detect if the BOOT capacitor is missing or short-circuited. If the BOOT capacitor is missing, the regulator enters hiccup mode after 7 clock counts. If the BOOT capacitor is shorted, the device enters hiccup mode after 120 clock counts. Also, the boot regulator has a current limit to protect itself during a short-circuit condition.

For a boot fault, hiccup mode operates virtually the same as described previously for overcurrent protection (OCP), with soft start ramping up and down for repeated hiccups. Boot faults are non-latched faults, so the device will automatically recover when the fault is removed.

OVERVOLTAGE PROTECTION (OVP)

The ARG8100 consists of an always-on overvoltage protection circuit that monitors output overvoltage on the BIAS pin, perhaps caused by the FB pin pulled to ground, high-side MOSFET leakage current, or line/load transients. During an overvoltage fault caused by any of the above events, the controller tries to reduce the output overvoltage by terminating the high-side MOSFET switching and pulsing the low side MOSFET with minimum off-time (t_{OFFmin}) until FB returns to regulation. The ARG81800 waits for $t_{dPG(OV)}$ (120) clock counts before pulling the PGOOD low. If the overvoltage fault is not cleared even beyond $t_{dPG(OV)}$, PGOOD is pulled low and the device continuously attempts to reduce the output overvoltage. The output overvoltage protection threshold, at any given time, varies with the voltage on the feedback node as shown in Figure 4. If the BIAS pin is connected to VOUT, the maximum settable output voltage is limited to 20 V.

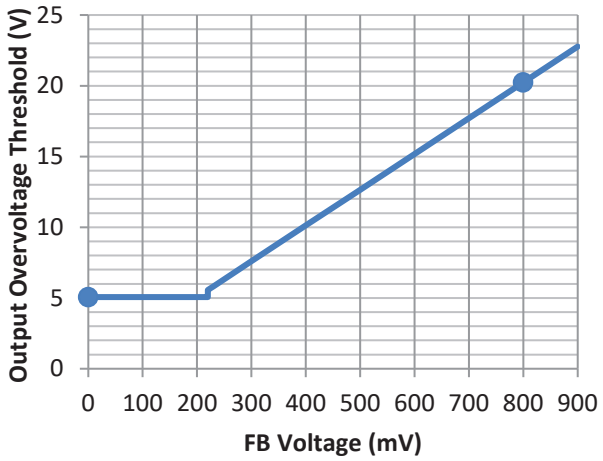

Figure 4: Output Overvoltage Threshold Variation with Increasing Feedback Voltage

SW PIN PROTECTION

Unlike most regulators, the ARG81800 protects itself when the SW pin is shorted to ground. If the SW pin is shorted to ground, there will be a very high current in the high-side MOSFET when it is turned on. The ARG81800 incorporates an internal secondary current protection to detect this unusually high current and turns off the high-side MOSFET if the high current persists for more than two consecutive switching cycles. After turning off the high-side MOSFET, the device enables the hiccup latch and attempts to restart after hiccup latch is cleared. If the short to ground is removed, the regulator will automatically recover; otherwise, the device continues hiccupping. Unlike other hiccup mode protections, the SW pin protection is not delayed until soft start is completed, i.e., V_{SS} > 2.3 V.

PIN-TO-GROUND AND PIN-TO-PIN SHORT PROTECTIONS

The ARG81800 is designed to satisfy the most demanding automotive applications. For example, the device has been carefully designed to withstand a short circuit to ground at each pin without causing any damage to the IC.

In addition, care was taken when defining the device pinouts to optimize protection against pin-to-pin adjacent short circuits. For

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example, logic pins and high-voltage pins are separated as much as possible. Inevitably, some low-voltage pins are located adjacent to high voltage pins, but in these instances, the low voltage pins are designed to withstand increased voltages, with clamps and/or series input resistance, to prevent damage to the device.

THERMAL SHUTDOWN (TSD)

The ARG81800 monitors internal junction temperature and shuts down the IC by disabling the switching pulses of high- and low-side MOSFETs if the junction temperature exceeds the Thermal Shutdown Threshold T_{TSD}. Also, to prepare for a restart, the internal soft-start voltage (V_{SS}) and the voltage at the COMP pin are pulled low until $V_{SS} < V_{SSRST}$. TSD is a non-latched fault, so the device automatically recovers if the junction temperature decreases by approximately 20°C.

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Table 2: Summary of ARG81800 Fault Modes and Operation

Fault Mode	Internal Soft Start	During Fault Counting, before Hiccup Mode			BOOT Charging	PGOOD State	Latched Fault	Reset Condition
		V_{COMP}	High-Side MOFSET	Low-Side MOFSET				
V_{IN} undervoltage	Pulled low via 2 kΩ resistor, No Hiccup	Pulled low via 1 kΩ resistor, No Hiccup	Forced Turn-off	Forced Turn-off	Disabled	Depends on V_{REG}	NO	Automatic, V_{IN} above UVLO start threshold
Output shorted to ground	Hiccup, after 120 OCP clock counts	Clamped to I_{LIMHS}, then pulled low for Hiccup	f_{SW} / 4 due to V_{OUT} < 25%, responds to V_{COMP}	Turned on if BOOT voltage is too low	Not affected	Depends on V_{OUT}	NO	Automatic, Short removed
Output overcurrent, V_{OUT} > 50%	Hiccup, after 120 OCP clock counts	Clamped to I_{LIMHS}, then pulled low for Hiccup	f_{SW} responds to V_{COMP}	Turned on if BOOT voltage is too low	Not affected	Depends on V_{OUT}	NO	Automatic, Load current decreased
High-side MOSFET overcurrent (SW short to GND)	Hiccup, after 2 clock count	Pulled low via 1 kΩ resistor for hiccup	Forced Turn-off	Forced Turn-off	Not affected	Depends on V_{OUT}	NO	Automatic, Short removed
Boot capacitor open/missing	Hiccup, after 7 clock counts	Pulled low via 1 kΩ resistor for hiccup	Forced Turn-off	Turned off when fault occurs	Disabled when fault occurs	Depends on V_{OUT}	NO	Automatic, Boot capacitor replaced
Boot capacitor shorted (BOOTUV)	Hiccup, after 120 clock counts	Pulled low via 1 kΩ resistor for hiccup	Forced Turn-off	Turned off only during hiccup	Disabled only during hiccup	Depends on V_{OUT}	NO	Automatic, Short removed
Output overvoltage	Not affected	Transitions low via loop response	Turned-off by low V_{COMP}	Pulsed with Minimum off-time	Disabled when V_{FB} is too high	Pulled low when V_{FB} is too high	NO	Automatic, After V_{FB} returns to normal range
Output undervoltage	Not affected	Transitions high via loop response	Active, Responds to V_{COMP}	Turned on if BOOT voltage is too low	Not affected	Pulled low when V_{FB} is too low	NO	Automatic, After V_{FB} returns to normal range
FSET shorted to GND or above 1.0 V	Pulled Low	Pulled Low	Forced Turn-off	Forced Turn-off	Disabled	Depends on V_{OUT}	NO	Automatic
FB open	Not affected	Transitions low via loop response	Turned-off by low V_{COMP}	Pulsed with Minimum off-time	Disabled when V_{FB} is too high	Pulled low when V_{FB} is too high	NO	Automatic, After V_{FB} returns to normal range
Thermal shutdown (TSD)	Pulled low until V_{SS} < V_{SSRST} and TSD = 0	Pulled low until V_{SS} < V_{SSRST} and TSD = 0	Forced Turn-off	Forced Turn-off	Disabled	Pulled low	NO	Automatic, Part cools down

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APPLICATION INFORMATION

Design and Component Selection

PWM SWITCHING FREQUENCY (R_{FSET})

The PWM switching frequency is set by connecting a resistor from the FSET pin to signal ground. Figure 5 shows the relationship between the typical switching frequency (y-axis) and the FSET resistor (x-axis). For a required switching frequency (f_{SW}), the FSET resistor value can be calculated as follows:

Equation 2:

$$R_{FSET} = \frac{37037}{f_{SW}} - 2.96$$

where f_{SW} is in kHz and R_{FSET} is in kΩ.

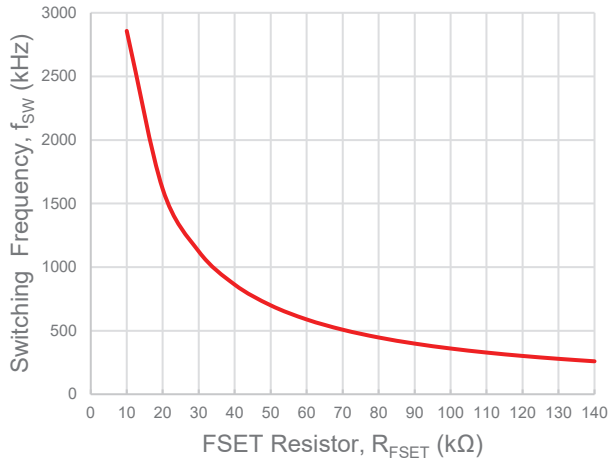

Figure 5: PWM Switching Frequency vs. R_{FSET}

While choosing the PWM switching frequency, the designer should be aware of the minimum controllable on-time, $t_{ON(MIN)}$, of the ARG81800. If the required on-time of the system is less than the minimum controllable on-time, pulse skipping will occur and the output voltage will have increased ripple. The PWM switching frequency should be calculated using Equation 3, where V_{OUT} is the output voltage, $t_{ON(MIN)}$ is the minimum controllable on-time of the device (see EC table), and $V_{IN(MAX)}$ is the maximum required operational input voltage (not the peak surge voltage).

Equation 3:

$$f_{SW} < \frac{V_{OUT}}{t_{ON(MIN)} \times V_{IN(MAX)}}$$

If an external clock f_{SYNC} is used for synchronization, the base switching frequency should be chosen such that pulse skipping will not occur at the maximum synchronized switching frequency (i.e., $1.5 \times f_{SYNC}$ should be less than the frequency f_{SW} in Equation 3).

OUTPUT VOLTAGE SETTING

The output voltage of the ARG81800 is determined by connecting a resistive feedback divider (R_{FB1}, R_{FB2}) from the output node (V_{OUT}) to the FB pin as shown in Figure 6. The feedback resistors must satisfy the ratio shown in Equation 4 below to produce the desired output voltage (V_{OUT}).

Equation 4:

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT}}{0.8} - 1.0$$

1% resistors are recommended to maintain the output voltage accuracy. There are tradeoffs while choosing the value of the feedback resistors. If the series combination ($R_{FB1} + R_{FB2}$) is too low, the light load efficiency of the regulator will be reduced. So to maximize the efficiency, it is best to choose large values for feedback resistors. On the other hand, large values of feedback resistors increases the parallel combination (R_{FB1}//R_{FB2}) and makes the regulator more susceptible to noise coupling onto the FB pin.

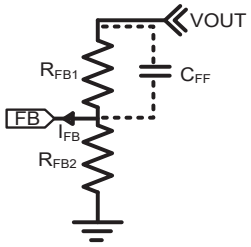

Figure 6: Feedback Divider with Feedforward Capacitor

Large values of R_{FB1} also impact the output voltage accuracy of the regulator. A small amount of leakage current I_{FB} flowing into the FB pin increases the output voltage beyond the set regulation voltage. The output voltage of the regulator considering the FB pin leakage current is given by:

Equation 5:

$$V_{OUT} = 0.8 \times (1 + \frac{R_{FB1}}{R_{FB2}}) + I_{FB} \times R_{FB1}$$

FB pin leakage current increases the output voltage beyond the set regulation voltage by an amount of I_{FBRFB1}. The larger the value of R_{FB1}, the larger is the inaccuracy in the output voltage. A feedforward capacitor (C_{FF}) can be connected in parallel with

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R_{FB1} to increase phase margin and loop crossover frequency for improving transient response of the regulator. Addition of C_{FF} results in an additional zero and pole in the compensation network and boosts the loop phase at the crossover frequency. In general, C_{FF} should be less than 25 pF. While large value of C_{FF} increases the loop crossover frequency and reduces the phase margin, very small value of C_{FF} will not have any effect. Optimal value of C_{FF} can be calculated from the below equation.

Equation 6:

$$C_{FF} = \frac{1}{2 \times \pi \times R_{FB1} \times f_C}$$

OUTPUT INDUCTOR (L_O)

The ARG81800 incorporates a peak current mode control technique for closed-loop regulation of the output voltage. It is common knowledge that, without adequate slope compensation, a peak current mode controlled regulator will become unstable when duty cycle is near or above 50%. Hence, to stabilize the regulator over the complete range of its operating duty cycle, the ARG81800 employs a fixed internal slope compensation (S_E). Many factors determine the selection of output inductor, such as switching frequency, output/input voltage ratio, transient response, and ripple current. A larger value inductor will result in less ripple current, which also results in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current.

A good rule of thumb for determining the output inductor is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum output current ($I_{OUT(MAX)}$). The inductance value can be calculated from the following equation:

Equation 7:

$$L_O = \frac{V_{OUT}}{f_{SW} \times \Delta I_{LO}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where ΔI_{LO} is the peak-to-peak inductor ripple current, which is $0.3 \times I_{OUT(MAX)}$.

A second constraint on inductor value arises from the loop stability at duty cycles greater than 50%. Although slope compensation is primarily required to avoid subharmonic oscillations, the inductor value calculated from the formula derived by Dr. Ridley, given below in Equation 8, can critically damp the pole pair at half the switching frequency.

Equation 8:

$$L_O \geq \frac{V_{OUT}}{S_E} \times \left(1 - 0.18 \times \frac{V_{OUT}}{V_{IN(MIN)}}\right)$$

where L_O is output inductance in µH and S_E is external slope compensation provided in the Electrical Characteristics table.

To avoid dropout, $V_{IN(MIN)}$ must be approximately 1 to 1.5 V above V_{OUT}. Choose output inductor such that its inductance is greater than the maximum of inductance values calculated in Equation 7 and Equation 8. However, absolute maximum inductance should not exceed $1.1 \times V_{OUT} / S_{E(min)}$.

The saturation current of the inductor should be higher than the peak current capability of the ARG81800. Ideally, for output short-circuit conditions, inductor should not saturate, given the highest peak current limit (I_{LIMHSx}) at minimum duty cycle. At the very least, the output inductor should not saturate with the peak operating current according to the following equation:

Equation 9:

$$I_{SAT\_Lo} > I_{LIMHSx(MAX)} - \left(\frac{S_E \times V_{OUT}}{1.15 \times f_{SW} \times V_{IN(MAX)}}\right)$$

where $t_{ON(MIN)}$ is the minimum on-time provided in the Electrical Characteristics table.

The typical DC output current capability of the regulator at any given duty cycle (D) is:

Equation 10:

$$I_{OUT(TYP)} = I_{LIMHSx(TYP)} - \frac{S_E \times D}{f_{SW}} - \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L_O}$$

After an inductor is chosen, it should be tested during output short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure neither the inductor nor the regulator are damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

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OUTPUT CAPACITORS (C_O)

The output capacitor of switching regulators filter the output voltage to provide an acceptable level of ripple on the output voltage, and they also store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{OUT}) is a function of the output capacitor parameters: C_O, ESR_{CO}, and ESL_{CO}:

Equation 11:

$$\Delta V_{OUT} = \Delta I_{LO} \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO} + \frac{\Delta I_{LO}}{8 \times f_{SW} \times C_O}$$

The type of output capacitors determine which terms of Equation 11 are dominant. For ceramic output capacitors, ESR_{CO} and ESL_{CO} are virtually zero, so the output voltage ripple will be dominated by the third term of Equation 11. The value of C_O can be calculated as:

Equation 12:

$$C_O \geq \frac{\Delta I_{LO}}{8 \times f_{SW} \times \Delta V_{OUT}}$$

Voltage ripple of a regulator using ceramic output capacitors can be reduced by increasing the total capacitance, reducing the inductor current ripple, or increasing the switching frequency. For electrolytic output capacitors, the value of capacitance will be relatively high, so the third term in Equation 11 will be very small and the output voltage ripple will be determined primarily by the first two terms:

Equation 13:

$$\Delta V_{OUT} = \Delta I_{LO} \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO}$$

Voltage ripple of a regulator using electrolytic output capacitors can be reduced by: decreasing the equivalent ESR_{CO} and ESL_{CO} by using a high quality capacitor, adding more capacitors in parallel, or reducing the inductor current ripple.

As the ESR of some electrolytic capacitors can be quite high, Allegro recommends choosing a quality capacitor for which the ESR or the total impedance is clearly documented in the capacitor datasheet. Also, ESR of electrolytic capacitors usually increases significantly at cold ambient temperatures, as much as 10 times, which increases the output voltage ripple and in most cases reduces the stability of the system.

The transient response of the regulator depends on the quantity and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (high di_O/dt), the change in the output voltage, using electrolytic output capacitors, is:

Equation 14:

$$\Delta V_{OUT} = \Delta I_{LO} \times ESR_{CO} + \frac{di_O}{dt} \times ESL_{CO}$$

When ceramic capacitors are used in the output, the output voltage deviation during load transients depends on the bulk output capacitance along with various other factors. To calculate the bulk ceramic capacitance required, the entire load transient duration can be divided into two stages: large signal and small signal. During large signal load transients, immediately after the transient event, the output voltage deviates from the nominal value due to large mismatch in the load current requirement and the inductor current. The output voltage deviation during this interval is maximum and depends on output inductor, bulk output capacitance, and closed-loop crossover frequency. For designs with higher crossover frequency, the controller typically saturates the duty cycle, i.e., either minimum or maximum. For a chosen output inductor and crossover frequency values, the output voltage deviation can be minimized by increasing the output bulk capacitance. In the case of a buck converter, operating with a low duty cycle, the step-down load transient is more severe and hence the output capacitance should be determined for this scenario. The bulk ceramic output capacitance required is given by:

Equation 15:

$$C_{O,bulk} = \frac{{\Delta I_O}^2 \times L_O}{2 \times V_{OUT} \times \Delta V_{OUT,spec}}$$

where ΔI_O is the magnitude of the change in the load current, $\Delta V_{OUT,spec}$ is the maximum allowed output voltage deviation during load transient event. Gradually, as the mismatch between the load current and the inductor current becomes small, the output voltage deviation also reduces, resembling a small signal transient event. Eventually, during small signal transient interval, the error amplifier brings the output voltage back to its nominal value. The speed with which the error amplifier brings the output voltage back into regulation depends mainly on the loop crossover frequency. A higher crossover frequency usually results in a shorter time to return to the nominal set voltage.

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OUTPUT VOLTAGE RIPPLE – ULTRALOW-I$_Q$ LP MODE

After choosing output inductor and output capacitor(s), it is important to calculate the output voltage ripple ($V_{PP(LP)}$) during ultralow-I_Q LP mode. With ceramic output capacitors, the output voltage ripple in PWM mode is usually negligible, but this is not the case during LP mode.

In LP mode, the peak inductor current during on-time of the high-side switch is limited to $I_{PEAK(LP)}$. Also, in LP mode, the low-side switch is constantly turned off thereby forcing the regulator to operate in Discontinuous Conduction Mode (DCM) in order to reduce switching losses. A LP comparator monitors the output voltage on the FB pin and allows the regulator to switch until the FB pin voltage is greater than 0.5% of its nominal value (0.8 V). When FB voltage is greater than 0.804 V, the ARG81800 coasts by terminating the switching pulses.

During coasting, the device shuts down most of its internal control circuitry to ensure very low quiescent current is drawn from the input. The number of switching pulses, in LP mode, required to coast the device depend on various factors including: input voltage, output voltage, load current, output inductor, and output capacitor. If ARG81800 starts coasting after a single switching pulse, then the output voltage ripple would be dictated by this single pulse. The peak inductor current without slope compensation (I_{PEAK_LO}) is given by:

Equation 16:

$$I_{PEAK\_LO} = \frac{I_{PEAK(LP)}}{1 + \frac{S_E \times L_O}{V_{IN} - V_{OUT}}}$$

where $I_{PEAK(LP)}$ is the peak inductor current, specified in the Electrical Characteristics table, at which device enters into LP mode. Referring to Figure 7, on-time and off-time calculations are given as:

Equation 17:

$$t_{ON} = \frac{I_{PEAK\_LO} \times L_O}{V_{IN} - V_{OUT} - I_{PEAK_L} \times (R_{DS(ON)HS} + L_{O(DCR)})}$$

Equation 18:

$$t_{OFF} = \frac{I_{PEAK\_LO} \times L_O}{V_{OUT}}$$

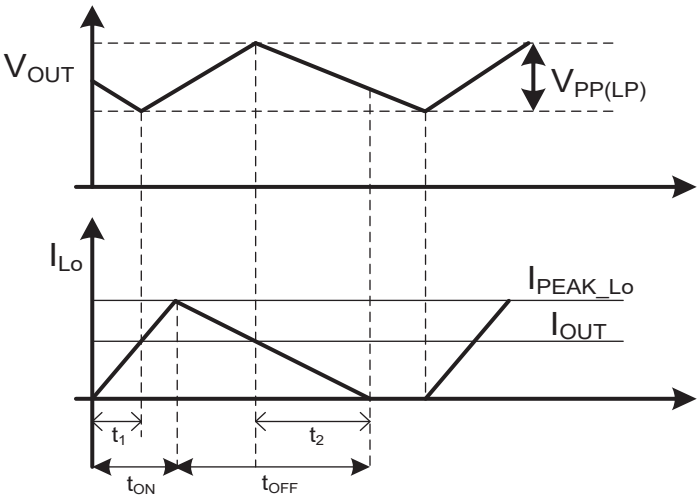

Figure 7: Output Voltage Ripple in LP Mode

During on-time interval, the length of time for the inductor current to rise from 0 A to I_{OUT} is:

Equation 19:

$$t_1 = \frac{I_{OUT} \times L_O}{V_{IN} - V_{OUT} - I_{PEAK\_LO} \times (R_{DS(ON)HS} + L_{O(DCR)})}$$

During off-time interval, the length of time for the inductor current to fall from I_{OUT} to 0 A is:

Equation 20:

$$t_2 = \frac{I_{OUT} \times L_O}{V_{OUT}}$$

Given the peak inductor current (I_{PEAK_L}) and the rise and fall times (t_{ON} and t_{OFF}) for the inductor current, the output voltage ripple for a single switching pulse can be calculated as follows:

Equation 21:

$$V_{PP(LP)} = \frac{I_{PEAK\_LO} - I_{OUT}}{2 \times C_{OUT}} \times (t_{ON} + t_{OFF} - t_1 - t_2)$$

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INPUT CAPACITORS

Three factors should be considered when choosing the input capacitors. First, the capacitors must be chosen to support the maximum expected input surge voltage with adequate design margin. Second, the capacitor RMS current rating must be higher than the expected RMS input current to the regulator. Third, the capacitors must have enough capacitance and a low enough ESR to limit the input voltage dV/dt to much less than the hysteresis of the UVLO circuitry (250 mV nominal) at maximum loading and minimum input voltage. The input capacitors must deliver an RMS current (I_{RMS}) given by:

Equation 22:

$$I_{RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where the duty cycle (D) is defined as:

Equation 23:

$$D \approx \frac{V_{OUT}}{V_{IN}}$$

Figure 8 shows the normalized input capacitor RMS current versus duty cycle. To use this graph, simply find the operational duty cycle (D) on the x-axis and determine the input/output current multiplier on the y-axis. For example, at a 20% duty cycle, the input/output current multiplier is 0.40. Therefore, if the regulator is delivering 1.0 A of steady-state load current, the input capacitor(s) must support 0.40 × 1.0 A or 0.4 A RMS.

The input capacitor(s) must limit the voltage deviations at the VIN pin to significantly less than the device UVLO hysteresis during maximum load and minimum input voltage condition. The following equation allows to calculate the minimum input capacitance required:

Equation 24:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{0.85 \times f_{SW} \times \Delta V_{IN(MIN)}}$$

where $\Delta V_{IN(MIN)}$ is chosen to be much less than the hysteresis of the VIN UVLO comparator ($\Delta V_{IN(MIN)} \leq 150$ mV is recommended), and f_{SW} is the nominal PWM frequency. The D × (1–D) term in Equation 22 has an absolute maximum value of 0.25 at 50% duty cycle. So, for example, a very conservative design based on I_{OUT} = 1.0 A, f_{SW} = 0.5 MHz, D × (1–D) = 0.25, and ΔV_{IN} =150 mV yields:

$$C_{IN} \geq \frac{1.0 \times 0.25}{0.85 \times 0.5 \times 10^{6} \times 150 \times 10^{-3}} = 1.95\ \mu F$$

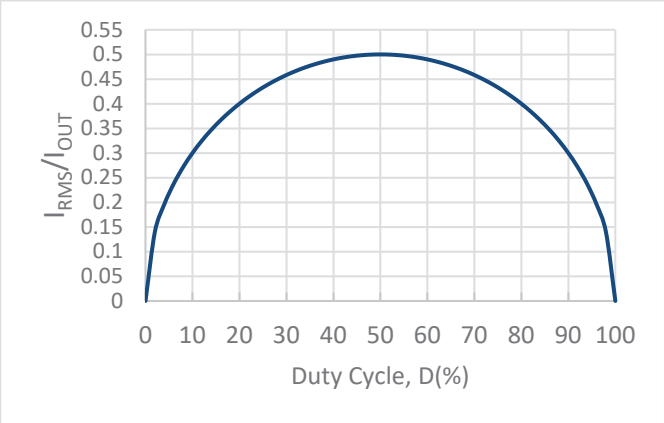

Figure 8: Normalized Input Capacitor Ripple versus Duty Cycle

A good design should consider the DC bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction), so these types should be avoided. The X5R, X7R, and X8R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

For all ceramic capacitors, the DC bias effect is even more pronounced on smaller sizes of device case, so a good design uses the largest affordable case size (such as 1206 or 1210). Also, it is advisable to select input capacitors with plenty of design margin in the voltage rating to accommodate the worst case transient input voltage (such as a load dump as high as 40 V for automotive applications).

BOOTSTRAP CAPACITOR

A bootstrap capacitor must be connected between the BOOT and SW pins to provide floating gate drive to the high-side MOSFET. Usually, 47 nF is an adequate value. This capacitor should be a high-quality ceramic capacitor, such as an X5R or X7R, with a voltage rating of at least 16 V.

SOFT START AND HICCUP MODE TIMING (C_{SS})

The soft start time of the ARG81800 is determined by the value of the capacitance (C_{SS}) at the soft start pin. When the ARG81800 is enabled, the SS pin sources the charging current I_{SS} and the voltage across the soft start capacitor C_{SS} starts ramping upward from 0 V. However, PWM switching will begin only after the voltage across the C_{SS} rises above 400 mV.

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The soft start delay (t_{dSS}) can be calculated using the equation below:

Equation 25:

$$t_{dSS} = C_{SS} \times \left(\frac{0.4}{I_{SS}}\right)$$

If the device is starting with a very heavy load, a very fast soft start time may cause the regulator to exceed the pulse-by-pulse overcurrent threshold. This occurs because the sum of the full load current, the inductor ripple current, and the additional current required to charge the output capacitors

Equation 26:

$$I_{CO} = C_O \times \frac{V_{OUT}}{t_{SS}}$$

is higher than the pulse-by-pulse current threshold. This phenomenon is more pronounced when using high value electrolytic type output capacitors. To avoid prematurely triggering hiccup mode, the soft start capacitor (C_{SS}) should be calculated according to equation below:

Equation 27:

$$C_{SS} \geq \frac{I_{SS} \times V_{OUT} \times C_O}{0.8 \times I_{CO}}$$

where V_{OUT} is the output voltage, C_O is the output capacitance, I_{CO} is the amount of current allowed to charge the output capacitance during soft start (0.1 A < I_{CO} < 0.3 A is recommended). The soft start time (t_{SS}) can be calculated as below:

Equation 28:

$$t_{SS} = 0.8 \times \left(\frac{C_{SS}}{I_{SS}}\right)$$

Higher values of I_{CO} result in faster soft start times. However, lower values of I_{CO} ensure that hiccup mode is not falsely triggered. Allegro recommends starting the design with an I_{CO} of 0.1 A and increasing it only if the soft start time is too slow. If a non-standard capacitor value for C_{SS} is calculated, the next larger value should be used.

When the device is in hiccup mode, the soft start capacitor is used as a timing capacitor and sets the hiccup period. The soft start pin charges the soft start capacitor with I_{SS} during a startup attempt and discharges the same capacitor with I_{HIC} between startup attempts. Because the ratio of I_{SS}:I_{HIC} is approximately 4:1, the time between hiccups will be about four times as long as the startup time. Therefore, the effective duty cycle will be very low and the junction temperature will be kept low.

COMPENSATION COMPONENTS (R_Z, C_Z, AND C_P)

The objective of the selection of the compensation components is to ensure adequate stability margins to avoid instability issues, to maintain a high loop gain at DC to achieve excellent output voltage regulation and to obtain a high loop bandwidth for superior transient response. To a first order, the closed-loop model of a peak current mode controlled regulator can be broken into two blocks as shown below in Figure 9.

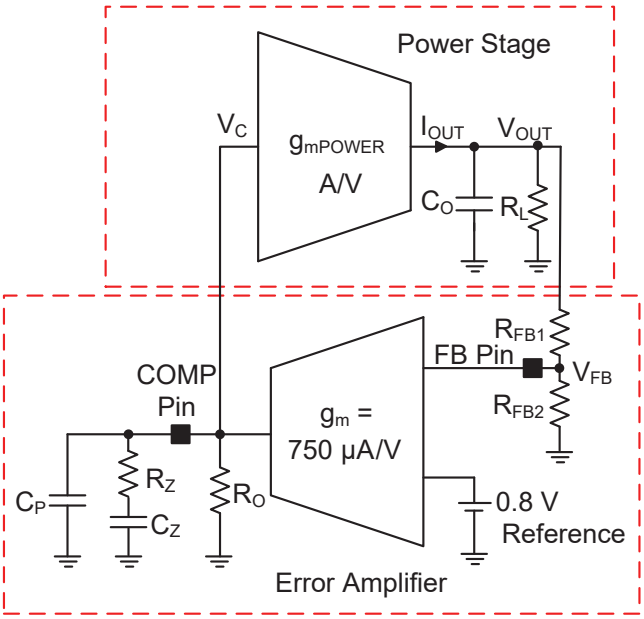

Figure 9: Closed-Loop Model of Peak Current Mode Controlled Regulator

POWER STAGE

The power stage includes the output filter capacitor, C_O, the equivalent load, R_L, and the inner current loop which consists of the PWM modulator and the output inductor, L_O. The inner current loop, with a first-order approximation, can be effectively modeled as a transconductance amplifier that converts the control voltage (V_C) from the error amplifier to a peak output inductor current with an equivalent gain g_{mPower}. Although, the peak current through the inductor is being controlled—neglecting the inductor ripple current—it is acceptable to replace it with output current I_{OUT}.

From a small-signal point of view, the current mode control loop behaves like a current source and therefore the power inductor can be ignored. The output capacitor integrates the ripple current through the inductor, effectively forming a single pole with the output load. A control-to-output transfer function between the control voltage (V_C), output of the error amplifier in the feed-

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back loop, and the regulator output voltage (V_{OUT}) describes the dynamics of the power stage. The DC gain of the power stage, i.e., control-to-output transfer function, is given by:

Equation 29:

$$G_{DC(CO)} = g_{mPOWER} \times R_L$$

where g_{mPOWER} is the equivalent gain of the inner current loop (specified in the Electrical Characteristics table) and R_L is the load resistance.

The control-to-output transfer function has a pole $f_{P(CO)}$, formed by the output capacitance (C_O) and load resistance (R_L), located at:

Equation 30:

$$f_{P(CO)} = \frac{1}{2\pi \times R_L \times C_O}$$

The control-to-output transfer function has a zero $f_{Z(CO)}$, formed by the output capacitance (C_O) and its associated ESR, located at:

Equation 31:

$$f_{Z(CO)} = \frac{1}{2\pi \times ESR \times C_O}$$

For a design with very low-ESR type output capacitors (such as ceramic or OSCON output capacitors), the ESR zero, $f_{Z(CO)}$, is usually at a very high frequency so it can be ignored. On the other hand, with high-ESR electrolytic output capacitors, the ESR zero falls below or near the 0 dB crossover frequency of the closed-loop; hence, it should be cancelled by the pole formed by the C_P capacitor and the R_Z resistor discussed and identified later as $f_{P2(EA)}$.

ERROR AMPLIFIER

The error amplifier, as a part of the output voltage feedback loop, comprises a transconductance amplifier with an external Type-II compensation formed by R_Z-C_Z-C_P network. A Type-II compensated error amplifier introduces two poles and a zero. The placement of these poles and zero should be such that the closed-loop system has sufficient stability margins and high bandwidth (loop crossover frequency) and provides optimal transient response.

The DC gain of the feedback loop, including the error amplifier and the feedback resistor divider is given by:

Equation 32:

$$G_{DC(FB)} = A_{VOL} \times \frac{R_{FB2}}{R_{FB1} + R_{FB2}} = A_{VOL} \times \frac{V_{FB}}{V_{OUT}}$$

where A_{VOL} is the open-loop DC gain of the error amplifier (specified in the Electrical Characteristics table).

The DC gain of the error amplifier is 65 dB (equivalent to 1778) and with a g_m value of 750 µA/V, the effective output impedance, R_O, of the amplifier is:

Equation 33:

$$R_O = \frac{1778}{750 \times 10^{-6}} = 2.37\ M\Omega$$

Typically, $R_O \gg R_Z$ and $C_Z \gg C_P$, which simplifies the derivation of the transfer function of the Type-II compensated error amplifier. The transfer function has a (very) low frequency pole $f_{P1(EA)}$ dominated by the error amplifier output impedance R_O and the compensation capacitor C_Z:

Equation 34:

$$f_{P1(EA)} = \frac{1}{2\pi \times R_O \times C_Z}$$

The transfer function of the Type-II compensated error amplifier also has a zero at frequency $f_{Z(EA)}$ caused by the resistor R_Z and the capacitor C_Z:

Equation 35:

$$f_{Z(EA)} = \frac{1}{2\pi \times R_Z \times C_Z}$$

Lastly, the transfer function of the Type-II compensated error amplifier has a (very) high frequency pole $f_{P2(EA)}$ dominated by the resistor R_Z resistor and the capacitor C_P:

Equation 36:

$$f_{P2(EA)} = \frac{1}{2\pi \times R_Z \times C_P}$$

Although there are many different approaches for designing the feedback loop, a good design approach attempts to maximize the closed-loop system stability, while providing a high bandwidth and optimized transient response. A generalized tuning procedure is presented below to systematically determine the values of compensation components (R_Z, C_Z, and C_P) in the feedback loop.

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A GENERALIZED TUNING PROCEDURE

1. Choose the system bandwidth (f_C). This is the frequency at which the magnitude of the gain crosses 0 dB. Recommended values for f_C, based on the PWM switching frequency, are in the range $f_{SW} / 20 < f_C < f_{SW} / 10$. A higher value of f_C generally provides a better transient response, while a lower value of f_C generally makes it easier to obtain higher gain and phase margins.
2. Calculate the R_Z resistor value. This sets the system bandwidth (f_C):

   Equation 37:

$$R_Z = f_C \times \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times C_O}{g_{mPOWER} \times g_m}$$

3. Calculate the range of values for the C_Z capacitor. Use the following:

   Equation 38:

$$\frac{4}{2\pi \times R_Z \times f_C} < C_Z < \frac{1}{2\pi \times R_Z \times 1.5 \times f_{P(CO)}}$$

   To maximize system stability, i.e., high gain and phase margins, use a higher value of C_Z. To optimize transient recovery time, although at the expense of low stability margins, use a lower value of C_Z.

4. Calculate the frequency of the ESR zero $f_{Z(CO)}$ formed by the output capacitor(s) by using Equation 31 (repeated here):

$$f_{Z(CO)} = \frac{1}{2\pi \times ESR \times C_O}$$

If $f_{Z(CO)}$ is at least one decade higher than the target crossover frequency f_C, then $f_{Z(CO)}$ can be ignored. This is usually the case for a design using ceramic output capacitors. Use Equation 36 to calculate the value of C_P by setting $f_{P2(EA)}$ to either $5 \times f_C$ or $f_{SW} / 2$, whichever is higher.

Alternatively, if $f_{Z(CO)}$ is near or below the target crossover frequency f_C, then use Equation 36 to calculate the value of C_P by setting $f_{P2(EA)}$ equal to $f_{Z(CO)}$. This is usually the case for a design using high ESR electrolytic output capacitors.

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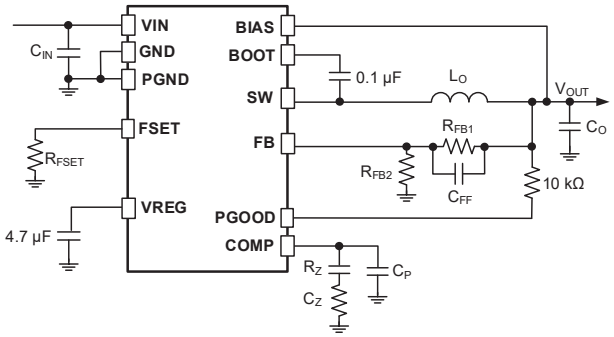

Figure 10: Applications Schematic Showing Component Locations

Table 3: Recommended External Components (for load transient slew rate < 50 mA/µs)

ARG81800											
V_{OUT}	f_{SW}	R_{FSET}	L_O	C_O	COMP Components (PM > 60 deg)			FB Components			$C_{IN(MIN)}$
					R_Z	C_Z	C_P	R_{FB1}	R_{FB2}	C_{FF}	
5.0 V	2.15 MHz	14.3 kΩ	4.7 µH	20 µF	30.1 kΩ	1.2 nF	10 pF	732 kΩ	137 kΩ	4.7 pF	1.0 µF
3.3 V	2.15 MHz	14.3 kΩ	3.3 µH	20 µF	30.1 kΩ	2.2 nF	10 pF	301 kΩ	95.3 kΩ	4.7 pF	1.0 µF
5.0 V	400 kHz	90.9 kΩ	22 µH	33 µF	24.9 kΩ	1.2 nF	10 pF	732 kΩ	137 kΩ	4.7 pF	4.7 µF
3.3 V	400 kHz	90.9 kΩ	15 µH	47 µF	26.1 kΩ	2.2 nF	10 pF	301 kΩ	95.3 kΩ	4.7 pF	4.7 µF
ARG81800-1											
V_{OUT}	f_{SW}	R_{FSET}	L_O	C_O	COMP Components (PM > 60 deg)			FB Components			$C_{IN(MIN)}$
					R_Z	C_Z	C_P	R_{FB1}	R_{FB2}	C_{FF}	
5.0 V	2.15 MHz	14.3 kΩ	9.1 µH	20 µF	51.1 kΩ	1.2 nF	10 pF	732 kΩ	137 kΩ	4.7 pF	1.0 µF
3.3 V	2.15 MHz	14.3 kΩ	7.5 µH	20 µF	40.2 kΩ	1.2 nF	10 pF	301 kΩ	95.3 kΩ	4.7 pF	1.0 µF
5.0 V	400 kHz	90.9 kΩ	43 µH	33 µF	34.0 kΩ	2.2 nF	10 pF	732 kΩ	137 kΩ	4.7 pF	4.7 µF
3.3 V	400 kHz	90.9 kΩ	33 µH	47 µF	34.0 kΩ	2.2 nF	10 pF	301 kΩ	95.3 kΩ	4.7 pF	4.7 µF

Note 1: Components were chosen to maintain LP ripple voltage and minimize voltage droop during LP to PWM changeover.
Note 2: C_{FF} is chosen to offset 15 to 25 pF of stray capacitance at the FB pin.

Table 4: Recommended External Components (for load transient slew rate > 50 mA/µs)

ARG81800											
V_{OUT}	f_{SW}	R_{FSET}	L_O	C_O	COMP Components (PM > 60 deg)			FB Components			$C_{IN(MIN)}$
					R_Z	C_Z	C_P	R_{FB1}	R_{FB2}	C_{FF}	
5.0 V	2.15 MHz	14.3 kΩ	4.7 µH	42 µF	10.0 kΩ	5.6 nF	10 pF	732 kΩ	137 kΩ	4.7 pF	1.0 µF
3.3 V	2.15 MHz	14.3 kΩ	3.3 µH	42 µF	8.06 kΩ	9.1 nF	10 pF	301 kΩ	95.3 kΩ	4.7 pF	1.0 µF
5.0 V	400 kHz	90.9 kΩ	22 µH	55 µF	5.11 kΩ	9.1 nF	10 pF	732 kΩ	137 kΩ	4.7 pF	4.7 µF
3.3 V	400 kHz	90.0 kΩ	15 µH	69 µF	5.23 kΩ	9.1 nF	10 pF	301 kΩ	95.3 kΩ	4.7 pF	4.7 µF
ARG81800-1											
V_{OUT}	f_{SW}	R_{FSET}	L_O	C_O	COMP Components (PM > 60 deg)			FB Components			$C_{IN(MIN)}$
					R_Z	C_Z	C_P	R_{FB1}	R_{FB2}	C_{FF}	
5.0 V	2.15 MHz	14.3 kΩ	9.1 µH	42 µF	30.1 kΩ	5.6 nF	10 pF	732 kΩ	137 kΩ	4.7 pF	1.0 µF
3.3 V	2.15 MHz	14.3 kΩ	7.5 µH	42 µF	12.1 kΩ	5.6 nF	10 pF	301 kΩ	95.3 kΩ	4.7 pF	1.0 µF
5.0 V	400 kHz	90.9 kΩ	43 µH	55 µF	10.0 kΩ	9.1 nF	10 pF	732 kΩ	137 kΩ	4.7 pF	4.7 µF
3.3 V	400 kHz	90.9 kΩ	33 µH	69 µF	10.0 kΩ	9.1 nF	10 pF	301 kΩ	95.3 kΩ	4.7 pF	4.7 µF

Note 1: Components were chosen to maintain LP ripple voltage and minimize voltage droop during LP to PWM changeover.
Note 2: C_{FF} is chosen to offset 15 to 25 pF of stray capacitance at the FB pin.

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POWER DISSIPATION AND THERMAL CALCULATIONS

The total power dissipated in the ARG81800 is the sum of the power dissipated from the V_{IN} supply current (P_{IN}), the power dissipated due to the switching of the high-side power MOSFET (P_{SWH}), the power dissipated due to the conduction of rms current in the high-side MOSFET (P_{CH}) and low-side MOSFET (P_{CL}), power dissipated due to the low-side MOSFET body diode conduction during the non-overlap time (P_{NO}) and the power dissipated by both high-side and low-side gate drivers (P_{DRIVER}).

The power dissipated from the V_{IN} supply current (with BIAS pin open) can be calculated using Equation 39:

Equation 39:

$$P_{IN} = V_{IN} \times I_{IN,PWM} + (V_{IN} - V_{GS}) \times (Q_{GH} + Q_{GL}) \times f_{SW}$$

where V_{IN} is the input voltage, $I_{IN,PWM}$ is the input quiescent current drawn by the ARG81800 in PWM mode (see EC table), V_{GS} is the MOSFET gate drive voltage (typically 4.8 V), Q_{GH} and Q_{GL} are the internal high-side and low-side MOSFET gate charges (approximately 0.3 nC and 0.6 nC, respectively), and f_{SW} is the PWM switching frequency.

The power dissipated by the high-side MOSFET during PWM switching can be calculated using Equation 40:

Equation 40:

$$P_{SWH} = \frac{V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}}{2}$$

where V_{IN} is the input voltage, I_{OUT} is the regulator output current, f_{SW} is the PWM switching frequency, t_r and t_f are the rise and fall times measured at the switch node.

The exact rise and fall times at the SW node will depend on the external components and PCB layout, so each design should be measured at full load. Approximate values for both t_r and t_f range from 10 to 20 ns.

The power dissipated in the high-side MOSFET while it is conducting can be calculated using Equation 41:

Equation 41:

$$P_{CH} = I_{RMS,H}^2 \times R_{DS(ON)H} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(I_{OUT}^2 + \frac{\Delta I_{LO}^2}{12}\right) \times R_{DS(ON)H}$$

Similarly, the conduction losses dissipated in the low-side MOSFET while it is conducting can be calculated by the following equation:

Equation 42:

$$P_{CL} = I_{RMS,L}^2 \times R_{DS(ON)L} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(I_{OUT}^2 + \frac{\Delta I_{LO}^2}{12}\right) \times R_{DS(ON)L}$$

where I_{OUT} is the regulator output current, ΔI_{LO} is the peak-to-peak inductor ripple current, $R_{DS(ON)H}$ is the on-resistance of the high-side MOSFET, $R_{DS(ON)L}$ is the on-resistance of the low-side MOSFET.

The $R_{DS(ON)}$ of both MOSFETs have some initial tolerance plus an increase from self-heating and elevated ambient temperatures. A conservative design should accommodate an $R_{DS(ON)}$ with at least 15% initial tolerance plus 0.39%/°C increase due to temperature.

The power dissipated in the low-side MOSFET body diode during the non-overlap time can be calculated as follows:

Equation 43:

$$P_{NO} = V_{SD} \times I_{OUT} \times 2 \times t_{NO} \times f_{SW}$$

where V_{SD} is the source-to-drain voltage of the low-side MOSFET (typically 0.60 V), and t_{NO} is the non-overlap time (15 ns typical).

The power dissipated in the internal gate drivers can be calculated using Equation 44:

Equation 44:

$$P_{DRIVER} = (Q_{GH} + Q_{GL}) \times V_{GS} \times f_{SW}$$

where V_{GS} is the gate drive voltage (typically 4.8 V).

Finally, the total power dissipated in the ARG81800 is given by:

Equation 45:

$$P_{TOTAL} = P_{IN} + P_{SWH} + P_{CH} + P_{CL} + P_{NO} + P_{DRIVER}$$

The average junction temperature (T_J) can be calculated as follows:

Equation 46:

$$T_J = P_{TOTAL} \times R_{\theta JA} + T_A$$

where P_{TOTAL} is the total power dissipated from Equation 45, $R_{\theta JA}$ is the junction-to-ambient thermal resistance (37°C/W on a 4-layer PCB), and T_A is the ambient temperature.

$R_{\theta JA}$ includes the thermal impedance from junction to case, $R_{\theta JC}$ and the thermal impedance from case to ambient, $R_{\theta CA}$. $R_{\theta CA}$ is generally determined by the amount of copper that is used underneath and around the device on the printed circuit board.

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The maximum allowed power dissipation depends on how efficiently heat can be transferred from the junction to the ambient air, i.e., minimizing the $R_{\theta JA}$. As with any regulator, there are limits to the amount of heat that can be dissipated before risking thermal shutdown. There are tradeoffs between ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, airflow, and other nearby heat sources. Even a small amount of airflow will reduce the junction temperature considerably.

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EMI/EMC AWARE PCB DESIGN

The ARG81800 is designed to minimize electromagnetic (EM) emissions when proper PCB layout techniques are adopted. A good PCB layout is also critical for the ARG81800 to provide clean and stable output voltages. Design guidelines for EMI/EMC-aware PCB layout are presented below. Figure 10 shows a typical application schematic of a synchronous buck regulator IC with critical power paths/loops.

1. Place the ceramic input capacitors as close as possible to the VIN pin and PGND pins to make the loop area minimal, and the traces of the input capacitors to VIN pin should be short and wide to minimize the inductance. This critical loop is shown as trace 1 in Figure 11. The bulk/electrolytic input capacitor can be located further away from VIN pin. The input capacitors and ARG81800 IC should be on the same side of the board with traces on the same layer.
2. The loop from the input supply and capacitors, through the high-side MOSFET, into the load via the output inductor, and back to ground should be minimized with relatively wide traces.
3. When the high-side MOSFET is off, free-wheeling current flows from ground, through the synchronous low-side MOSFET, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces. This loop is shown as trace 2 in Figure 11.
4. Place the output capacitors relatively close to the output inductor (L_O) and the ARG81800. Ideally, the output capacitors, output inductor and the ARG81800 should be on the same layer. Connect the output inductor and the output capacitors with a fairly wide trace. The output capacitors must use a ground plane to make a very low-inductance connection to the GND. These critical connections are shown as trace 3 in Figure 11.
5. Place the output inductor (L_O) as close as possible to the SW pin with short and wide traces. This critical trace is shown as trace 4 in Figure 11. The voltage at SW node transitions from 0 V to V_{IN} with a high dv/dt rate. This node is the root cause of many noise issues. It is suggested to minimize the SW copper area to minimize the coupling capacitance between SW node and other noise-sensitive nodes; however, the SW node area cannot be too small in order to conduct high current. A ground copper area can be placed underneath the SW node to provide additional shielding. Also, noise sensitive analog signals (like FB, COMP) should not be routed near the SW polygon.
6. Place the feedback resistor divider (R_{FB1} and R_{FB2}) very close to the FB pin. Route the ground side of R_{FB2} as close as possible to the ARG81800.
7. Place the compensation components (R_Z, C_Z, and C_P) as close as possible to the COMP pin. Also route the ground side of C_Z and C_P as close as possible to the ARG81800.
8. Place the FSET resistor as close as possible to the FSET pin; Place the soft start capacitor C_{SS} as close as possible to the SS pin.
9. The output voltage sense trace (from VOUT to R_{FB1}) should be routed as close as possible to the load to obtain the best load regulation.
10. Place the bootstrap capacitor (C_{BOOT}) near the BOOT pin and keep the routing from this capacitor to the SW polygon as short as possible. This critical trace is shown as trace 5 in Figure 11.
11. A two-layer (TOP and BOT) PCB is sufficient for better thermal performance.
12. When connecting the input and output ceramic capacitors, use multiple vias to GND planes and place the vias as close as possible to the pads of the components. Do not use thermal reliefs around the pads for the input and output ceramic capacitors.
13. Place all the components on the TOP layer and limit the routing only to the top layer. Use BOT layer as GND plane.
14. To minimize thermal resistance, extend ground planes on TOP layer as much as possible and use thermal vias to connect them to GND plane in BOT layer.
15. To minimize PCB losses and improve system efficiency, the power traces should be as wide as possible.
16. EMI/EMC issues are always a concern. Allegro recommends having placeholder for an RC snubber from SW to ground. The resistor should be 0805 or 1206 size.

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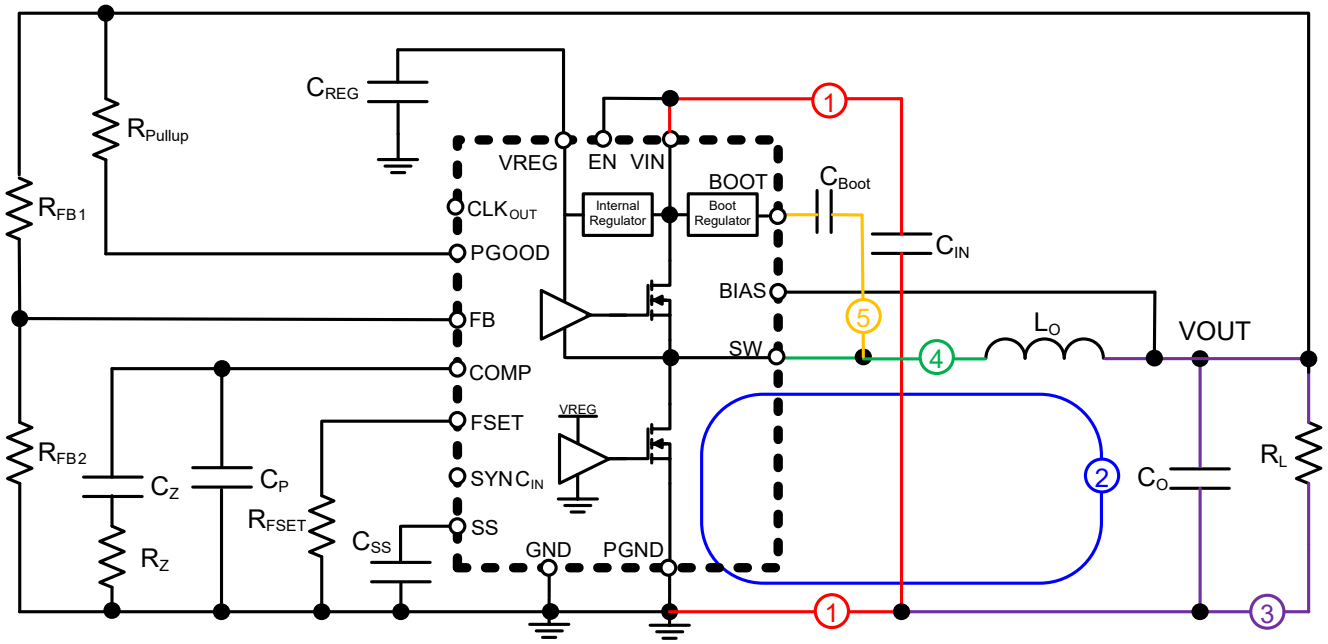

Figure 11: PCB Layout for Minimizing EM Emissions

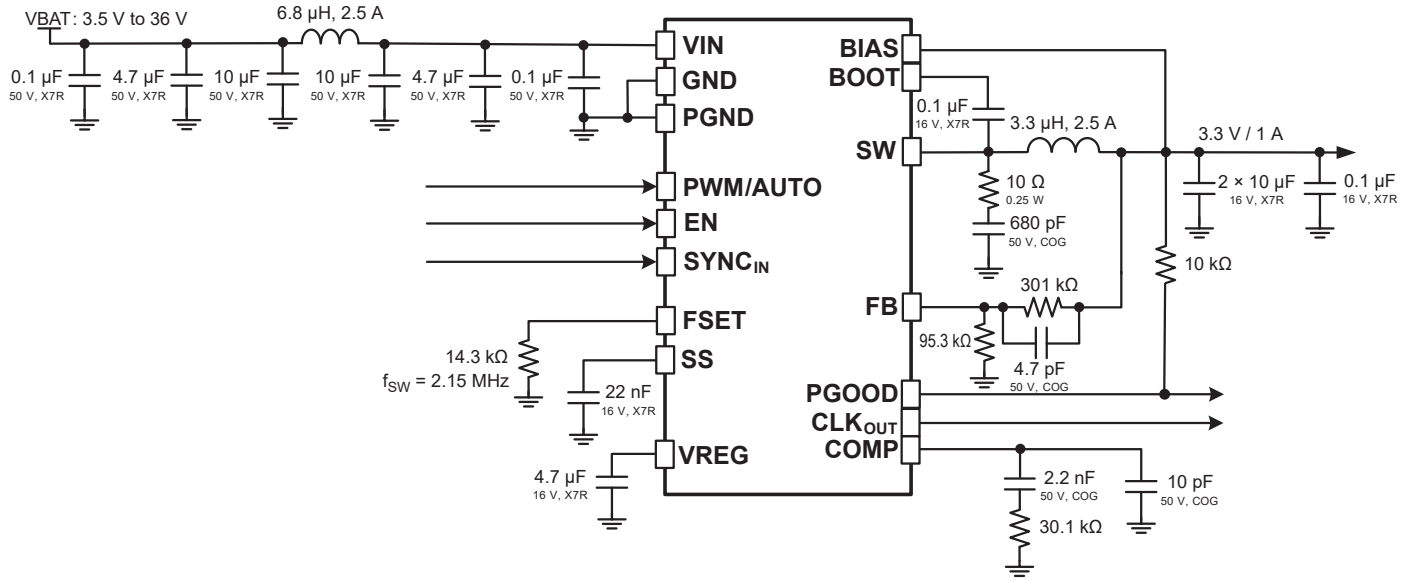

Figure 12: 3.3 V, 1 A Buck Regulator with Input EMI Filter

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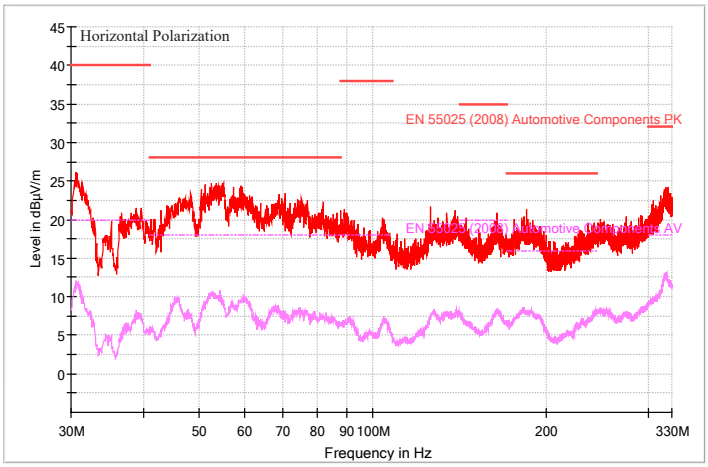

Figure 13: Radiated EMI – Biconical Antenna
V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, f_{SW} = 2.15 MHz

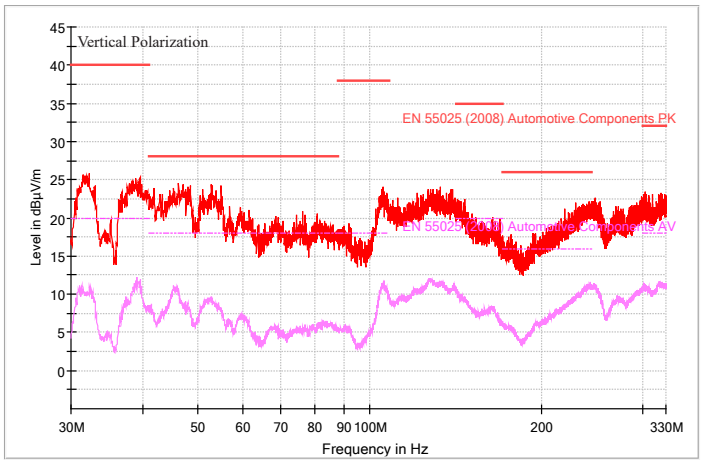

Figure 14: Radiated EMI – Biconical Antenna
V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, f_{SW} = 2.15 MHz

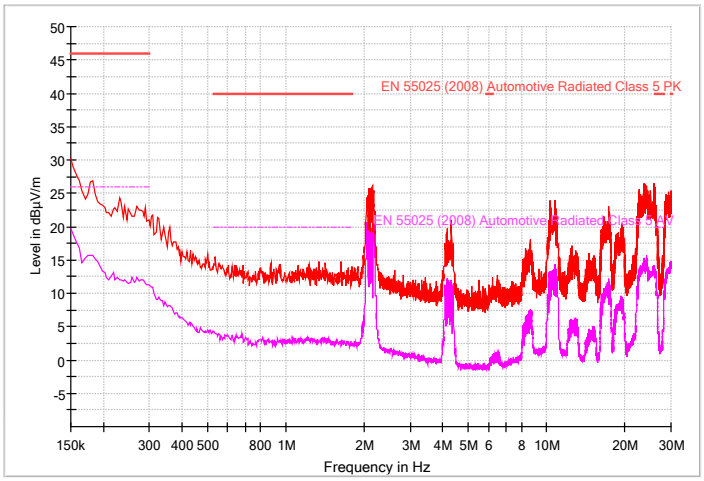

Figure 15: Radiated EMI – Monopole Antenna
V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, f_{SW} = 2.15 MHz

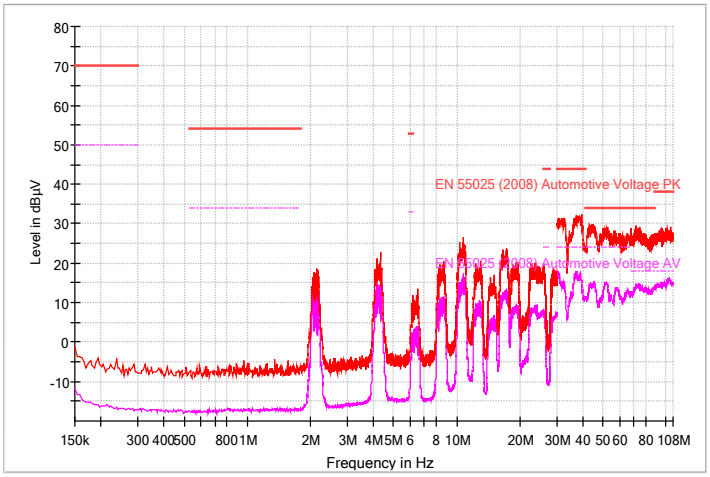

Figure 16: Conducted EMI
V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, f_{SW} = 2.15 MHz

EMI test results are obtained using standard evaluation board with Input EMI filter and Snubber (see Figure 12 above).

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TYPICAL REFERENCE DESIGNS

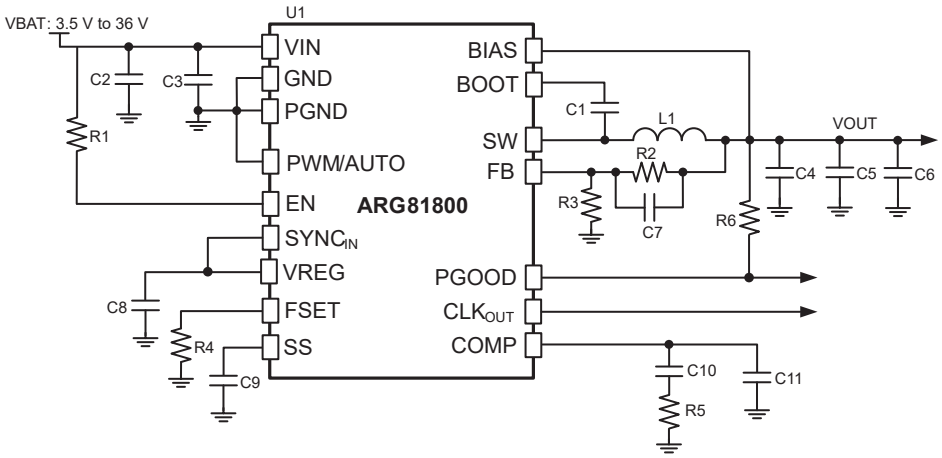

Figure 17: Reference Design 1 – AUTO Mode with CLK_{OUT} enabled
V_{IN} = 3.5 to 36 V, V_{OUT} = 3.3 V, I_{OUT} = 0 to 1.0 A, f_{SW} = 2.15 MHz

Table 5: Reference Design 1 – Recommended Bill of Materials

Designator	Description	Value	Footprint	Manufacturer	Manufacturer P/N
C1	Capacitor, X7R	0.1 µF, 50 V	0603	Murata	GCM188R71H104KA57D
C2	Capacitor, X7R	4.7 µF, 50 V	1206	Murata	GRJ31CR71H475KE11L
C3	Capacitor, X7R	0.1 µF, 50 V	0603	Murata	GCM188R71H104KA57D
C4	Capacitor, X7R	0.1 µF, 50 V	1206	Murata	GCM319R71H104KA37J
C5	Capacitor, X7R	10 µF, 16 V	1210	Murata	GRM32DR71C106KA01L
C6	Capacitor, X7R	10 µF, 16 V	1210	Murata	GRM32DR71C106KA01L
C7	Capacitor, C0G (NP0)	4.7 pF, 50 V	0603	Murata	GCM1885C1H4R7BA16D
C8	Capacitor, X7R	4.7 µF, 16 V	0805	Murata	GCJ21BR71C475KA01L
C9	Capacitor, X7R	22 nF, 50 V	0603	Murata	GRM188R71H223KA01D
C10	Capacitor, X7R	2.2 nF, 50 V	0603	Murata	GCM188R71H222KA37D
C11	Capacitor, C0G (NP0)	10 pF, 50 V	0603	Kemet	C0603C100J5GACTU
L1	Inductor	3.3 µH, 2 A	5.2 mm × 5.2 mm	Wurth Electronics	74437334033
R1	Resistor, 1%, 1/10 W	10 kΩ	0603	Panasonic	ERJ-3EKF1002V
R2	Resistor, 1%, 1/10 W	301 kΩ	0603	Panasonic	ERJ-3EKF3013V
R3	Resistor, 1%, 1/10 W	95.3 kΩ	0603	Panasonic	ERJ-3EKF9532V
R4	Resistor, 1%, 1/10 W	14.3 kΩ	0603	Panasonic	ERJ-3EKF1432V
R5	Resistor, 1%, 1/10 W	30.1 kΩ	0603	Panasonic	ERJ-3EKF3012V
R6	Resistor, 1%, 1/10 W	10 kΩ	0603	Panasonic	ERJ-3EKF1002V
U1	Allegro IC	ARG81800	QFN20_4x4	Allegro	ARG81800KESJSR

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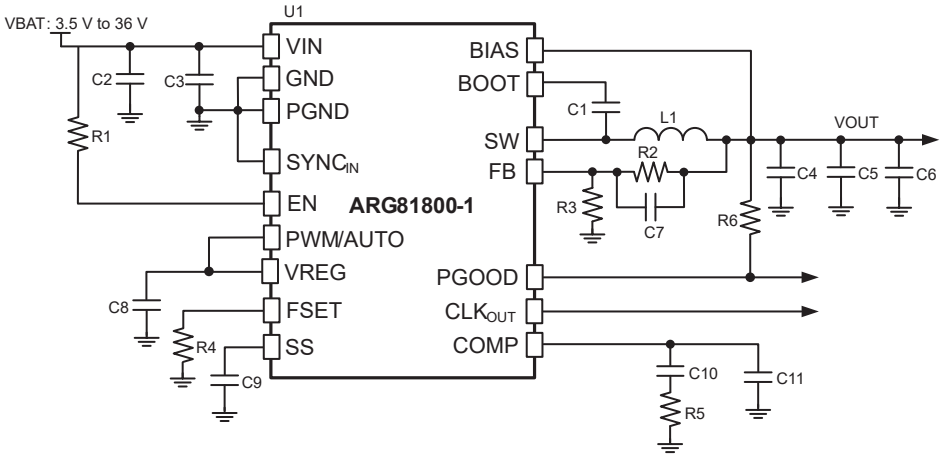

Figure 18: Reference Design 2 – Forced PWM Mode with CLK_{OUT} disabled
V_{IN} = 3.5 to 36 V, V_{OUT} = 5.0 V, I_{OUT} = 0 to 0.5 A, f_{SW} = 400 kHz

Table 6: Reference Design 2 – Recommended Bill of Materials

Designator	Description	Value	Footprint	Manufacturer	Manufacturer P/N
C1	Capacitor, X7R	0.1 µF, 50 V	0603	Murata	GCM188R71H104KA57D
C2	Capacitor, X7R	4.7 µF, 50 V	1206	Murata	GRJ31CR71H475KE11L
C3	Capacitor, X7R	0.1 µF, 50 V	0603	Murata	GCM188R71H104KA57D
C4	Capacitor, X7R	0.1 µF, 50 V	1206	Murata	GCM319R71H104KA37J
C5	Capacitor, X7R	22 µF, 16 V	1210	Murata	GRM32ER71C226MEA8L
C6	Capacitor, X7R	10 µF, 16 V	1210	Murata	GRM32DR71C106KA01L
C7	Capacitor, C0G (NP0)	4.7 pF, 50 V	0603	Murata	GCM1885C1H4R7BA16D
C8	Capacitor, X7R	4.7 µF, 16 V	0805	Murata	GCJ21BR71C475KA01L
C9	Capacitor, X7R	22 nF, 50 V	0603	Murata	GRM188R71H223KA01D
C10	Capacitor, X7R	2.2 nF, 50 V	0603	Murata	GCM188R71H222KA37D
C11	Capacitor, C0G (NP0)	10 pF, 50 V	0603	Kemet	C0603C100J5GACTU
L1	Inductor	47 µH, 2.2A	10 mm × 10 mm	Wurth Electronics	7447714470
R1	Resistor, 1%, 1/10 W	10 kΩ	0603	Panasonic	ERJ-3EKF1002V
R2	Resistor, 1%, 1/10 W	732 kΩ	0603	Panasonic	ERJ-3EKF7323V
R3	Resistor, 1%, 1/10 W	140 kΩ	0603	Panasonic	ERJ-3EKF1403V
R4	Resistor, 1%, 1/10 W	90.9 kΩ	0603	Panasonic	ERJ-3EKF7152V
R5	Resistor, 1%, 1/10 W	34 kΩ	0603	Panasonic	ERJ-3EKF3402V
R6	Resistor, 1%, 1/10 W	10 kΩ	0603	Panasonic	ERJ-3EKF1002V
U1	Allegro IC	ARG81800-1	QFN20_4x4	Allegro	ARG81800KESJSR-1

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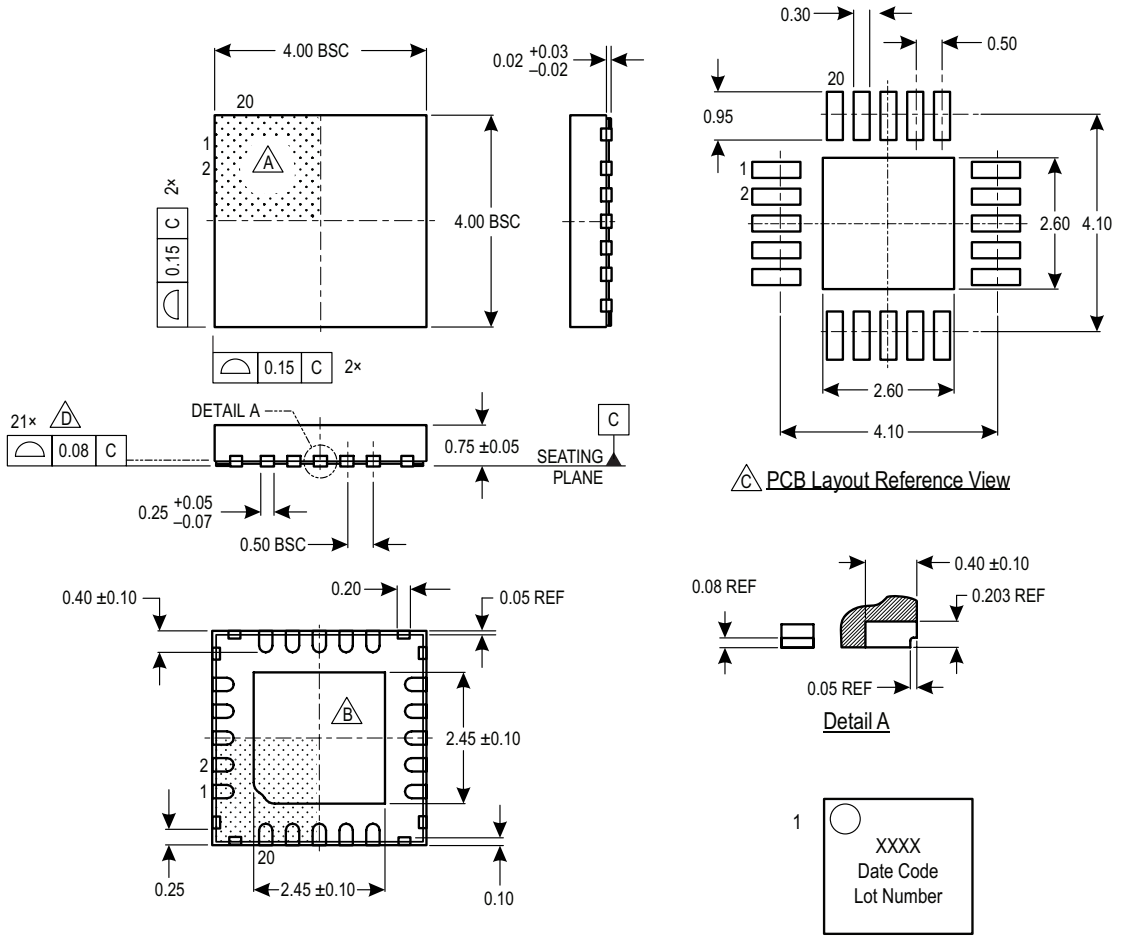
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WGGD)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area.

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion).

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-21BM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

D Coplanarity includes exposed thermal pad and terminals.

E Branding scale and appearance at supplier discretion.

E Standard Branding Reference View

Line 1: Part Number
Line 2: 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Pin 1 Dot top left
Center align

Figure 19: Package ES, 20-pin wettable flank QFN with exposed thermal pad

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Revision History

Number	Date	Description
–	June 11, 2019	Initial release
1	June 27, 2019	Updated Table 3 (page 33).
2	July 5, 2022	Updated package drawing (page 41)

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