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Q-RIFT PCB DESIGN FOR ACS37610 DIFFERENTIAL HALL CORELESS SENSOR TO MINIMIZE POSITION TOLERANCE ERROR AND IMPROVE THERMAL HANDLING

By Christian Kasparek, Simon Rock, and Cedric Gillet
Allegro MicroSystems

ABSTRACT

When designing and integrating new sensing elements into an application, the desire to reduce the cost and increase the power density of the system is a common theme that typically raises questions about the design of the geometry and the sensing elements:

- Traditional high-current sensors use a ferrous C-core to concentrate the magnetic field to a single Hall plate array on a sensor IC.
- New differential Hall sensing technologies enable removal of all ferrous concentrators.

The new, truly coreless approach is a well-known solution in applications for electric vehicles (xEVs), and it is commonly used for mid- to high-power xEV traction inverters where current can reach up to ~1500 A or higher through a busbar. By running current through the copper within the PCB, the same coreless, differential Hall technology can also be leveraged in lower-power applications, limited by the maximum current that can be run through the PCB. Compared to classic PCB notch designs, Allegro-patented PCB Q-Rift designs can more than double the maximum allowable current—ranging up to 300 A or a peak of 400 A—to serve a wider range of lower-power applications.

The Q-Rift PCB design from Allegro MicroSystems solves two major problems for engineers looking for a simple, high-power-density solution:

- Plug-and-play simplicity with minimal calibration: the Q-Rift design changes the geometries of each of the copper traces within the PCB directly below the sensor IC package. This not only permits the magnetic field to be properly coupled with the sensing elements but also allows specific designs that substantially reduce misplacement tolerance caused by pick-and-place manufacturing processes. This creates an easier plug-and-play solution that greatly simplifies or eliminates end-of-line calibration steps.
- Improved thermal handling by optimizing copper layers: by optimizing all copper layers of the PCB, more copper can be added to increase the conductor cross-sectional area. This allows the PCB to thermally handle up to 400 A. The Allegro Q-Rift PCB employs a design rule that can be applied to various board thicknesses and layer count.

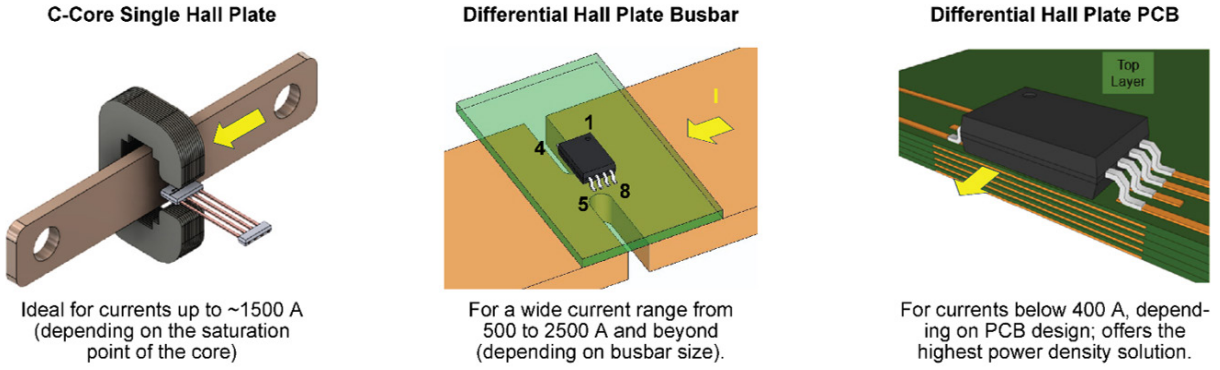

Figure 1: Examples of a busbar with a C-core (left), notched busbar with a coreless differential Hall sensor (middle), and coreless PCB design (right)

TECHNICAL DETAILS

DC Notch PCB and DC Q-Rift PCB

When moving from core-based to coreless sensors, the coupling factor (CF) of the sensor is typically lower for coreless sensors. This is because the core that concentrates the magnetic flux density on the Hall plates is missing. To counteract this, the PCB or busbar geometry is modified to increase the B-field at the Hall plates and thereby increase the CF. A common method is to use a notch where the Hall plates are located, which means that the width of the PCB or busbar is narrowed down. An illustration of a PCB with five layers and the sensor mounted on top is shown in Figure 1 (right).

A consequence of this modification is that the B-field is changing strongly in z-direction and the position tolerance in z-direction is therefore worse as compared to a core-based solution. Figure 2 shows the Bz-component of the B-field for a wide notch (8 mm). The notch width was chosen such that it matches the CF of the DC Q-Rift which is 250 mG/A. The figure also shows the location of the differential Hall plates in the nominal position, as well as ±0.25 mm tolerances in z-direction. The Bz-component shows a gradient where the Hall plates are located. Note that the scale is capped at ±0.01 T to show the gradient in the vicinity of the Hall plates.

Table 1 shows an overview of the position tolerance error of the DC Notch PCB. The position tolerance in x-direction (left to right in Figure 2) and z-direction (up and down in Figure 2) is analyzed for ±0.25 mm. The values in the table are coupling factor variations with respect to the nominal position. The maximum position tolerance error of the DC Notch PCB is larger than 5%.

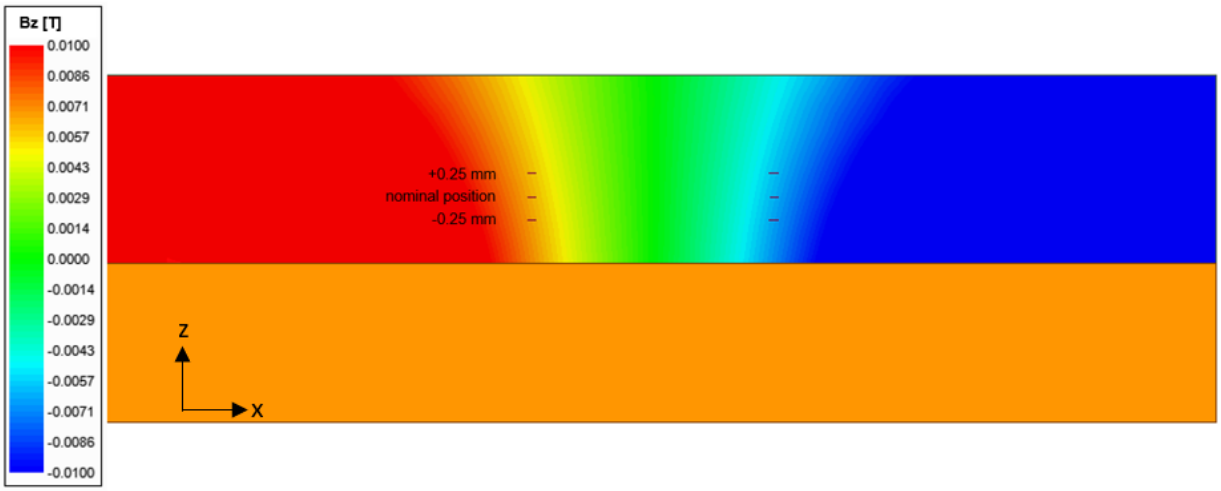

Figure 2: Bz-Field for a notch width of 8 mm. The scale is cut to ± 0.01 T to show the Bz gradient at the Hall plate locations.

Table 1: Summary of position tolerances of DC Notch and DC Q-Rift in x- and z-direction. All values are CF variations relative to the nominal position.

	DC Notch			DC Q-Rift		
dz (mm)	dx = –0.25 mm	dx = 0 mm	dx = 0.25 mm	dx = –0.25 mm	dx = 0 mm	dx = 0.25 mm
0.25	–5.0	–5.2	–5.0	–0.1	–1.1	–0.1
0	0.3	0.0	0.3	1.2	0.0	1.3
–0.25	5.4	5.0	5.4	0.3	–1.0	0.3

To reduce calibration effort for customers, a Q-Rift design was developed where each PCB layer was designed independently, to increase the uniformity of the Bz component at the Hall plate locations. The number of layers and the layer thicknesses were kept the same to better compare the results. Due to different requirements, a Q-Rift different layout was developed for DC and AC applications.

Figure 3 shows the Bz component of the DC Q-Rift and the nominal and ±0.25 mm positions. The Bz component is more uniform as compared to the notched PCB. Table 1 shows that the maximum difference of the CF has been reduced to 1%. This is a clear improvement as compared to the notched PCB and shows that the DC Q-Rift is much easier to handle than the notched PCB.

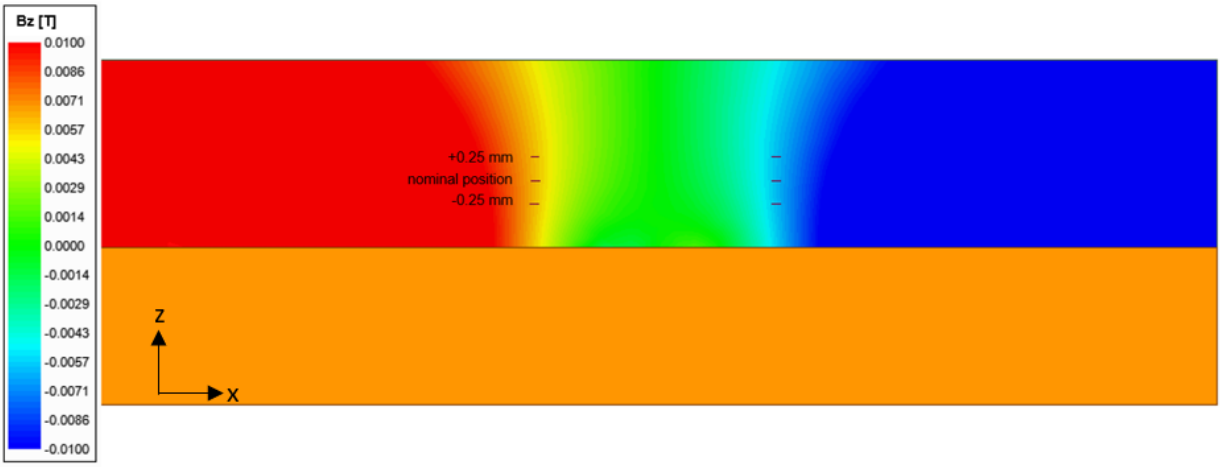

Figure 3: Bz-Field of a DC Q-Rift PCB. Bz-Field for a notch width of 8 mm. The scale is cut to ±0.01 T to show the Bz gradient at the Hall plate locations.

AC Notch and Q-Rift PCB

When designing a Q-Rift PCB for AC applications, not only the position tolerance is important, but also the frequency response. That means that the gain and phase should not change with frequency. This is a common issue due to the skin effect. To achieve a flat frequency response, the notch width is typically in the order of 3 mm. However, a narrow notch increases the position tolerance error in z-direction. [1]

Figure 4 shows the gain error and phase shift of an AC Q-Rift (blue) and Notch PCB (red). The AC Q-Rift was optimized for a low gain and phase error and a low placement tolerance error. The AC Notch was designed such that it matches the gain and phase error of the AC Q-Rift. The notch width is 4 mm. Figure 4 shows that the frequency response is very flat. Table 2 shows that the gain error is < 0.1% and the phase shift is < 1.5° up to 2 kHz for both PCBs. Therefore, both boards show an excellent AC performance.

Figure 5 shows the Bz component of the AC Notch PCB. Due to the narrow notch, which is required for a flat frequency response, there is a very strong gradient of the Bz component of the magnetic field. Table 3 shows that the maximum position tolerance error is as large as 16%. In contrast, the Bz component of the AC Q-Rift PCB shows a much weaker gradient, as shown in Figure 6. Indeed, Table 3 shows that the position tolerance error has been reduced to 1.6% which is a remarkable improvement.

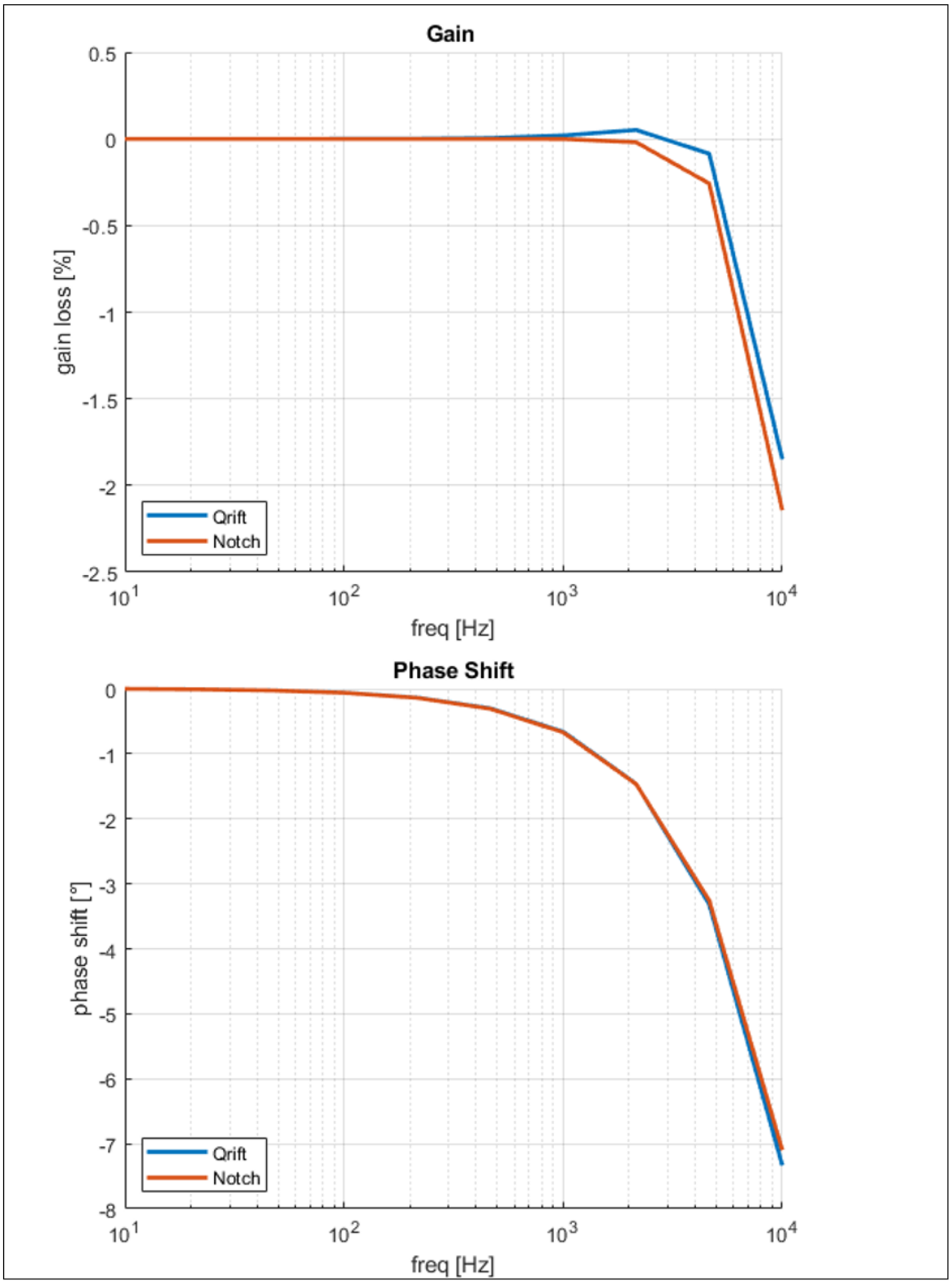

Figure 4: Frequency response of Notch (red) and Q-Rift(blue) PCB for AC applications.

Table 2: Comparison of frequency response of notch and Q-Rift

	AC Notch		AC Q-Rift	
Frequency (Hz)	**Gain (%)**	**Phase (°)**	**Gain (%)**	**Phase (°)**
10	0.00	0.00	0.00	0.00
22	0.00	–0.01	0.00	–0.01
46	0.00	–0.02	0.00	–0.02
100	0.00	–0.06	0.00	–0.06
215	0.00	–0.14	0.00	–0.14
464	0.00	–0.31	0.00	–0.30
1000	0.00	–0.67	0.02	–0.66
2154	–0.02	–1.47	0.05	–1.46
4642	–0.26	–3.26	–0.09	–3.31
10000	–2.14	–7.10	–1.85	–7.33

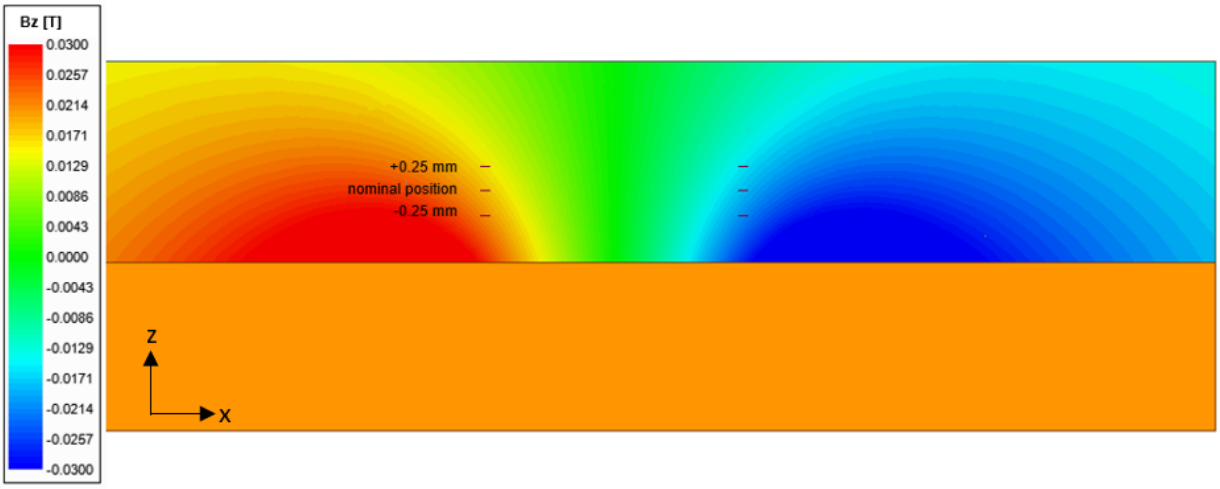

Figure 5: Frequency response of Notch (red) and Q-Rift(blue) PCB for AC applications.

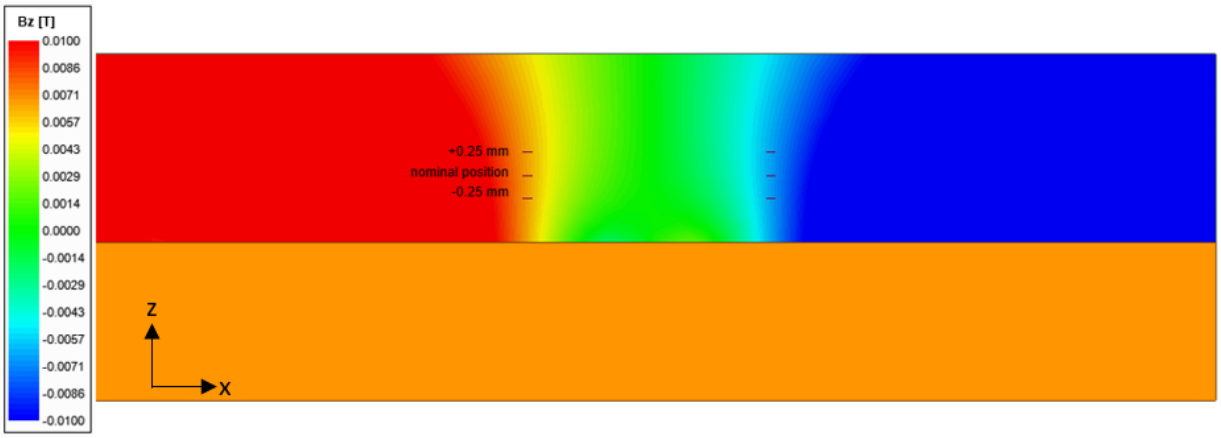

Figure 6: Bz component of AC-optimized Q-Rift shows a very uniform distribution.

Table 3: Summary of position tolerances of AC Notch and AC Q-Rift in x- and z-direction. All values are CF variations relative to the nominal position.

	AC Notch			AC Q-Rift		
dz (mm)	dx = –0.25 mm	dx = 0 mm	dx = 0.25 mm	dx = –0.25 mm	dx = 0 mm	dx = 0.25 mm
0.25	–14.6	–13.8	–14.6	–0.5	–1.6	–0.6
0	–0.9	0.0	–0.9	1.3	0.0	1.2
–0.25	15.3	16.2	15.3	1.0	–0.1	0.9

THERMAL PERFORMANCE

Another big advantage of the Q-Rift over the notched PCB is thermal performance. Figure 7 shows the temperature over time of the DC Q-Rift (blue) and notched PCB (red) if a continuous current of 155 A is applied at room temperature. The temperature is measured with an external temperature probe that is taped directly under the PCB where the Q-Rift and notch are located.

The temperature of the notched PCB increases strongly and reaches a plateau at 80°C after 5 min. In contrast, the temperature of the DC Q-Rift remains constant at room temperature over the full measurement time of over 17 min. Even if the current is increased to 300 A, the DC Q-Rift the temperature does not exceed 90°C (yellow). A similar thermal performance is expected for the AC Q-Rift. The thermal measurements demonstrate that the Q-Rift PCB can be operated at a much higher current than the notched PCB.

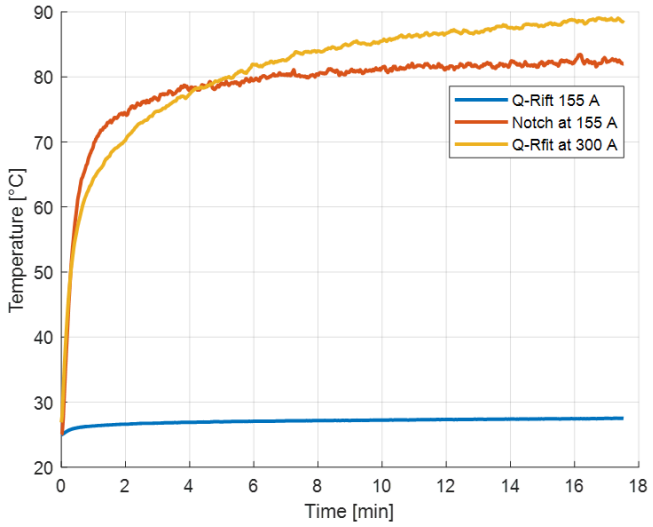

Figure 7: PCB Temperature over time after applying 155 and 300 A, respectively.

CONCLUSION

The Q-Rift PCB design shows an improved misplacement tolerance and can operate at higher current than a classical notched PCB. The easy assembly and mounting reduce the overall cost and effort for the manufacturer making traditional core-based sensing in the moderate current range obsolete.

REFERENCES

[1] Notched Busbar Design Guidelines For Coreless ACS37610 Differential Current Sensor. https://www.allegromicro.com/-/media/files/application-notes/an296231-acs37610-busbar-notch-guidelines.pdf

Revision History

Number	Date	Description
–	January 4, 2024	Initial release

955 PERIMETER ROAD • MANCHESTER, NH 03103 • USA
+1-603-626-2300 • FAX: +1-603-641-5336 • ALLEGROMICRO.COM