Automotive Multi-Output Voltage Regulator

FEATURES AND BENEFITS

- 6 to 45 V input range
- DC-to-DC buck converter with 5.7 V output
- Overcurrent protection with foldback, and undervoltage lockout (UVLO)
- Dual 5 V outputs
  - Digital 5 V ±2%, 200 mA
  - Analog 5 V, 200 mA
  - Short-to-supply protection on analog regulator
  - Analog to digital regulator output tracking <0.5% throughout operating temperature range

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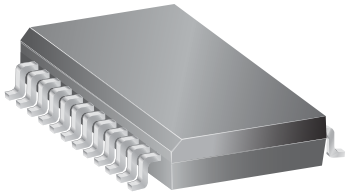
PACKAGE: 24-pin SOIC (suffix LB)



Not to scale

DESCRIPTION

The A8450 is a multi-output power supply intended for automotive applications. The A8450 operates from a wide input supply range and is designed to satisfy the requirements of high ambient temperature environments.

Four regulated voltage outputs provide multiple options. The 3.3 V regulator and the 1.2 to 3.3 V adjustable regulator can be used to power microcontroller or DSP cores, or for I/O, sensing, and A-to-D conversion. Two 5 V outputs, one digital and the other analog, feature output tracking within 0.5% of each other over the operating temperature range. In addition, the analog regulator is protected against short-to-battery conditions. All four regulators feature foldback current limit protection.

The device can be enabled or disabled using two input pins. The high voltage input, on the ENBAT pin, allows enable/disable using an engine ignition or battery switch signal. The logic-level input, on the ENB pin, allows enable/disable by microcontroller or DSP signals.

When disabled, the A8450 draws less than 10 µA of current. A POR (power-on-reset) block monitors the supply voltages and provides a reset signal, with an adjustable delay, for microcontroller or DSP resets. A separate fault pin signals TSD

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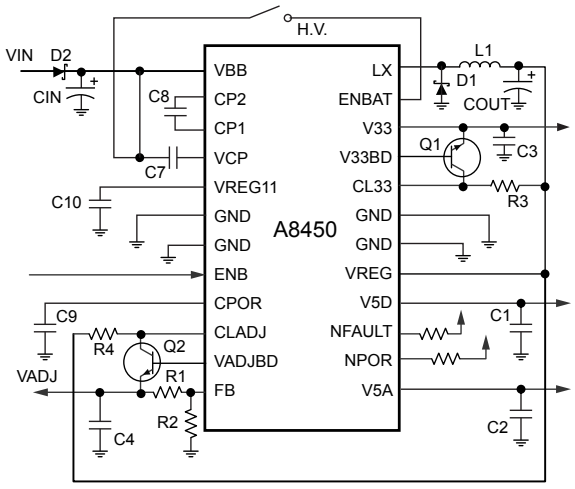
Typical Application



FEATURES AND BENEFITS (continued)

- 3.3 V linear regulator, with foldback current limit
- Adjustable 1.2 V to 3.3 V linear regulator, adjustable foldback current limit
- Ignition switch enable; Sleep mode
- 100% duty cycle operation for low input voltages
- Power OK output
- –40°C to 135°C ambient operating temperature range

DESCRIPTION (continued)

(thermal shutdown), 5 V analog short-to-supply, and 5 V analog or digital undervoltage.

The A8450 is supplied in a 24-pin SOIC-W package (part number suffix LB) with internally fused power ground pins for enhanced thermal performance. This provides an $R_{\theta JA}$ of 35°C/W on a 4-layer board (see chart on p. 5). The lead (Pb) free version has 100% matte tin leadframe plating.

SELECTION GUIDE

Part Number	Pb-free	Packing	Terminals	Package
A8450KLBTR-T	Yes	1000 pieces per 13-in. reel	24	SOIC-W surface mount, internally fused power ground pins (6-7, 18-19)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Units
Load Supply Voltage	V_{BB}	VBB pin	– 40	V
Analog Output	V_{5A}	V5A pin	–1 to 45	V
Logic Input Signal	V_{ENBAT}	ENBAT pin input	–0.3 to 45	V
	V_{ENB}	ENB pin input	–0.3 to 6.5	V
LX Voltage	V_{LX}	LX pin	–2 to V_{BB}	V
Operating Temperature Range	T_A	K range	–40 to 135	°C
Junction Temperature	$T_J(max)$		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

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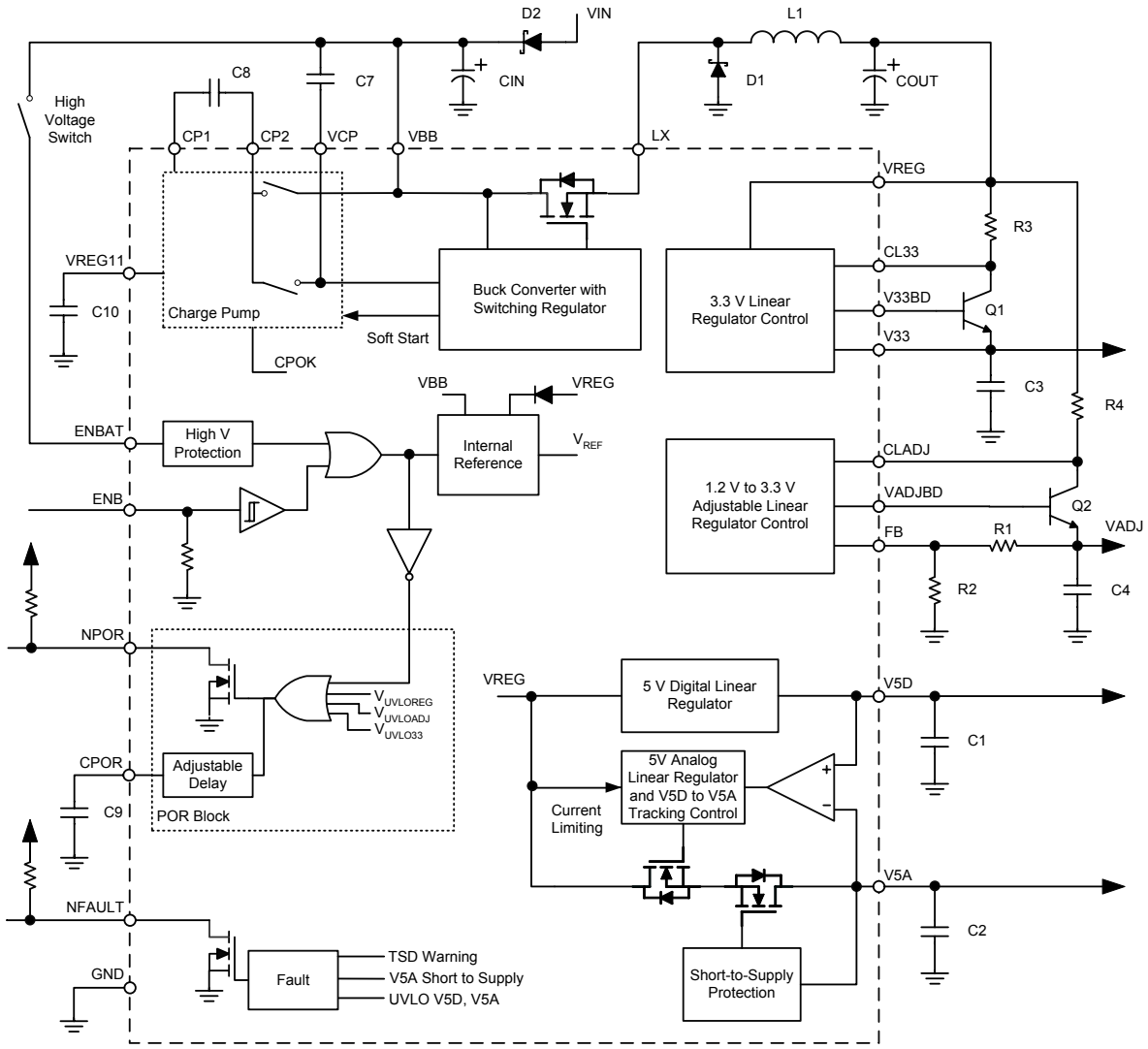
FUNCTIONAL BLOCK DIAGRAM



ID	Characteristics	Representative Device
C1, C2, C3, C4	1 µF, 25 V ceramic X7R	
COUT	100 µF, 35 V low-ESR electrolytic	UHC1V101M, Nichicon
CIN	47 µF, 63 V electrolytic	
C7, C8	0.1 µF, 50 V ceramic X7R (for 14 V applications), or 0.1 µF, 100 V ceramic X7R (for 42 V applications)	
C10	0.22 µF, 10 V X7R	
D1, D2	1 A, 40 V Schottky (for 14 V applications)	EKO4, Sanken
L1	100 µH, 1.2 A	D03316HT, Coilcraft
Q1, Q2 pass transistors	npn transistor, h_{FE} > 50	MPSW06

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ELECTRICAL CHARACTERISTICS: Valid at T_A = –40ºC to 135°C, V_{BB} = 6 to 45 V, V_{ENB} = 5 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Quiescent Current	I_{BB}	Enabled mode: V_{ENBAT} or V_{ENB} = HIGH, I_{OUT} = 0 mA: V_{BB} = 14 V	–	6	10	mA
		Enabled mode: V_{ENBAT} or V_{ENB} = HIGH, I_{OUT} = 0 mA; V_{BB} = 6 V	–	10	15	mA
		Disabled mode: V_{ENBAT} and V_{ENB} = LOW	–	–	10	µA
Regulated Output Voltage	V_{REG}	I_{LOAD} = 550 mA = $I_{LOADV5D}$ + $I_{LOADV5A}$ + $I_{LOADV33}$ + $I_{LOADV-ADJ}$; V_{BB} > 6.5 V	5.50	–	5.80	V
		Dropout: 6 V ≤ V_{BB} < 6.5 V	5.00	–	5.80	V
Buck Switch On-Resistance	R_{DSON}	T_J = 25°C	–	415	500	mΩ
		T_J = 135°C	–	650	750	mΩ
Buck Switch Current Limit	I_{DSLIM}		1.0	1.2	2.2	A
DC-to-DC Fixed Off-Time	t_{OFF}	V_{BB} = 14 V	–	4.75	–	µs
Soft Start Time	t_{SS}	V_{BB} = 14 V	5	10	15	ms
LOGIC INPUTS						
ENBAT Logic Input Voltage	V_{ENBAT}	HIGH input level	2.7	–	45	V
		LOW input level	–0.3	–	0.8	V
ENBAT Input Current	I_{ENBAT}	HIGH input level, V_{ENBAT} = 45 V	–	–	300	µA
		HIGH input level, V_{ENBAT} = 14 V	–	–	70	µA
		LOW input level, V_{ENBAT} = 0.8 V	–1	–	10	µA
ENB Logic Input Voltage	V_{ENB}	HIGH input level	2.7	–	6.5	V
		LOW input level	–0.3	–	0.8	V
ENB Input Current	I_{ENB}	HIGH input level, V_{ENB} ≥ 2.7 V	–	–	50	µA
		LOW input level, V_{ENB} ≤ 0.8 V	–1	–	10	µA
LINEAR REGULATOR OUTPUTS*						
V5D Output Voltage	V_{OUTV5D}	1 mA ≤ $I_{LOADV5D}$ ≤ 200 mA	4.9	5.0	5.1	V
V5A Output Voltage	V_{OUTV5A}	1 mA ≤ $I_{LOADV5A}$ ≤ 200 mA	4.9	5.0	5.1	V
V33 Output Voltage	V_{OUTV33}		3.234	3.300	3.366	V
V5A to V5D Tracking	V_{TRACK}	50 mA ≤ $I_{LOADV5A}$, $I_{LOADV5D}$ ≤ 200 mA; V_{BB} > 6.5 V	–25	–	25	mV
V5D Current Limit	$I_{OUTV5DLIM}$		200	300	–	mA
V5A Current Limit	$I_{OUTV5ALIM}$		200	300	–	mA
Base Drive Output Current	I_{BD}	1 V ≤ $V_{OUTVADJ}$, V_{OUTV33} ≤ 4 V	5.0	10.0	16.0	mA
Feedback Voltage	V_{FB}		1.16	1.20	1.24	V
Feedback Input Bias Current	I_{FB}		–400	–100	100	nA

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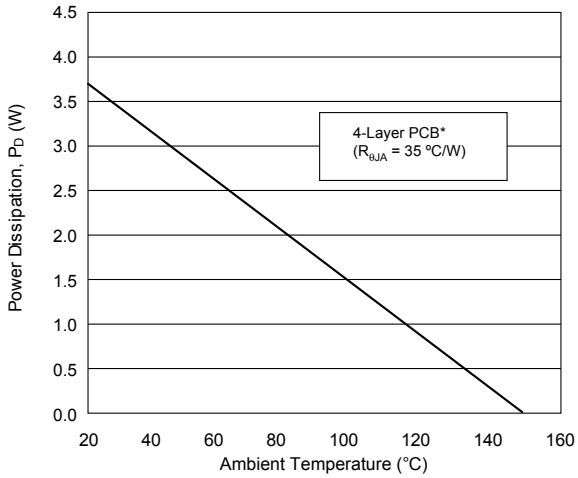
ELECTRICAL CHARACTERISTICS (continued): Valid at T_A = –40ºC to 135°C, V_{BB} = 6 to 45 V, V_{ENB} = 5 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
PROTECTION						
NFAULT, NPOR Output Voltage	V_{ERRON}	Fault asserted; I_{NFAULT}, I_{NPOR} = 1 mA	–	–	400	mV
NFAULT, NPOR Leakage Current	I_{ERROFF}	V_{NFAULT}, V_{NPOR} = 5 V	–	–	1	µA
POR Delay	t_{POR}	C9 = 0.47 µF	65	100	135	ms
V33 Undervoltage Threshold	$V_{UVLOV33}$	V_{33} rising	2.80	2.95	3.10	V
		V_{33} falling	2.75	2.90	3.05	V
V33 Hysteresis	V_{HYSV33}		–	80	–	mV
V5A, V5D Undervoltage Threshold	V_{UVLOV5}	V5A, V5D rising	4.36	4.50	4.75	V
		V5A, V5D falling	4.24	4.38	4.63	V
V5A, V5D Hysteresis	V_{HYSV5}		–	125	–	mV
VADJ Undervoltage Threshold	$V_{UVLOVADJ}$	V_{FB} rising	1.02	1.07	1.12	V
		V_{FB} falling	0.97	1.02	1.07	V
VADJ Hysteresis	$V_{HYSVADJ}$	At FB pin	–	70	–	mV
VADJ, V33 Overcurrent Threshold	V_{OC}		175	200	225	mV
VREG Undervoltage Threshold	$V_{UVLOVREG}$		4.94	5.15	5.36	V
Thermal Warning Threshold	T_{JTW}	T_J rising	–	160	–	°C
Thermal Shutdown Threshold	T_{JTSD}	T_J rising	–	175	–	°C
Thermal Shutdown Hysteresis	T_{HYSTSD}	Recovery period = $T_{JTSD} - T_{JTW}$	–	15	–	°C

*Linear regulator output specifications are only valid when V_{REG} is in regulation ($V_{BB} \geq 6.5$).

Power Dissipation Versus Ambient Temperature



*In still air; mounted on PCB based on JEDEC high-conductance standard PCB (JESD51-7; High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages); data on other PCB types is provided on the Allegro website.

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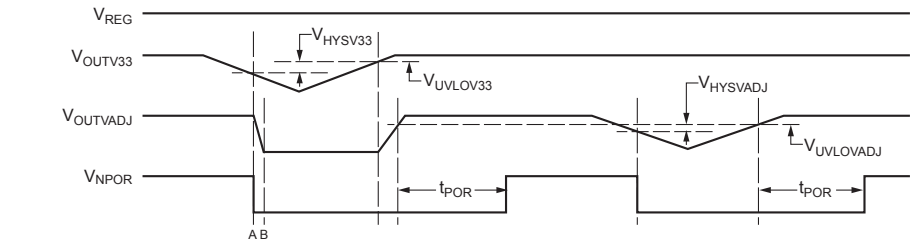
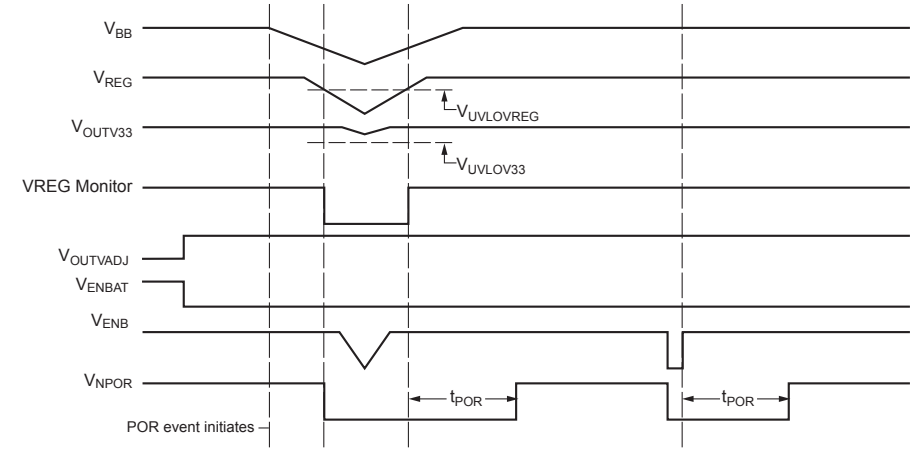
TIMING DIAGRAMS



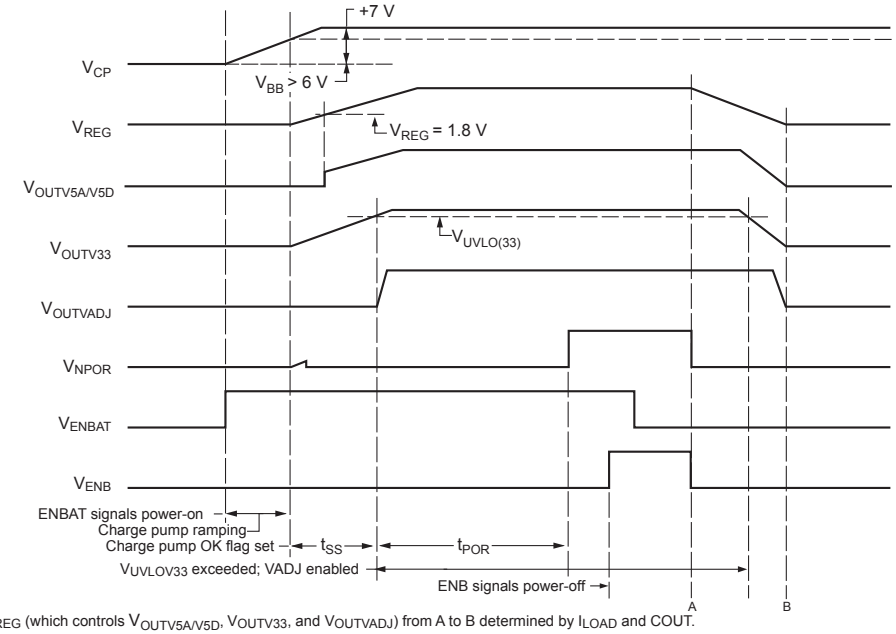
Slope of V_{OUTV33} and $V_{OUTVADJ}$ from A to B determined by I_{LOAD} and output capacitor (C3, C4).

Figure 1a. NPOR fault due to undervoltage lockout on the V33 or FB pins



V33 can sustain regulation with normal load by bulk capacitor (COUT) on V_{REG}.

Figure 1b. Power-off using V_{BB}



Slope of V_{REG} (which controls $V_{OUTV5A/V5D}$, V_{OUTV33}, and $V_{OUTVADJ}$) from A to B determined by I_{LOAD} and COUT.

Figure 1c. Power-on using ENBAT, followed by power-off using ENB

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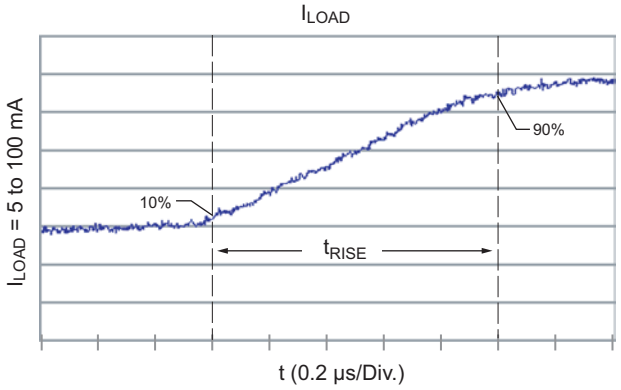
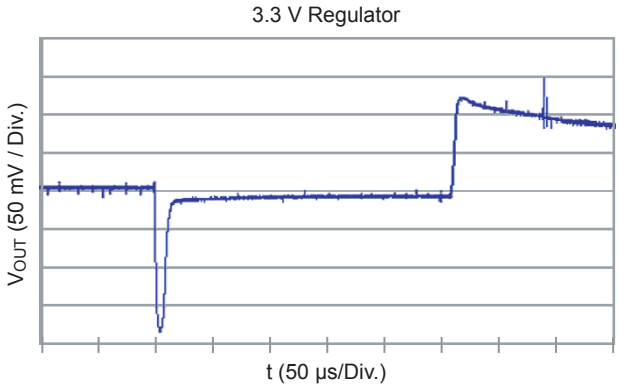
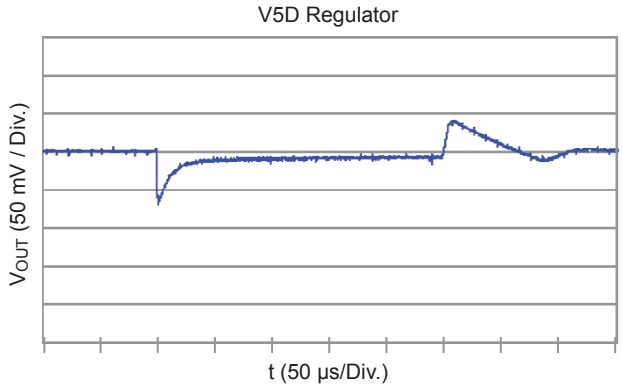
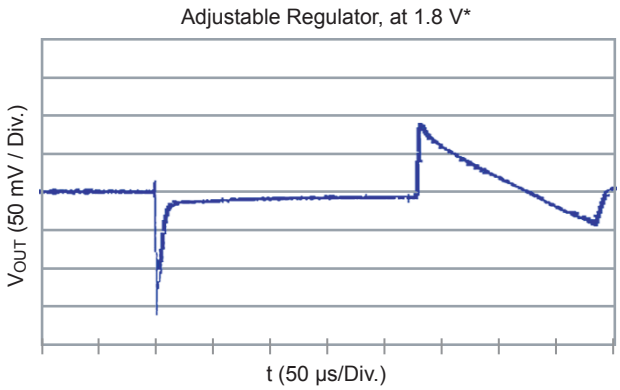
LOAD TRANSIENTS DIAGRAMS

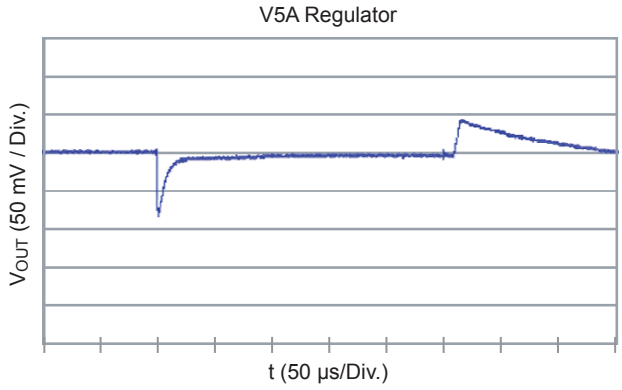
V_{IN} = 12 V; I_{LOAD} = 100 mA; T_A = 25°C; ac-coupled; C1, C2, C3 and C4 = 1 µF











*For the adjustable regulator, the transient load response is improved as the voltage is reduced. This is due to the ability of the regulator to provide more base drive (V_{ADJBD}) because of more available voltage. When the adjustable regulator approaches 3.3 V, its transient load response is equivalent to the response of the V33 regulator.

For all regulators, load transients can be improved by increasing the output capacitance (C1, C2, C3, and C4). In order to keep ESR down it is best to use ceramic type capacitors. However, large values in ceramic type capacitors are either not available or very expensive. If larger values are needed, above 22 µF, electrolytic capacitors with low ESR ratings can be used. Performance can be improved further by adding a 1 µF ceramic in parallel with the electrolytic.

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FUNCTIONAL DESCRIPTION

Buck Converter with Switching Regulator. A current-mode, variable frequency buck DC-to-DC converter and switching regulator are integrated in the A8450, as shown in figure 2. This feature allows the device to efficiently handle power over a wide range of input supply levels. The DC-to-DC converter outputs 5.7 V typical and has an overcurrent limit of 1.2 A typical.

The converter employs a soft-start feature. This ramps the converter output voltage and limits the maximum demand on V_{REG} by controlling the inrush current required at power-on to charge the external capacitor, COUT, and any DC load.

An internal charge pump provides gate drive for the N-channel MOSFET buck switch. A 100% duty cycle is implemented when using low V_{BB} input voltages.

At V_{BB} lower than 12 V, off-time, t_{OFF}, is reduced, as shown in figure 3. This reduction keeps the switching frequency, f_{PWM}, within a reasonable range and lowers the ripple current. Lowering the ripple current at low V_{BB} levels prevents degradation of linear regulator headroom due to V_{REG} ripple voltage.

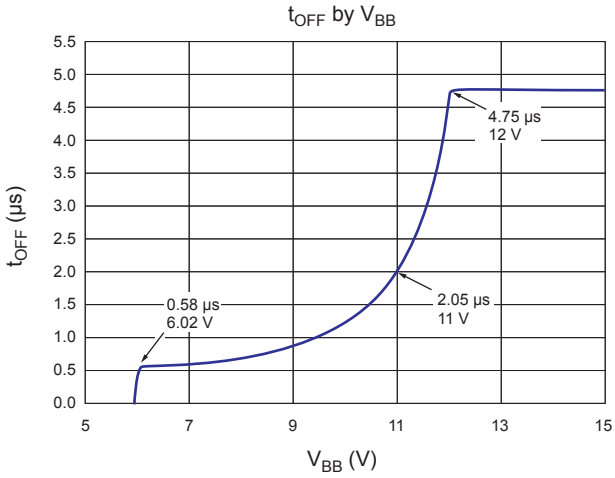

Figure 3. When VBB falls below 12 V, t_{OFF} decreases

5 V Linear Regulators. Two 5 V medium-power linear regulators are provided. These low-dropout regulators feature foldback current limiting for short-to-ground protection. When a direct short is applied to the regulator output, either V5A or V5D, the current folds back

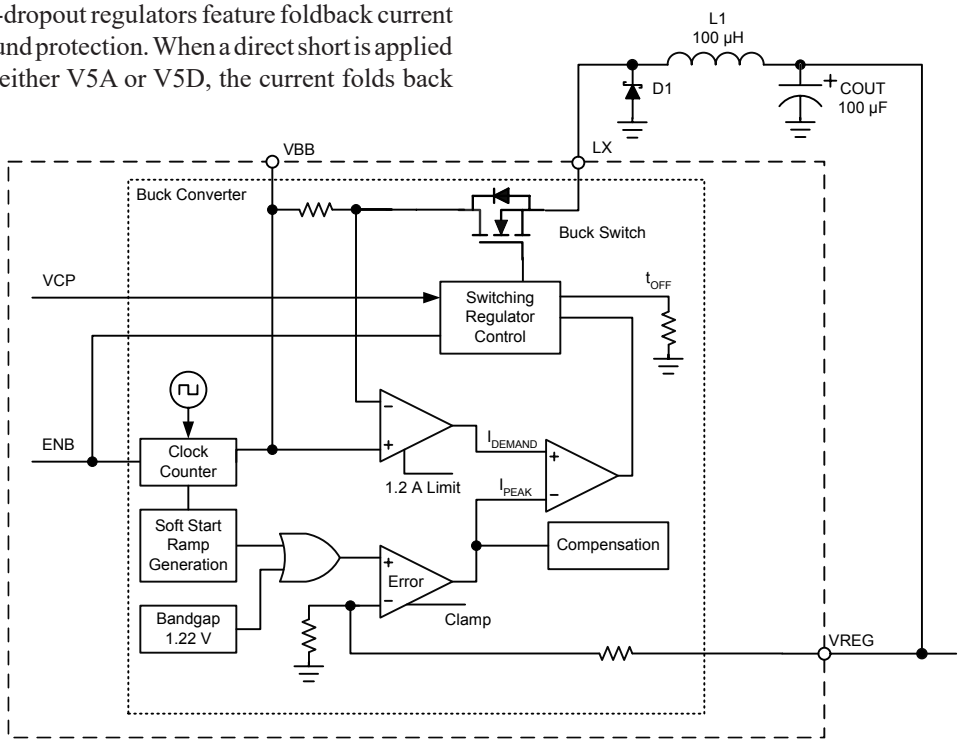

Figure 2. Buck converter with switching regulator

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to 0 V at 50 mA, as shown in figure 4a. The voltage recovers to its regulated output when the short is removed.
The V5A and V5D regulators track each other during power-on, and when the device is enabled and ramped up out of disabled mode, the regulators will start to track when V_{REG} reaches approximately 1.8 V. These regulators are guaranteed to track to within 0.5% of each other under normal operating conditions.

3.3 V and Adjustable Linear Regulators. Two additional linear regulators, one that outputs at 3.3 V, and another that has a 1.2 V to 3.3 V adjustable output, can be implemented using external npn pass transistors. The output voltage of the adjustable regulator, $V_{OUTVADJ}$ (V), is set by the values of the output resistors, R1 and R2 (Ω). It can be calculated as

$$V_{OUTVADJ} = V_{FB} (1+R1/R2)$$

where V_{FB} (V) is the voltage on the feedback pin, FB.

Additional pins, CL33 and CLADJ, are provided for setting current limits. These are used to protect the external pass transistors from a short-to-ground condition. The current limit setting, I_{CL} (mA), is calculated using the formula

$$I_{CL} = V_{OC}/R_{RCL}$$

where RCL (Ω) is the current-limiting resistor corresponding to that regulator (R3 for the 3.3 V regulator, and R4 for the adjustable regulator). When I_{CL} is exceeded, the maximum load current through that regulator is folded back to 40% of I_{CL} ±10%, as shown in figure 4b. If current limiting is not needed, the CL33 and CLADJ pins should be shorted to the VREG pin.

Disabled Mode. When the two input signal pins, ENBAT and ENB, are pulled low, the A8450 enters disabled mode. This is a sleep mode, in which all internal circuitry is disabled in order to draw a minimal current from VBB. When either of these pins is pulled high, the device is enabled. When emerging from disabled mode, the buck converter switching regulator does not operate until the charge pump has stabilized (≈300 µs).
Enabled Mode. When one or both signal input pins, ENBAT and ENB, are in the high state, the A8450 is enabled.
ENBAT is an edge-triggered enable (logic 1 ≥ 2.7 V), which is used to enable the A8450 in response to a high-voltage signal, such as from an automobile ignition or battery switch. In this capacity, ENBAT is used only as a momentary switch to wake up the device. If there is no need for a high-voltage signal, ENBAT can be pulled low continuously.
ENB is used to initiate the reset of the device. If ENBAT is pulled

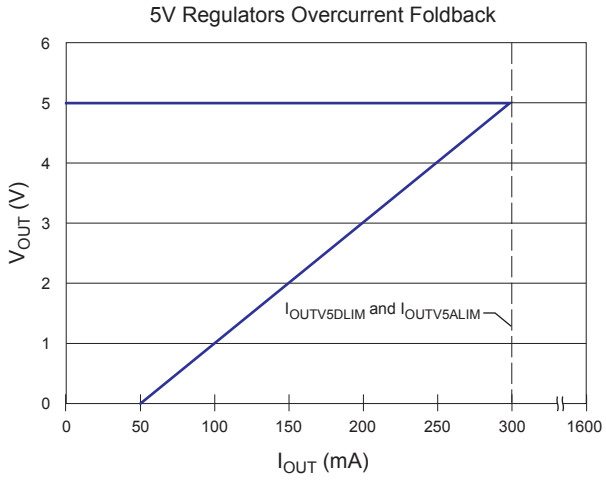

Figure 4a. Linear foldback to 50 mA. Foldback occurs at the typical current limit for the 5 V regulator.

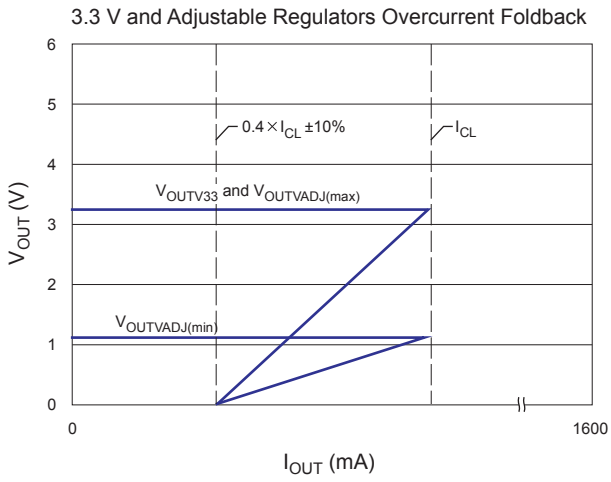

Figure 4b. Linear foldback to a percentage of I_{CL}. Foldback occurs at the current limit setting for the regulator.

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low, ENB acts as a single reset control.

Diagnostics. An open drain output, through the NFAULT pin, is pulled low to signal to a DSP or microcontroller any of the following fault conditions:

- V5A, the 5 V analog regulator output, is shorted to supply
- Either or both V5A and the V5D regulator outputs are below their UVLO threshold, V_{UVLOV5}
- Device junction temperature, T_J, exceeds the Thermal Warning threshold, T_{JTW}

Charge Pump. The charge pump generates a voltage above V_{BB} in order to provide adequate gate drive for the N-channel buck switch. A 0.1 µF ceramic monolithic capacitor, C7, should be connected between the VCP pin and the VBB pin, to act as a reservoir to run the buck converter switching regulator.

V_{CP} is internally monitored to ensure that the charge pump is disabled in the case of a fault condition. In addition, a 0.1 µF ceramic monolithic capacitor, C8, should be connected between CP1 and CP2.

Power On Reset Delay. The POR block monitors the supply voltages and provides a signal that can be used to reset a DSP or microcontroller. A POR event is triggered by any of the following conditions:

- Either V33 or VADJ is pulled below its UVLO threshold, $V_{UVLOV33}$ or $V_{UVLOVADJ}$. This occurs if the current limit on either regulator, V_{OC}, is exceeded. It also occurs if the VREG voltage falls below V_{REGMON}, due to current exceeding I_{DSLIM}.
- Both input signal pins, ENB and ENBAT, are pulled low. This immediately pulls the NPOR pin low, indicating that the device is beginning a power-off sequence. In addition, the buck converter switching regulator is disabled, and the VREG supply begins to ramp down. The rate at which V_{REG} decays is dependent on the total current draw, I_{LOAD}, and value of the output capacitors (C1, C2, C3, and C4).
- V_{REG} drops below its UVLO threshold, $V_{UVLOVREG}$.
- During any normal power-on, $V_{OUTVADJ}$ falls below $V_{UVLOVADJ}$, triggering a POR.

An open drain output, through the NPOR pin, is provided to signal a POR event to the DSP or microcontroller. The reset occurs after an adjustable delay, t_{POR}, set by an external capacitor, C9, connected to the CPOR pin. The value of t_{POR} (ms) is calculated using the following formula

$$t_{POR} = 2.13 \times 10^5 \times C_{CPOR}$$

where C_{CPOR} (µF) is the value of the C9 capacitor.

A POR can be forced without a significant drop in the supply voltage, V_{REG}, by pulsing low both the ENB and the ENBAT pins. However, pulse duration should be short enough so that V_{REG} does not drop significantly.

Thermal Shutdown. When the device junction temperature, T_J, is sensed to be at T_{JTSD} (≈15°C higher than the thermal warning temperature, T_{JTW}), a fault is indicated at the NFAULT pin. At the same time, a thermal shutdown circuit disables the buck converter, protecting the A8450 from damage.

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APPLICATION INFORMATION

Component Selection

Output Inductor (L1). This inductor must be rated to handle the total load current, I_{LOAD}. In addition, the value chosen must keep the ripple current to a reasonable level. A typical selection is a power inductor rated at 100 µH and 1.3 A.

The worse-case ripple current, $I_{RIPPLE(max)}$ (mA), can be calculated as

$$I_{RIPPLE(max)} = V_{L1OFF} \times t_{OFF} / L_{L1}$$

where L_{L1} (µH) is the inductance for the selected component, and V_{L1OFF} is the voltage (V) through the inductor when the A8450 is in the quiescent state

$$V_{L1OFF} = V_{REG(max)} + V_{D1} + (I_{LOAD} \times R_{L1})$$

where V_{D1} (V) is the voltage drop on diode D1, I_{LOAD} (mA) is the total load current, and R_{L1} is the specified DC resistance (Ω) for the selected inductor at its rated temperature.

The frequency, f_{PWM} (Hz), of the switching regulator in the buck converter can then be estimated by

$$f_{PWM} = 1/(t_{ON} + t_{OFF})$$

where t_{ON} (µs) is calculated as

$$t_{ON} = I_{RIPPLE(max)} \times L_{L1} / V_{L1ON}$$

and V_{L1ON} (V) as

$$V_{L1ON} = V_{BB} - (I_{LOAD} \times R_{DSON(max)}) - (I_{LOAD} \times R_{L1}) - V_{REG(max)}$$

Example
Given a typical application with V_{BB} = 14 V, t_{OFF} = 4.75 µs, and I_{LOAD} = 550 mA. (Note that the value for t_{OFF} is constant for V_{BB} > 12 V, as shown in figure 3.)

Given also a 100 µH power inductor rated at 400 mΩ for 125ºC. (Note that temperature ratings for inductors may include self-heating effects. If a 125ºC rating includes a self-heating temperature rise of 20ºC at maximum current, then the actual ambient temperature, T_A, cannot exceed 105ºC.)

$$V_{L1OFF} = 5.8 + 0.8 + (0.550 \times 0.400) = 6.821 \text{ V}$$

$$I_{RIPPLE(max)} = 6.821 \times 4.75 / 100 = 0.324 \text{ A}$$

$$V_{L1ON} = 14 - (0.550 \times 0.750) - (0.550 \times 0.400) - 5.8 = 7.56 \text{ V}$$

$$t_{ON} = 0.324 \times 100 / 7.56 = 4.3 \text{ µs}$$

$$f_{PWM} = 1/(4.3 + 4.75) = 111 \text{ kHz}$$

In the case of a shorted output, the buck converter could reach its internal current limit, I_{DSLIM}, of 1.2 A typical. To ensure safe operation, the I_{SAT} rating for the selected inductor should be greater than 1.4 A. However, if the external current limit resistors, R3 and R4, selected for the 3.3 V and adjustable (1.2 V to 3.3 V) regulators, are rated such that the total inductor current, I_{LOAD}, could never reach that internal current limit, then an inductor can be selected that has an I_{SAT} rating closer to the calculated output current of the device, I_{LOAD}, plus the maximum ripple current, $I_{RIPPLE(max)}$.

Higher inductor values can be chosen to lower I_{RIPPLE}. This may be an option if it is desired to increase the total maximum current that is drawn from the switching regulator. The maximum total current available, I_{LOAD} (mA), is calculated as

$$I_{LOAD} = I_{DSLIM} - (I_{RIPPLE(max)} / 2)$$

Catch Diode (D1). The Schottky catch diode should be rated to handle 1.2 times the maximum load current, I_{LOAD}, because the duty cycle at low input voltages, V_{BB}, can be very close to 100%. The voltage rating should be higher than the maximum input voltage, $V_{BB(max)}$, expected during any operating condition.

VREG Output Capacitor (COUT). Voltage ripple in the VREG output is the main consideration when selecting the VREG output capacitor, COUT. The peak-to-peak output voltage ripple, $V_{RIPPLE(p-p)}$ (mV), is calculated as

$$V_{RIPPLE(p-p)} = I_{RIPPLE} \times ESR_{COUT}$$

with ESR in ohms. It is recommended that the maximum level of $V_{RIPPLE(p-p)}$ be less than 200 mV.

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For electrolytic output capacitors, a low-ESR type is recommended, with a minimum voltage rating of 10 V. However, because ESR decreases with voltage, the most cost-effective choice may be a capacitor with a higher voltage rating.

Regulator Output Capacitors (C3 and C4). The output capacitors used with the 3.3 V regulator (C3) and the 1.2 V to 3.3 V adjustable regulator (C4), should be 1 µF or greater X7R (5% tolerance) ceramic or equivalent capacitors, with a maximum capacitance change of ±15% over a temperature range of –55ºC to 125ºC.

The ESR of these capacitors does not affect the outputs of the corresponding regulators. If a greater capacitance is used, the regulators have improved ripple rejection at frequencies greater than 100 kHz.

Pass Transistors (Q1 and Q2). The pass transistors used to implement the 3.3 V regulator and the 1.2 V to 3.3 V adjustable regulator must ensure the following:

- **Stable operation.** The cutoff frequency for the control loops of the regulators is 100 kHz. Transistors must be selected that have gain bandwidth product, f_T (kHz), and beta, h_{FE} (A), ratings such that

$$f_T / h_{FE} > 100 \text{ kHz}$$

- **Adequate base drive.** It is acceptable to use a lower level of current gain, h_{FE}, for lower total load currents, I_{LOAD}. The lower limit for I_{LOAD} is limited by the minimum base current for the A8450, $I_{BD(min)}$, and the minimum h_{FE} of the pass transistor, such that

$$I_{LOAD} = I_{BD(min)} \times h_{FE(min)}$$

  Note that h_{FE} is dependent on operating temperature. Lower temperatures decrease h_{FE}, affecting the current capacity of the transistor.

- **Packaged for sufficient power dissipation.** In order to ensure appropriate thermal handling, the design of the application must take into consideration the thermal characteristics of the PCB where the A8450 and pass transistors are mounted, the ambient temperature, and the power dissipation characteristics of the transistor packages. In general, the power dissipation, P_D (mW), is estimated by

$$P_D = (V_{REG} - V_{OUT}) \times I_{LOAD}$$

  For a typical application where V_{REG} = 5.8 V, V_{OUT} = 2.5 V, and I_{LOAD} = 190 mA

$$P_D = (5.8 - 2.5) \times 190 = 627 \text{ mW}$$

Adjusting Pass Transistor Power Dissipation

Transistors are manufactured in a wide variety of package types, and the thermal dissipation efficiencies of the packages can vary greatly. In general, increasing thermal efficiency can also increase cost substantially. Selecting the package to closely match operating conditions is important to optimizing application design and cost.

Even when using a thermally enhanced package, it remains difficult to provide high current to a load at high ambient operating temperatures. Depending on the load requirements, using drop resistors, as shown in figure 5, may be necessary to protect the pass transistor from overheating.

The output current-limiting resistors, RCL (corresponding to R3 and R4), will drop between 175 mV and 225 mV at the highest current output, I_{LOAD}. Assuming no additional resistance, the voltage dropped, V_{DROP} (mV), on each pass transistor is

$$V_{DROP} = V_{REG} - V_{RCL} - V_{OUT}$$

This can be substituted into the power dissipation formula

$$P_D = V_{DROP} \times I_{LOAD}$$

Given a typical application where V_{REG} = 5.8 V, V_{RCL} = 0.175 V,

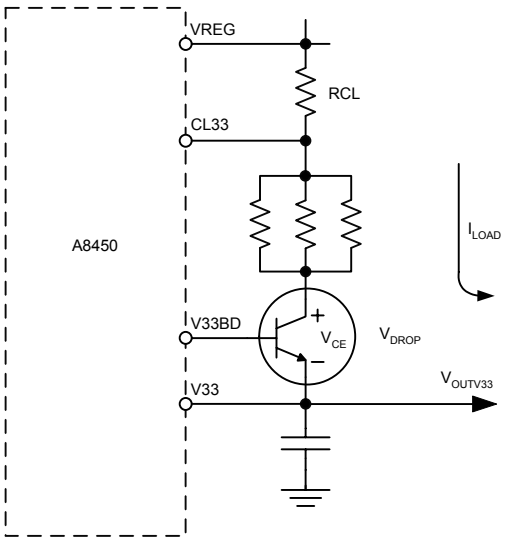

Figure 5. Placement of drop resistors for thermal protection; example shown is for the 3.3 V regulator.

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V_{OUT} = 3.3 V, and I_{LOAD} = 350 mA, then P_D is approximately 814 mW.

P_D can be used to estimate the minimum required operating temperature rating for the transistor. The ability of a package to dissipate heat is approximated by the thermal resistance from the die (junction) to the ambient environment, $R_{\theta JA}$ (°C/W). This includes the significant effect of dissipation through the package leads and the PCB on which the transistor is mounted, and the state of the ambient air. The typical rating for a DPAK package is 32°C/W. The expected self-induced temperature rises in the package, ΔT_J (°C), given P_D = 0.814 W, is approximated as

$$\Delta T_J = P_D \times R_{\theta JA} = 26°C$$

In automotive applications, where under-the-hood ambient temperatures can exceed 125°C, the pass transistor would have to be rated to provide the required beta at ≥151°C, plus a safe operating margin.

For a selected transistor, V_{CE} can change depending on current, temperature, and transistor beta. Typically, transistors are rated at a minimum beta at a defined V_{CE}. However, V_{CE} should be calculated with some margin so there is always enough headroom to drive the device at the desired load.

To provide an operating margin, or if a lower-value RCL is required, voltage drop resistors, RDROP, can be added to the circuit, between the RCL and the transistor (figure 5). It is also important to consider tolerances in resistance values and V_{REG}. The level of $V_{REG(min)}$ is 5.6 V, at which level P_D is reduced, but also the voltage available for V_{CE} is reduced. Calculating maximum and minimum voltage drops is useful in determining the values of the drop resistors.

The required drop resistor value, R_{RDROP}, can be determined in terms of the voltage drops across each component of the circuit, as shown in the following formula

$$V_{DROP} \geq V_{OUT}$$

where

$$V_{DROP} = V_{REG} - V_{RCL} - V_{RDROP} - V_{CE}$$

Assume that $V_{REG(max)}$ = 5.8 V and $V_{OUT(max)}$ = 3.3 V. Assume also that T_A = 125°C, and V_{CE} = 1V (as specified for the MPSW06 npn transistor, beta = 300 at 125°C).

In order to determine the resistance values for the current-limiting and drop resistors, V_{RCL} and V_{DROP} can be expressed in terms of $I_{LOAD(lim)}$

$$V_{RCL} = (I_{LOAD(lim)} \times R_{CL})$$

$$V_{RDROP} = (I_{LOAD(lim)} \times R_{RDROP})$$

Assume a typical I_{LOAD} = 350 mA. However, under normal operating conditions, the current limit set by RCL would be higher than the expected normal current, so assume $I_{LOAD(lim)}$ = 0.400 A and R_{CL} = 44 Ω. Substituting to determine V_{RCL}

$$V_{RCL} = 0.400 \times 0.44 = 0.176 \text{ V}$$

We can now solve for R_{RDROP} and then V_{DROP}

$$V_{REG} - V_{RCL} - (I_{LOAD} \times R_{RDROP}) - V_{CE} \geq V_{OUT}$$

$$5.8 - 0.176 - (0.4 \times R_{RDROP}) - 1 \geq 3.30 \text{ V}$$

therefore

$$R_{RDROP} \geq 3.31 \text{ Ω}$$

and

$$V_{RDROP} = 0.4 \times 3.31 = 1.3 \text{ V}$$

Using four 0.25 W resistors valued at 14.7 Ω in parallel will drop 1.3 volts.

Using the drop resistors as calculated above, the power dissipation in the transistor, P_D (W) is reduced to

$$P_D = I_{LOAD(lim)} \times (V_{REG} - V_{RCL} - V_{RDROP} - V_{OUT})$$

$$= 0.400 \times (5.8 - 0.176 - 1.3 - 3.3) = 0.410 \text{ W}$$

and

$$\Delta T_J = P_D \times R_{\theta JA} = 13°C$$

The power dissipated in the transistor is significantly reduced. A transistor in a power package with an $R_{\theta JA}$ of 32°C/W at 400 mA (a 50 mA margin) undergoes a temperature rise of 13°C with the drop resistors, as opposed to a similar transistor at 350 mA rising 26°C without drop resistors. At high output currents, properly selected drop resistors can protect the external pass transistor from overheating.

A8450 Power Dissipation. The A8450 is designed to operate in applications with high ambient temperatures. The total power dissipated in the device must be considered in conjunction with the thermal dissipation capabilities of the PCB where the A8450 is mounted, as well as the capabilities of the device package itself.

The ability of a package to dissipate heat is approximated by

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the thermal resistance from the die (junction) to the ambient environment, $R_{\theta JA}$ (°C/W). This includes the significant effect of dissipation through the package leads and the PCB on which the package is mounted, and the temperature of the ambient air. Test results for this 24-lead SOIC are approximately 35 °C/W when mounted on a high-thermally conductive PCB (based on the JEDEC standard PCB, having four layers with buried copper areas).

The total power that can be applied to the device, $P_{D(lim)}$ (W), is affected by the maximum allowable device junction temperature, $T_{J(max)}$ (°C), $R_{\theta JA}$, and the ambient air temperature, T_A (°C), as shown in the following formula

$$P_{D(lim)} = (T_{J(max)} - T_A) / R_{\theta JA}$$

$P_{D(lim)}$ can be estimated based on several parameters, using the following formula

$$P_{D(lim)} = P_{D(Ibias)} + P_{D(V5A)} + P_{D(V5D)} + P_{D(buckdc)} + P_{D(buckac)} + P_{D(BD)}$$

where

$$P_{D(Ibias)} = V_{BB} \times I_{BB}$$

$$P_{D(V5A)} = (V_{REG} - 5\ V) \times I_{LOAD(V5A)}$$

$$P_{D(V5D)} = (V_{REG} - 5\ V) \times I_{LOAD(V5D)}$$

$$P_{D(buckdc)} = I_{LOAD}^2 \times R_{DSON(TJmax)} \times DC$$

$$P_{D(buckac)} = I_{LOAD} \times [V_{BB}(5\ ns / 14\ V) \times V_{BB}] \times 0.5\, f_{PWM}$$

$$P_{D(BD)} = I_{V33BD(max)} \times (V_{REG} - 4\,V) + I_{VADJBD(max)} \times (V_{REG} - V_{ADJ} - 0.7\,V)$$

and

$$I_{LOAD} = I_{LOAD(V33)} + I_{LOAD(VADJ)} + I_{LOAD(V5D)} + I_{LOAD(V5A)}$$

R_{DSON} is a function of T_J. For the purposes of estimating $P_{D(lim)}$, the relationship can be assumed to be linear throughout the practical T_J operating range (see test conditions for R_{DSON} in the Electrical Characteristics table).

DC (duty cycle) is a function of V_{BB} and V_{REG}. This can be calculated precisely as

$$DC = V_{REG(off)} / (V_{REG(on)} + V_{REG(off)})$$

A rough estimate for DC is

$$DC = (V_{REG} + V_{LX}) / V_{BB}$$

$I_{V33BD(max)}$ is the maximum current drawn on the V33BD pin. It is dependent on I_{OUTV33} and the h_{FE} of the pass transistor.

$I_{ADJBD(max)}$ is the maximum current drawn on the VADJBD pin. It is dependent on $I_{OUTVADJ}$ and the h_{FE} of the pass transistor.

Overcurrent Protection

The current supplied by the 3.3 V and the 1.2 to 3.3 V adjustable regulators is limited to I_{CL}. Current above I_{CL} is folded back linearly, as shown in figure 4b. In the case of a shorted load, the collector current is reduced to 40% of I_{CL} ±10%, to ensure protection of the pass transistors. After the short is removed, the voltage recovers to its regulated level.

The maximum power dissipated in the transistor during a shorted load condition is:

$$P_D \approx (V_{REG} - V_{OUT}) \times (0.4 \times I_{CL})$$

where V_{OUT} = 0 V.

Low Input Voltage Operation

When the charge pump has ramped enough to enhance the buck switch, the buck converter switching regulator is enabled. This occurs at $V_{BB} \approx 5.7$ V. At that point, the duty cycle, DC, of the A8450 can be forced to 100% until V_{IN} is high enough to allow the switch to begin operating normally. The point at which normal switching begins is dependent on ambient temperature, T_A. Increases in T_A cause R_{DSON} to increase. Other significant factors are I_{LOAD}, V_{REG}, the ESR of the output inductor (L1), and the forward biasing voltage for the output Schottky diode (D1).

Regulator Bypass

Some applications may not require the use of all four regulators provided in the A8450. For the regulators that are not used, the corresponding external components are not needed.

If either or both of the two 5 V regulators are not required by the application, bypass an unused regulator by not connecting its output terminal, V5D or V5A. Also, the corresponding output capacitor, C1 or C2, is not used.

For the 3.3 V regulator and the 1.2 V to 3.3 V adjustable regulator, if either or both are not needed, the corresponding external components are not used. In addition, if the 3.3 V regulator is not used, CL33 and V33 are not connected. If the adjustable regulator is not used, CLADJ and FB are not connected. However, to ensure stability of the A8450, the base drive pin, V33BD or VADJBD, of any unused regulator must be shorted to VREG.

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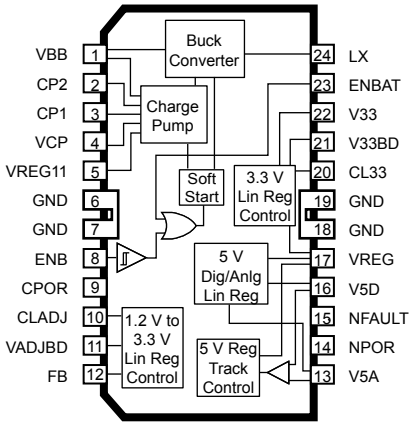
Pinout Diagram



Terminal List Table

Name	Description	Number
VBB	Supply input	1
CP2	Charge pump capacitor, positive side	2
CP1	Charge pump capacitor, negative side	3
VCP	Charge pump output used to drive N-channel buck converter transistor	4
VREG11	Internal reference	5
GND	Power ground	6
GND	Power ground	7
ENB	Logic control	8
CPOR	Connection for POR adjustment	9
CLADJ	Current limit for adjustable regulator	10
VADJBD	Base drive for adjustable regulator pass transistor	11
FB	Feedback for adjustable regulator	12
V5A	5 V analog regulator output	13
NPOR	Power on Reset logic output	14
NFAULT	Diagnostic output; open drain; low during fault condition	15
V5D	5 V digital regulator output	16
VREG	DC-to-DC converter supply output	17
GND	Power ground	18
GND	Power ground	19
CL33	Current limit for 3.3 V regulator	20
V33BD	Base drive for 3.3 V regulator pass transistor	21
V33	3.3 V regulator output	22
ENBAT	High voltage logic control	23
LX	Buck converter switching regulator output	24

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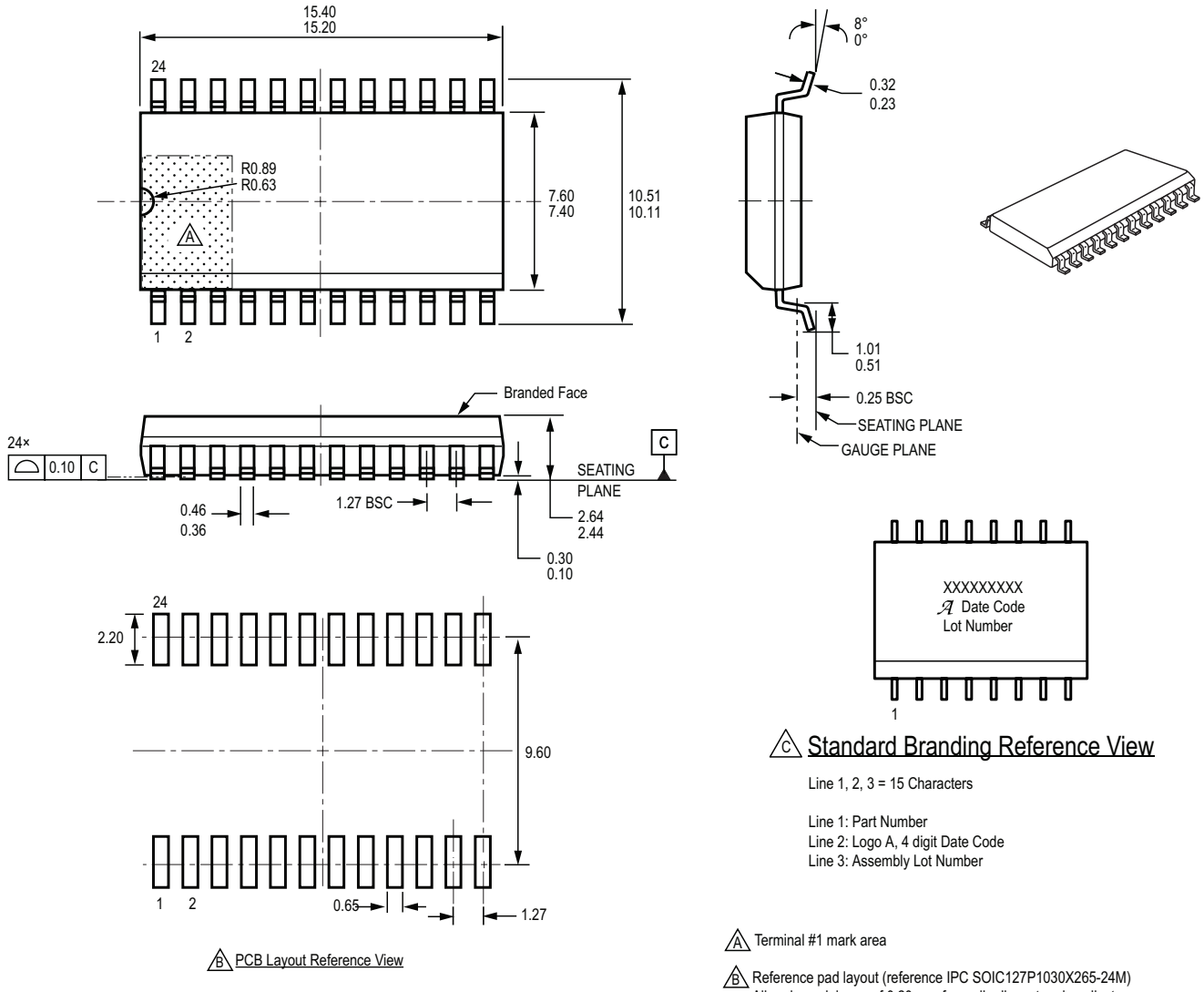
Package LB, 24-Pin SOICW

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000388, Rev. 1 and JEDEC MS-013AD)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
Internal configuration of fused pins is device-dependent



B PCB Layout Reference View

C Standard Branding Reference View

Line 1, 2, 3 = 15 Characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Assembly Lot Number

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

Leads 6 and 7, and 18 and 19 are internally fused ground leads, for enhanced thermal dissipation.

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Revision History

Number	Date	Description
8	January 30, 2012	Update product availability
9	May 14, 2020	Minor editorial updates
10	May 9, 2022	Updated package drawing (page 16) and other minor editorial updates

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