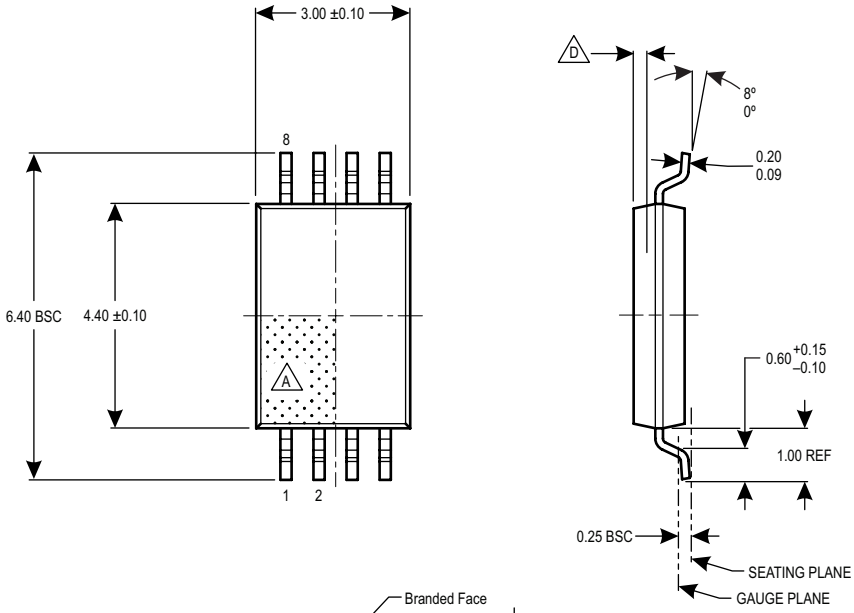
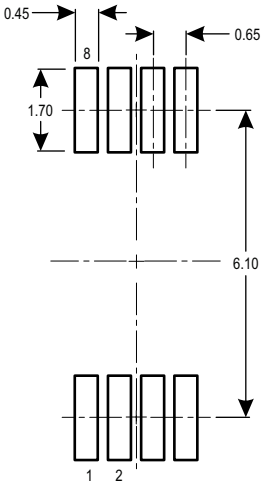
Package Drawing

Designator: LU
Type: 8-pin TSSOP

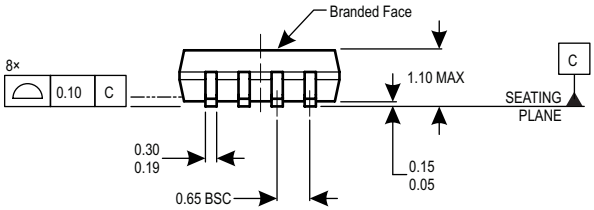
For Reference Only – Not for Tooling Use

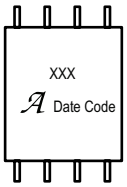
(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153AA)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





B PCB Layout Reference View





C Standard Branding Reference View

Line 1: Maximum 3 characters
Line 2: Maximum 5 characters

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Active Area Depth 0.36 mm REF

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